

# **2N2274 AND** SILICON PRECISION-ALLOY

ESIGNED FOR low-level chopper applications, Type 2N2274 Silicon Precision-Alloy Transistors feature extremely low leakage current, low offset voltage, and uniquely low inverted dynamic saturation resistance.

### ABSOLUTE MAXIMUM RATINGS

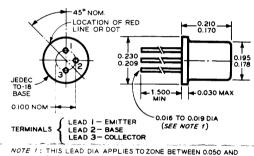
Storage Temperature65 C to $+$ 140 C
Collector Voltage, V <sub>CBO</sub>
Collector Voltage, $V_{CEO}$
Emitter Voltage, $V_{EBO}$
Emitter Voltage, $V_{ECO}$
Collector Current, $I_C$
Total Device Dissipation <sup>2</sup> at 25 C
Lead Temperature at 1/16" ± 1/32" from case

The maximum ratings are limiting absolute values above which the serviceability may be impaired from the viewpoint of life or satisfactory performance. The breakdown voltages may be far above the maximum voltage ratings. To avoid permanent damage to the transistors, do not attempt to measure these characteristics above the maximum ratings.

<sup>2</sup> Due to the nature of these transistors, the dissipation in the base emitter circuit may be appreciable under high base drive conditions and must be included in the total device dissipation. For temperatures above 25 C, derate by 1.3 mw/°C.

Type 2N2275 SPAT® identifies matched pairs of Type 2N2274 transistors with an offset voltage match guaranteed over the temperature range of +25 C to +65 C.

#### ACTUAL SIZE **MECHANICAL SPECIFICATIONS**



THIS LEAD DIA APPLIES TO ZONE BETWEEN 0.050 AND 0.250 FROM BASE SEAT. IN ZONE BETWEEN 0.250 AND 0.050, A MAX OF 0.021 DIA IS HELD. OUTSIDE OF THESE ZONES, THE LEAD DIA IS NOT CONTROLLED.

# ELECTRICAL CHARACTERISTICS at T = 25 C

	CHARACTERISTICS		TEST COND	OITIONS		MIN.	TYP.	MAX.	UNITS
		D - C	CHARAC	TERI	STICS				
ICBO	Collector Cutoff Current	V <sub>CB</sub>	= -10V					3	nA
ICBO	Collector Cutoff Current	$V_{CB}$	= -10V	T ==	+65 C	_		45	nA
I <sub>EBO</sub>	Emitter Cutoff Current	V <sub>EB</sub>	= -10V				_	3	nA
I <sub>EBO</sub>	Emitter Cutoff Current	V <sub>EB</sub>	= -10V	τ =	+65 C		_	45	nA
I <sub>E</sub> CO	Emitter Current	VEC	= -10V		·			3	nA
BV <sub>CBO</sub>	Collector Breakdown Voltage	lc	$= -1 \mu A$			25			volts
BVCEO	Collector Breakdown Voltage	lč	$= -10\mu A$			25		_	volts
BVEBO	Emitter Breakdown Voltage	ΙĒ	$= -1 \mu A$			25	_		volts
BVECO	Emitter Breakdown Voltage	1 <sub>E</sub>	$= -1 \mu A$			25			volts
V <sub>RT</sub>	Reach Through Voltage	$\bar{V}_{EB}$	$= -1\dot{V}$			25			volts
hFE	D-C Amplification Factor	VCE	= -0.5V	lc	= -5mA	10	15		70113
VOFF	Offset Voltage	I <sub>B</sub>	$= -500 \mu A$		÷		1.8	3.0	mV
VOFF	Offset Voltage	I <sub>B</sub>	≃ −1mA			_	2.1	3.25	mV
VOFF	Offset Voltage	ΙB	= -1.5  mA			_	2.4	3.5	mV
	HIGH	FREQ	UENCY CI	HAR	ACTERI	STICS			
rs	Inverted Dynamic Saturation Re-						<del></del>		
	sistance <sup>4</sup>	lв	= -1.5 mA	lε	$= 100 \mu A$	4	11	1 <i>7</i>	ohms
Cib	Input Capacitance	V <sub>EB</sub>	= -6V	lc	= 0 f = 4	∮mc —	4	6	рF
Cob	Output Capacitance	V <sub>CB</sub>	= -6V	ΙE	= 0 f = 4	1mc —	6	9	pF
Ceb	Emitter Diode Capacitance <sup>5</sup>	ΙE	$= 0.25 \mu A$	ť	= 10mc	_	12	16	pF
<del></del>	Emitter Diode Recovery Time <sup>6</sup>	lB	= -1.5mA no	m.		_	6	1.5	μsec
fT	Gain Bandwidth Product	VCE	= -6V	le	= 1  mA f = 4	4mc 6	9	_	mc
	TYPE	2 N 2 2	75 MAT	HED	PAIR	DATA			
△Voff	Differential Offset Voltage <sup>7</sup>	IB	= -1.5 mA				_	100	μ٧
	*	TA	= +25C  to  +	65C					•

<sup>3</sup>Typical values are for engineering guidance only.

<sup>4</sup>To be measured in circuit of Figure 1. . "SPAT" is a registered trademark of the Philco Corp. <sup>5</sup>To be measured in circuit of Figure 2

<sup>6</sup>To be measured in circuit of Figure 3.

<sup>7</sup>To be measured in circuit of Figure 4.

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TRANSISTOR DIVISION CONCORD, N. H.

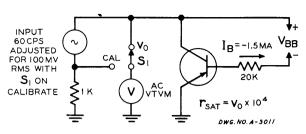


FIGURE 1
INVERTED DYNAMIC r<sub>s</sub> TEST CIRCUIT

The inverted dynamic saturation resistance, which is the slope of the  $V_{OFF}$ ,  $I_E$  characteristic at a specified base current, is measured in the circuit shown in Figure 1. The circuit reads  $r_s$  directly as the ratio of the a-c collector voltage,  $V_o$  to a calibrated a-c collector current.

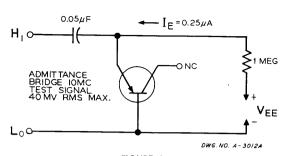


FIGURE 2
EMITTER DIODE CAPACITANCE TEST CIRCUIT

Figure 2 shows the test circuit for the measurement of the emitter diode capacitance,  $C_{eb}$ . The measurement is made with the emitter diode slightly forward biased (IE  $=0.25\mu\text{A}$ ). The 10 MC test signal from the admittance bridge should be less than 40 MV RMS.

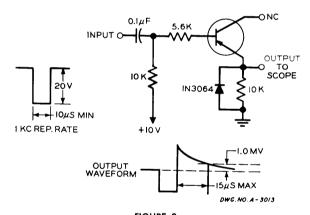


FIGURE 3 EMITTER DIODE RECOVERY TIME TEST CIRCUIT

The emitter diode reverse recovery time, a measure of the transient response of the chopper, is measured in the circuit of Figure 3. The measurement is made as the time for the emitter current to recover from a specified forward value to a specified reverse value. The IN3064 diode across the 10K emitter resistance serves to clamp the emitter potential to reduce the output voltage change to a convenient level.

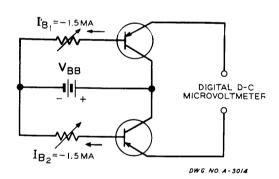


FIGURE 4
DIFFERENTIAL OFFSET VOLTAGE MATCH TEST CIRCUIT

The offset voltage match,  $\triangle v_{OFF}$ , is measured in the circuit of Figure 4. The difference in the offset voltage at the specified base current is measured with a digital voltmeter.

In the construction of the components described, the full intent of the specification will be met. The Sprague Electric Company, however, reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the design of its products. Components made under military approvals will be in accordance with the approval requirements.

The information included herein is believed to be accurate and reliable. However, the Sprague Electric Company assumes no responsibility for its use; nor for any infringements of patents or other rights of third parties which may result from its use.

ISSUE OF JUNE, 1964

# 2N2276 AND 2N2277 SILICON PRECISION-ALLOY TRANSISTORS

EXTREMELY LOW leakage current, low offset voltage, and uniquely low inverted dynamic saturation resistance are the prime characteristics of Type 2N2276 Silicon Precision-Alloy Transistors, designed for use in low-level chopper applications.

### ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

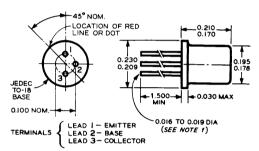
Storage Temperature65 C to $+$ 140 C
Collector Voltage, V <sub>CBO</sub>
Collector Voltage, V <sub>CEO</sub>
Emitter Voltage, V <sub>EBO</sub> 15 volts
Emitter Voltage, $V_{ECO}$
Collector Current, Ic
Total Device Dissipation <sup>2</sup> at 25 C
Lead Temperature at $\frac{1}{16}$ " $\pm \frac{1}{32}$ " from case
230 C for 10 sec

<sup>1</sup> The maximum ratings are limiting absolute values above which the serviceability may be impaired from the viewpoint of life or satisfactory performance. The breakdown voltages may be far above the maximum voltage ratings. To avoid permanent damage to the transistors, do not attempt to measure these characteristics above the maximum ratings.

Type 2N2277 SPAT® identifies matched pairs of Type 2N2276 Transistors with an offset voltage guaranteed over the temperature range of +25 C to +65 C.



#### MECHANICAL SPECIFICATIONS



NOTE 1: THIS LEAD DIA APPLIES TO ZONE BETWEEN 0.050 AND
0.250 FROM BASE SEAT. IN ZONE BETWEEN 0.250 AND
0.050, A MAX OF 0.021 DIA IS HELD. OUTSIDE OF THESE
ZONES, THE LEAD DIA IS NOT CONTROLLED.

# ELECTRICAL CHARACTERISTICS $^3$ at T = 25 C

		-	17414744						
	CHARACTERISTICS		TEST COND			MIN.	TYP.	MAX.	UNITS
		D - C	CHARAC	TERIS	TICS				
Сво	Collector Cutoff Current	V <sub>CB</sub>	= -10V				_	3	nA
ICBO	Collector Cutoff Current	VCB	= -10V	T = -	+65 C	_	_	45	n A
I <sub>EBO</sub>	Emitter Cutoff Current	VEB	= -10V			_	_	3	nA
1 <sub>EBO</sub>	Emitter Cutoff Current	V <sub>EB</sub>	= -10V	T = -	+65 C	_		45	nA
I <sub>E</sub> CO	Emitter Current	V <sub>EC</sub>	= -6V			_		3	nA
BVCBO	Collector Breakdown Voltage	lc	$= -1 \mu A$			15		_	volts
BVCEO	Collector Breakdown Voltage	١c	$= -10\mu$ A			10	_	_	volts
BVEBO	Emitter Breakdown Voltage	ΙĒ	$= -1 \mu A$			15		_	volts
BVECO	Emitter Breakdown Voltage	ΙĒ	$= -1 \mu A$			10	_		volts
V <sub>RT</sub>	Reach Through Voltage	V <sub>EB</sub>	= -10			10	_		volts
hFE	D-C Amplification Factor	VCE	= -0.5V	lc =	-5mA	10	15		_
VOFF	Offset Voltage	l <sub>B</sub>	$= -500 \mu A$			_	0.8	2.0	m۷
VOFF	Offset Voltage	ĺв	= -1 mA				1.1	2.25	m۷
VOFF	Offset Voltage	l <sub>B</sub>	= 1.5 mA				71.4	2.5	mV
	нісн	FREQ	UENCY CI	I A R A	CTERIST	ICS			
rs	Inverted Dynamic Saturation Resistance <sup>4</sup>		= -1.5mA	l <sub>E</sub>	= 100μA	4	10	17	
<b>C</b>		l <sub>B</sub>	= -1.5mA = -6V	ie Ic	$= 0 0 \mu$ A $= 0 f = 4 mc$			17	ohms
Cib	Input Capacitance	VEB				_	4	6	рF
Сор	Output Capacitance	V <sub>СВ</sub>	= -6V	l <u>e</u>	= 0 f = 4me = 10mc	-	.0	9	pF
C <sub>eb</sub>	Emitter Diode Capacitance <sup>5</sup>	ŀΕ	$= 0.25 \mu A$		= IOMC	_	12	16	pF
<del></del>	Emitter Diode Recovery Time <sup>6</sup>	IB	= -1.5mA no	_		<del>-</del>	•	15	μsec
f <sub>T</sub>	Gain Bandwidth Product	VCE	= -6V		= 1 mA f = 4 mc	6	9		mc
		TYPE 21	N2277 MATCH	ED PA	R DATA				
△VOFF	Differential Offset Voltage <sup>7</sup>	IB	= -1.5mA						
		TA	= +25C to +	65C				_	100µV
					7				

<sup>3</sup>Typical values are for engineering guidance only.

<sup>4</sup>To be measured in circuit of Figure 1. "SPAT" is a registered trademark of the Philco Corp. <sup>5</sup>To be measured in circuit of Figure 2.

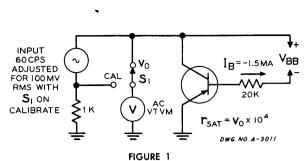
<sup>6</sup>To be measured in circuit of Figure 3.

<sup>7</sup>To be measured in circuit of Figure 4.

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<sup>&</sup>lt;sup>2</sup> Due to the nature of these transistors, the dissipation in the base emitter circuit may be appreciable under high base drive conditions and must be included in the total device dissipation. For temperatures above 25 C, derate by 0.8 mw/ $^{\circ}$ C.



INVERTED DYNAMIC IS TEST CIRCUIT

The inverted dynamic saturation resistance, which is the slope of the VOFF,  $I_E$  characteristic at a specified base current, is measured in the circuit shown in Figure 1. The circuit reads  $r_s$  directly as the ratio of the a-c collector voltage,  $V_o$  to a calibrated a-c collector current.

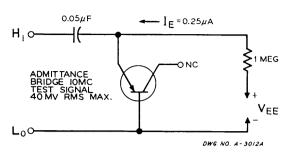


FIGURE 2
EMITTER DIODE CAPACITANCE TEST CIRCUIT

Figure 2 shows the test circuit for the measurement of the emitter diode capacitance,  $C_{eb}.$  The measurement is made with the emitter diode slightly forward biased (I $_{\rm E}=0.25\,\mu{\rm A}).$  The 10 MC test signal from the admittance bridge should be less than 40 MV RMS.

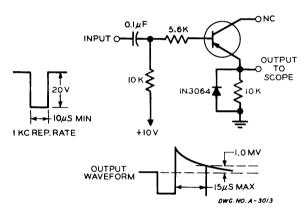


FIGURE 3
EMITTER DIODE RECOVERY TIME TEST CIRCUIT

The emitter diode reverse recovery time, a measure of the transient response of the chopper, is measured in the circuit of Figure 3. The measurement is made as the time for the emitter current to recover from a specified forward value to a specified reverse value. The IN3064 diode across the 10K emitter resistance serves to clamp the emitter potential to reduce the output voltage change to a convenient level.

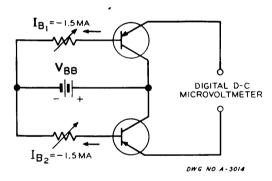


FIGURE 4
DIFFERENTIAL OFFSET VOLTAGE MATCH TEST CIRCUIT

The offset voltage match,  $\triangle v_{OFF}$ , is measured in the circuit of Figure 4. The difference in the offset voltage at the specified base current is measured with a digital voltmeter.

In the construction of the components described, the full intent of the specification will be met. The Sprague Electric Company, however, reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the design of its products. Components made under military approvals will be in accordance with the approval requirements.

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# TYPE 2N2278 AND 2N2279 SILICON PRECISION-ALLOY TRANSISTORS

ESIGNED FOR low-level chopper applications, Type 2N2278 Silicon Precision-Alloy Transistors feature extremely low leakage current, low offset voltage, and uniquely low inverted dynamic saturation resistance.

Type 2N2279 SPAT® identifies matched pairs of Type 2N2278 Transistors with an offset voltage match guaranteed over the temperature range of +25 C to +85 C.



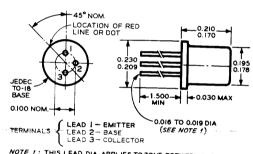
#### **ABSOLUTE MAXIMUM RATINGS'**

Storage Temperature65 C to $+$ 140 C
Collector Voltage, $V_{CBO}$
Collector Voltage, V <sub>CEO</sub>
Emitter Voltage, V <sub>EBO</sub>
Emitter Voltage, V <sub>ECO</sub>
Collector Current, I <sub>C</sub>
Total Device Dissipation <sup>2</sup> at 25 C
Lead Temperature at 1/16" ± 1/32" from case
000 01 10

The maximum ratings are limiting absolute values above which the serviceability may be impaired from the viewpoint of life or satisfactory performance. The breakdown voltages may be far above the maximum voltage ratings. To avoid permanent damage to the transistors, do not attempt to measure these characteristics above the maximum ratings.

2 Due to the nature of these transistors, the dissipation in the base emitter circuit may be appreciable under high base drive conditions and must be included in the total device dissipation. For temperatures above 25 C, derate by 1.3 mw/°C.

### MECHANICAL SPECIFICATIONS



THIS LEAD DIA APPLIES TO ZONE BETWEEN 0.050 AND 0.250 FROM BASE SEAT. IN ZONE BETWEEN 0.250 AND 0.050, A MAX OF 0.021 DIA IS HELD. OUTSIDE OF THESE ZONES, THE LEAD DIA IS NOT CONTROLLED.

# ELECTRICAL CHARACTERISTICS at T = 25 C

	CHARACTERISTICS	TEST CONDITIONS			MIN.	TYP.	MAX.	UNITS	
		D - C	CHARA	CTE	RISTICS				
ICBO	Collector Cutoff Current	V <sub>CB</sub>	= -10V					1	
Ісво	Collector Cutoff Current	V <sub>CB</sub>	= -10V	T =	+65C			15	n/
I <sub>EBO</sub>	Emitter Cutoff Current	VEB	= -10V		, , , ,		_	13	nA
I <sub>EBO</sub>	Emitter Cutoff Current	VEB	= -10V	T =	+65C	_	_	16	nA
I <sub>E</sub> CO	Emitter Current	VEC	= -10V	•	1000		_	15	nA
<b>BV</b> CBO	Collector Breakdown Voltage	lc	= -10nA			15		i	nA
BVCEO	Collector Breakdown Voltage	lc	$= -1 \mu A$			15	_	_	volts
BVEBO	Emitter Breakdown Voltage	l <sub>E</sub>	= -10nA				_		volts
BVECO	Emitter Breakdown Voltage	le .	= -10nA			1.5	_	_	volts
VOFF	Offset Voltage	'E 10	$= -500\mu$ A			15		_	vo its
VOFF	Offset Voltage	1B	= -1 mA				0.9	1.3	m۷
VOFF	Offset Voltage	ŧВ Is					1.0	1.75	m۷
TOFF		IB IB	= -1.5mA				1.2	2.25	m۷
	НІСН	FREC	UENCY	CHA	RACTERIS	STICS			
rs	Inverted Dynamic Saturation Resiste	ance4 lg	= -1mA	I <sub>E</sub>	= 100μA	7	13	18	ohms
Cib	Input Capacitance	V <sub>EB</sub>	= -6V	Ιc		lmc —	1.4	7	
Cob	Output Capacitance	V <sub>CB</sub>	= -6V	l <sub>E</sub>		lmc —	7	ć	pF
Ceb	Emitter Diode Capacitance <sup>5</sup>	le T	$= 0.25 \mu A$	f	= 10mc		12	16	pF
	Emitter Diode Recovery Time <sup>6</sup>	l <sub>B</sub>	= -1mA nor	n.		_	6		рF
f <u>T</u>	Gain Bandwidth Product	VCE	= -6V	I <sub>E</sub>	= 1mA f = 4	mc 7.6	12	15	μsec
		MA	TCHED	PAIR	DATA	7.0			m c
△V <sub>OFF</sub>	Differential Offset Voltage <sup>7</sup>	lg	= -1mA						
		TA	= +25C to	+85C		_	_	50	μ٧

<sup>3</sup>Typical values are for engineering guidance only.

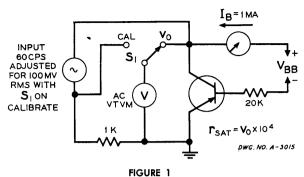
<sup>4</sup>To be measured in circuit of Figure 1. "SPAT" is a registered trademark of the Philco Corp. <sup>5</sup>To be measured in circuit of Figure 2.

<sup>6</sup>To be measured in circuit of Figure 3

<sup>7</sup>To be measured in circuit of Figure 4

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INVERTED DYNAMIC IS TEST CIRCUIT

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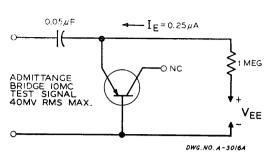


FIGURE 2
EMITTER DIODE CAPACITANCE TEST CIRCUIT

Figure 2 shows the test circuit for the measurement of the emitter diode capacitance,  $C_{eb}.$  The measurement is made with the emitter diode slightly forward biased (IE  $=0.25\mu\text{A}).$  The 10 MC test signal from the admittance bridge should be less than 40 MV RMS.

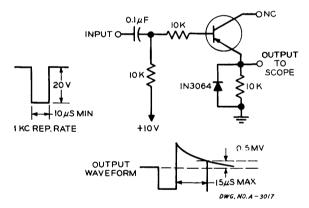


FIGURE 3
RECOVERY TIME TEST CIRCUIT

The emitter diode reverse recovery time, a measure of the transient response of the chopper, is measured in the circuit of Figure 3. The measurement is made as the time for the emitter current to recover from a specified forward value to a specified reverse value. The IN3064 diode across the 10K emitter resistance serves to clamp the emitter potential to reduce the output voltage change to a convenient level.

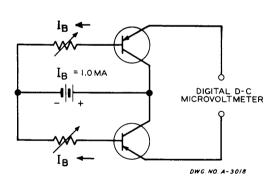


FIGURE 4
MATCHED OFFSET VOLTAGE TEST CIRCUIT

The offset voltage match,  $\triangle V_{OFF}$ , is measured in the circuit of Figure 4. The difference in the offset voltage at the specified base current is measured with a digital voltmeter.

In the construction of the components described, the full intent of the specification will be met. The Sprague Electric Company, however, reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the design of its products. Components made under military approvals will be in accordance with the approval requirements.

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# TYPE 2N2280 AND 2N2281 SILICON PRECISION-ALLOY TRANSISTORS

DFSIGNED FOR low-level chopper applications, Type 2N2280 Silicon Precision-Alloy Transistors feature extremely low leakage current, low offset voltage, and a very low inverted dynamic saturation resistance. Type 2N2280 transistor in matched pairs with an offset voltage match guaranteed over the temperature range of +25 C to +65 C are identified as Type 2N2281 SPAT® Transistors.

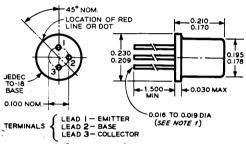


#### ABSOLUTE MAXIMUM RATINGS

Storage Temperature $\dots -65$ C to	o + 140 C
Collector Voltage, V <sub>CBO</sub>	— 10 volts
Collector Voltage, V <sub>CEO</sub>	6 volts
Emitter Voltage, V <sub>EBO</sub>	10 volts
Emitter Voltage, V <sub>ECO</sub>	6 volts
Collector Current, I <sub>C</sub>	— 50 ma
Total Device Dissipation <sup>2</sup> at 25 C	150 mw
Lead Temperature at $\frac{1}{6}$ " $\pm \frac{1}{32}$ " from case	

<sup>1</sup> The maximum ratings are limiting absolute values above which the serviceability may be impaired from the viewpoint of life or satisfactory performance. The breakdown voltages may be far above the maximum voltage ratings. To avoid permanent damage to the transistors, do not attempt to measure these characteristics above the maximum ratings.

#### **MECHANICAL SPECIFICATIONS**



NOTE 1: THIS LEAD DIA APPLIES TO ZONE BETWEEN 0.050 AND 0.250 FROM BASE SEAT. IN ZONE BETWEEN 0.250 AND 0.050, ANMAY OF 0.021 DIA IS HELD. OUTSIDE OF THESE ZONES, THE LEAD DIA IS NOT CONTROLLED.

DWG. NO. 4-3806

# ELECTRICAL CHARACTERISTICS $^3$ at T = 25 C

	CHARACTERISTICS		TEST	CONDITIONS	MIN.	TYP.	MAX.	UNITS
		D - C	CHARA	CTERISTICS				
Ісво	Collector Cutoff Current	V <sub>CB</sub>	= - 6V		_		3	nA
ICBO	Collector Cutoff Current	VCB	= - 6V	T = +65C	_		50	nA
I <sub>EBO</sub>	Emitter Cutoff Current	VEB	= - 6V		_	_	3	nA
I <sub>EBO</sub>	Emitter Cutoff Current	VEB	= - 6V	T = +65C	_		50	nA
BVCBO	Collector Breakdown Voltage	lc	$= -10\mu A$	·	10		_	volts
BVCEO	Collector Breakdown Voltage	lc	$= -25 \mu A$		6		_	volts
BVEBO	Emitter Breakdown Voltage	lĒ	$= -10\mu A$		10	_	_	volts
BVECO	Emitter Breakdown Voltage	ΙĘ	$= -10\mu A$		6	_		volts
VCE(SAT)	Collector Saturation Voltage	lč	= -5 mA	$l_B = -0.8 mA$	_	0.05	0.1	volt
VBE	Base Voltage	Ĩċ	= -5 mA	$l_B = -0.8 \text{ mA}$		0.9	1.35	volt
VOFF	Offset Voltage	la.	$= -250 \mu A$		_	0.6	1.0	mV
VOFF	Offset Voltage	İB	= -1mA			0.7	1.5	mV
VOFF	Offset Voltage	l <sub>B</sub>	= -1.5 mA			1.0	2.0	mV
	HIGH	FREQ	UENCY	CHARACTERIS	TICS			
rs	Inverted Dynamic Saturation Resi	stance <sup>4</sup> IB	= -1 mA	$I_E = 100 \mu A$	5	10	18	ohms
Cib	Input Capacitance	VEB	= -3V	lc = 0 $f = 4mc$	. —	5	8	pF
Соь	Output Capacitance	VCB	= -3V	$I_E = 1 \text{ mA f} = 4 \text{ mc}$	_	7	10	pF
	Emitter Diode Recovery Time <sup>5</sup>	l <sub>B</sub>	= -1  mA nom		_	6	15	μsec
fT	Gain Bandwidth Product	VCE	= -3V	le = 1 mA f = 4 mc	16	24	<u></u>	mc
		MAT	CHED P	AIR DATA				
△Voff	Differential Offset Voltage <sup>6</sup>	lв	= -1mA					
		TA	= +25C to $-$	⊢65 C			100	μV

<sup>&</sup>lt;sup>3</sup>Typical values are for engineering guidance only.

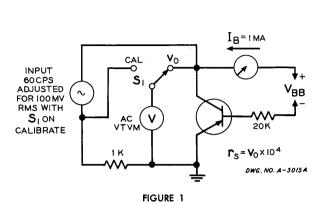
"SPAT" is a registered trademark of the Philco Corp.

 $<sup>^2</sup>$  Due to the nature of these transistors, the dissipation in the base emitter circuit may be appreciable under high base drive conditions and must be included in the total device dissipation. For temperatures above 25 C, derate by 1.3 mw/°C.

<sup>&</sup>lt;sup>4</sup>To be measured in circuit of Figure 1.

<sup>&</sup>lt;sup>5</sup>To be measured in circuit of Figure 2.

<sup>&</sup>lt;sup>6</sup>To be measured in circuit of Figure 3.



INVERTED DYNAMIC IS TEST CIRCUIT

The inverted dynamic saturation resistance, which is the slope of the V<sub>EC</sub>, I<sub>E</sub> characteristic at a specified base current, is measured in the circuit shown in Figure 1. The circuit reads  $r_S$  directly as the ratio of the a-c collector voltage,  $V_o$  to a calibrated a-c collector current.

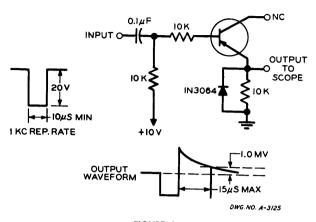
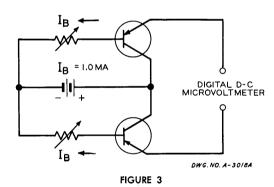


FIGURE 2

#### EMITTER DIODE RECOVERY TIME TEST CIRCUIT

The emitter diode reverse recovery time, a measure of the transient response of the chopper, is measured in the circuit of Figure 2. The measurement is made as the time for the emitter current to recover from a specified forward value to a specified reverse value. The IN3064 diode across the 10K emitter resistance serves to clamp the emitter potential to reduce the output voltage change to a convenient level.



#### MATCHED OFFSET VOLTAGE TEST CIRCUIT

The offset voltage match,  $\triangle V_{OFF}$ , is measured in the circuit of Figure 3. The difference in the offset voltage at the specified base current is measured with a digital voltmeter.

In the construction of the components described, the full intent of the specification will be met. The Sprague Electric Company, however, reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the design of its products. Components made under military approvals will be in accordance with the approval requirements.

The information included herein is believed to be accurate and reliable. However, the Sprague Electric Company assumes no responsibility for its use; nor for any infringements of patents or other rights of third parties which may result from it use.

1SSUE OF APRIL 1964

# TYPE 2N2377 P-N-P SILICON PRECISION-ALLOY TRANSISTORS

DESIGNED for amplifier and oscillator applications at frequencies through 15 megacycles, Type 2N2377 Silicon Precision-Alloy Transistors may be operated at junction temperatures up to 140 C with excellent performance. The Type 2N2377 is electrically identical to Types 2N495 and 2N1118 but is housed in the JEDEC TO-18 case.

Rated at 150 mw total dissipation with a collector voltage rating of 25 volts, Type 2N2377 SPAT® transistors feature low leakage currents and low saturation voltage. The amplifier stage gain at 140 C is within a few db of the gain at room temperature.

ABSOLUTE MAXIMUM RATINGS

Particularly well-suited for hightemperature applications, such as in airborne equipment, 2N2377 transistors are designed to meet the environmental requirements of Military Specification MIL-S-19500.



**ACTUAL SIZE** 

0.210

0.016 TO 0.019 DIA (SEE NOTE 1)

# MECHANICAL SPECIFICATIONS

0.028
0.048 DETERMINED BY SUBTRACTING DIA A FROM B 0.041±0.005

LEAD 1 - EMITTER LEAD 2 - BASE LEAD 3 - COLLECTOR

45°-TAB FOR VISUAL ORIENTATION ONLY

THIS LEAD DIA APPLIES TO ZONE BETWEEN 0.050 AND 0.250 FROM BASE SEAT. IN ZONE BETWEEN 0.250 AND 0.500, A MAX OF 0.021 DIA IS HELD. OUTSIDE OF THESE ZONES, THE LEAD DIA IS NOT CONTROLLED.

#### Storage Temperature .... ..... $-65\,\mathrm{C}$ to $+140\,\mathrm{C}$ Total Device Dissipation<sup>3</sup> at 25 C .150 mW Derating Factor above 25 C...... 1.3 mW °C Lead Temperature at $\frac{1}{16}$ " $\pm \frac{1}{32}$ " from case ...230 C for 10 sec

<sup>1</sup>The maximum ratings are limiting absolute values above which the serviceability may be impaired from the viewpoint of life or satisfactory performance.

<sup>2</sup>In this class of transistors, the maximum collector voltage is limited by

FIFCTBICAL

20NES, 1 HE LEAD DIA IS NOT CONTROLLED.

NOTE 2: MAX DIA LEADS AT GAGING PLANE 0.054 \$0.000 BELOW
BASE SEAT TO BE WITHIN 0.007 OF TRUE LOCATION
RELATIVE TO MAX WIDTH TAB AND TO 0.230 MAX DIA
MEASURED WITH SUITABLE GAGE. WHEN GAGE IS NOT
USED, MEASUREMENT MADE AT BASE SEAT. the punchthrough phenomenon <sup>3</sup>Due to the nature of this transistor, the dissipation in the base emitter

# circuit may be appreciable under high base drive conditions and must be included in the total device dissipation. (See Input Characteristic Curves.)

0.100 -(NOTE 2)

	ELECTRICAL	CHARACTERISTICS* (	at T =	25 C		
	CHARACTERISTICS	TEST CONDITIONS	MIN.	TYPICAL	MAX.	UNITS
	D	-C CHARACTERISTIC	S			UNITS
ICBO IEBO BVCEO hfe	Collector Cutoff Current <sup>5</sup> Emitter Cutoff Current Collector Voltage Collector Voltage	$V_{CB} = -25 \text{ V}$ $V_{EB} = -10 \text{ V}$ $I_{CEO} = -25 \mu A$ $V_{CE} = 0.5 \text{ V}$ $I_{CE} = -5 \text{ m}$		.002 .001 — 25	1.0 0.1 — 100	μΑ μΑ volts
	SMALL				100	
h <sub>fe</sub> f <sub>[</sub>	Current Amplification Factor Gain Bandwidth Product	$V_{CE} = -6 V$ $I_{E} = 1 mA$ $V_{CE} = -6 V$ $I_{E} = 1 mA$	15	30 20	120	mc mc
r <sub>b</sub> 'C <sub>c</sub>	Extrinsic Base Resistance Collector Capacitance Product	f = 4 mc $VCE = -6 V$	_	1450	5000	psec
C <sub>ob</sub>	Output Capacitance	$V_{CE} = -6 V$ $I_E = 1 mA$ $f = 4 mC$	_	6	12	pF
h <sub>ib</sub> h <sub>ob</sub>	Input Resistance Output Admittance	$V_{CE} = -6 V$ $I_{E} = 1 mA$ $V_{CE} = -6 V$ $I_{E} = 1 mA$	_	40 1.5	90 2.5	ohms µmhos

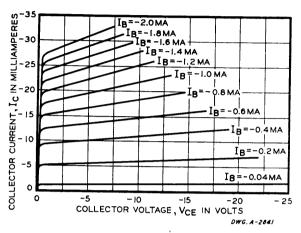
<sup>4</sup>Typical values are for engineering guidance only.

The saturation current will approximately double with every 10 C of temperature. With ratings at any collector voltage then, the ICBO may be calculated for any temperature by doubling the low voltage I<sub>CBO</sub> for every 10 C and adding the difference between the room temperature I<sub>CBO</sub> at the desired voltage and the room temperature ICBO at low voltage. "SAT" is a registered trademark of the Philco Corp.

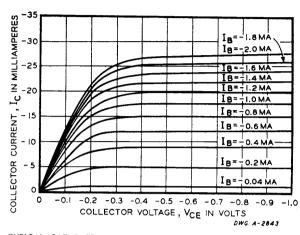
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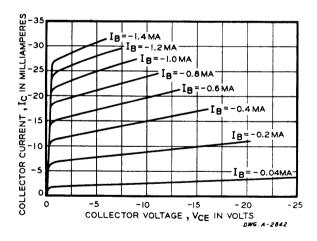
# **CHARACTERISTIC CURVES OF TYPE 2N2377 TRANSISTORS**



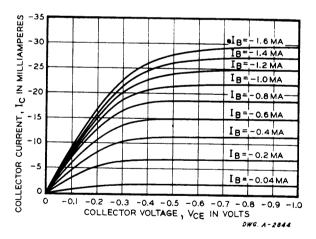
TYPICAL COLLECTOR CHARACTERISTICS
IN GROUNDED EMITTER CONFIGURATION
AT 25 C



TYPICAL SATURATED REGION COLLECTOR CHARACTERISTICS
IN GROUNDED EMITTER CONFIGURATION
AT 25 C

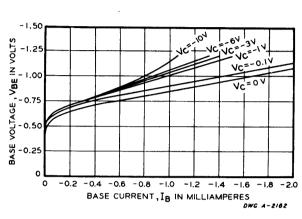


TYPICAL COLLECTOR CHARACTERISTICS IN GROUNDED EMITTER CONFIGURATION AT 125 C

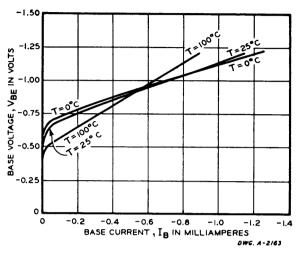


TYPICAL SATURATED REGION COLLECTOR CHARACTERISTICS
IN GROUNDED EMITTER CONFIGURATION
AT 125 C

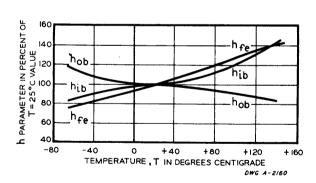
# CHARACTERISTIC CURVES OF TYPE 2N2377 TRANSISTORS - - cont.



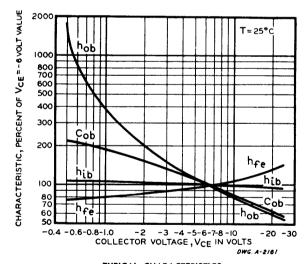
TYPICAL INPUT CHARACTERISTICS
IN GROUNDED EMITTER CONFIGURATION
AT 25 C



TYPICAL INPUT CHARACTERISTICS
IN GROUNDED EMITTER CONFIGURATION
AT 125 C

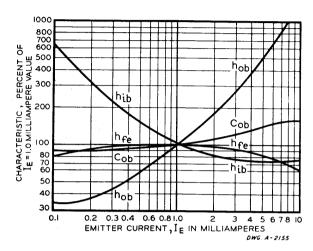


TYPICAL h PARAMETERS AS A FUNCTION OF TEMPERATURE NORMALIZED FOR 25 C WITH  $V_{CE} = -6$  VOLTS,  $I_E = 1.0$  MA



TYPICAL CHARACTERISTICS AS A FUNCTION OF COLLECTOR VOLTAGE NORMALIZED FOR  $V_{CE}=-6$  VOLTS WITH  $I_E=1.0$  MA

# CHARACTERISTIC CURVES OF TYPE 2N2377 TRANSISTORS - - cont.



TYPICAL CHARACTERISTICS AS A FUNCTION OF EMITTER CURRENT NORMALIZED FOR  $I_E = 1.0$ . MA WITH  $V_{CE} = -6$  VOLTS

In the construction of the components described, the full intent of the specification will be met. The Sprague Electric Company, however, reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the design of its products. Components made under military approvals will be in accordance with the approval requirements.

# TYPE 2N2378 P-N-P SILICON PRECISION-ALLOY TRANSISTORS

HIGH-SPEED switching at high temperatures is the major application for the Type 2N2378 Silicon Precision - Alloy Transistors. The frequency at which  $\beta$  equals unity ( $f_T$ ) is typically about 20 megacycles. The Type 2N2378 is electrically identical with Types 2N496 and 2N1119 but is housed in the JEDEC TO-18 case.

Since the saturation resistance is typically less than 10 ohms, the voltage drop at saturation is in the order of a tenth of a volt. Consequently, there is very low power dissipation in the "on" condition. This permits the designer to gain the advantages of low voltage operation and minimum load impedance.

#### **ABSOLUTE MAXIMUM RATINGS**<sup>1</sup>

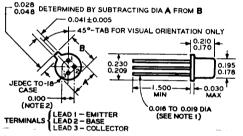
Storage Temperature $-65$ (	C to $+140$ $C$
Collector Voltage <sup>2</sup> , V <sub>CB</sub> or V <sub>CE</sub>	10 volts
Collector Current, Ic	50 mA
Derating Factor above 25 C	1.3 mW/°C
Total Device Dissipation <sup>3</sup> at 25 C	150 mW
Lead Temperature at $\frac{1}{16}$ " $\pm \frac{1}{22}$ " from case	
	10 C for 10 sec

<sup>1</sup>The maximum ratings are limiting absolute values above which the serviceability may be impaired from the viewpoint of life or satisfactory performance. The diode breakdown and punchthrough voltages may be far above the maximum collector voltage rating. For this reason it is important that the 2N2378 not be tested above the maximum voltage rating to avoid permanent damage to the transistor.

Because the input voltage is usually four or five times the saturation voltage even at elevated temperatures, Type 2N2378 SPAT® transistors are particularly suited for direct coupled switching circuits. They feature very low leakage currents and a 150 mw rated dissipation at 25 C ambient temperature.



ACTUAL SIZE



NOTE 1: THIS LEAD DIA APPLIES TO ZONE BETWEEN 0.050 AND 0.250 FROM BASE SEAT. IN ZONE BETWEEN 0.250 AND 0.500, A MAX OF 0.021 DIA IS HELD. OUTSIDE OF THESE ZONES, THE LEAD DIA IS NOT CONTROLLED.

NOTE 2: MAX DIA LEADS AT GAGING PI ANE 0.054 +9.00° DEI OW.

NOTE 2: MAX DIA LEAD DIA IS NOT CONTROLLED.

NOTE 2: MAX DIA LEADS AT GAGING PLANE 0.000 BELOW
BASE SEAT TO BE WITHIN 0.007 OF TRUE 10.000 BELOW
RELATIVE TO MAX WIDTH TAB AND TO 0.230 MAX DIA
MEASURED WITH SUITABLE GAGE. WHEN GAGE IS NOT
USED, MEASUREMENT MADE AT BASE SEAT.

\*\*PRE-NO.4-1459\*\*

<sup>2</sup>In this class of transistor, the maximum collector voltage is limited by the punchthrough phenomenon.

<sup>3</sup>Due to the nature of this transistor, the dissipation in the base emitter circuit may be appreciable under high base drive conditions and must be included in the total device dissipation. (See Input Characteristic Curves.)

## ELECTRICAL CHARACTERISTIC at T = 25 C

	CHARACTERISTICS	TEST CONDITIONS	MIN.	TYPICAL	MAX.	UNITS
	D - C	CHARACTERISTIC	: S			
Ісво	Collector Cutoff Current <sup>5</sup>	$V_{CB} = -10V$		.001	0.1	μΑ
I <sub>EBO</sub>	Emitter Cutoff Current	$V_{EB} = -10V$		.001	0.1	μA
ICEX	Collector Cutoff Current	$V_{CE} = -4.5V$ $V_{BE} = -0.45V$	_	5	25	μA
BVCEO	Collector Breakdown Voltage	$I_{C} = -25 \text{ uA}$	_	_	10	volts
hae	Current Amplification Factor	$V_{CE} = -0.5V$ Ic = -15 mA	15	25	_	_
VCE (SAT)	Collector Voltage	$I_{C} = -5 \text{ mA}  I_{B} = -0.8 \text{ m/s}$	A —	0.08	0.15	volts
VBE	Input Voltage	$I_{C} = -5 \text{ mA}$ $I_{B} = -0.8 \text{ m/s}$	A 0.75	0.9	1.0	volts
	SMALL	SIGNAL PARAME	TERS			
fr	Gain Bandwidth Product	$V_{CE} = -6 V$ $f = 4 mc$ $I_{E} = 1 mA$	7.2	20	_	mc
r <sub>b</sub> 'C <sub>c</sub>	Extrinsic Base Resistance	$V_{CE} = -6 V$ $I_E = 1 mA$	_	1500	5000	psec
	Collector Capacitance Product	$V_{CE} = -6 V$ $I_{E} = 1 mA$	_	6	12	•
Cop	Output Capacitance	1 CE 0 1 1E 1 111A		U	12	рF
K's	Hole Storage <sup>6</sup>	$l_B = -1 \text{ mA}$	_	90	175	nsec

<sup>4</sup>Typical values are for engineering guidance only.

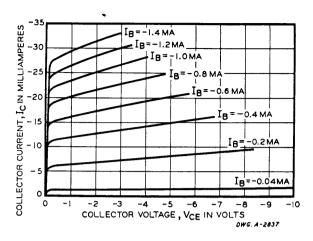
The saturation current will approximately double with every 10 C of temperature. At any collector voltage, then, the I<sub>CBO</sub> may be calculated for any temperature by doubling the low voltage I<sub>CBO</sub> for every 10 C and adding the difference between the room temperature I<sub>CBO</sub> at the desired voltage and the room temperature I<sub>CBO</sub> at low voltage.

To be tested in hole storage circuit. See page 4.

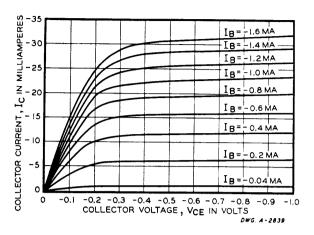
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#### CHARACTERISTIC CURVES OF TYPE 2N2378 TRANSISTORS

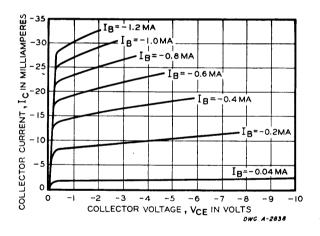


TYPICAL COLLECTOR CHARACTERISTICS IN GROUNDED EMITTER CONFIGURATION AT 25 C

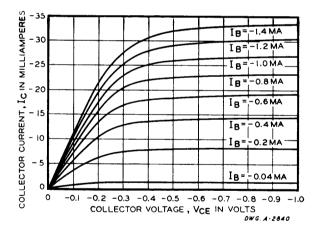


TYPICAL SATURATED REGION COLLECTOR CHARACTERISTICS IN GROUNDED EMITTER CONFIGURATION

AT 25 C

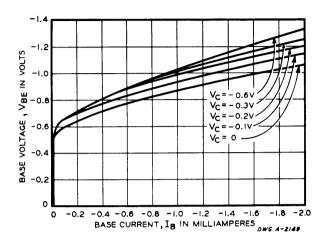


TYPICAL COLLECTOR CHARACTERISTICS IN GROUNDED EMITTER CONFIGURATION AT 125 C

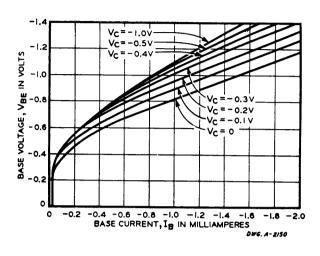


TYPICAL SATURATED REGION COLLECTOR CHARACTERISTICS
IN GROUNDED EMITTER CONFIGURATION
AT 125 C

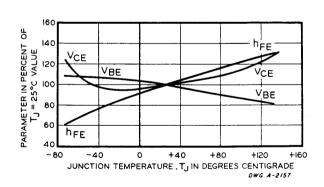
# CHARACTERISTIC CURVES OF TYPE 2N2378 TRANSISTORS - - cont.



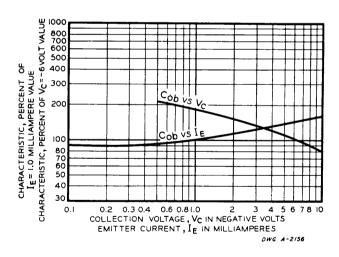
TYPICAL INPUT CHARACTERISTICS
IN GROUNDED EMITTER CONFIGURATION
AT 25 C



TYPICAL INPUT CHARACTERISTICS
IN GROUNDED EMITTER CONFIGURATION
AT 125 C

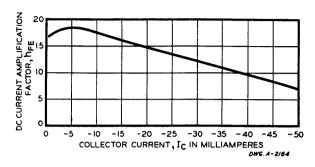


TYPICAL PARAMETERS
AS A FUNCTION OF JUNCTION TEMPERATURE
NORMALIZED FOR 25 C



TYPICAL CHARACTERISTICS AS A FUNCTION OF COLLECTOR VOLTAGE AND EMITTER CURRENT AT 25 C

#### CHARACTERISTIC CURVES OF TYPE 2N2378 TRANSISTORS - - cont.



TYPICAL D-C β
AS A FUNCTION OF COLLECTOR CURRENT
IN GROUNDED EMITTER CONFIGURATION
AT 25 C

#### HOLE STORAGE MEASUREMENT OF TYPE 2N2378 TRANSISTORS

The hole storage factor  $K_{s}'$  is a device constant defined as the excess stored charge (in saturation) per unit excess base current, where excess base current is the amount of current supplied to the base in excess of that required to just keep the transistor in saturation. While the hole storage factor may be expressed in units of time, this is not a time measurement and does not imply that the storage time in any particular circuit is that specified.

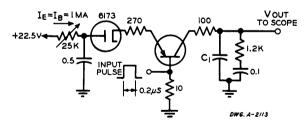
The storage time in an actual circuit is a function of the ratio of both the "turn-on" base current and

the "turn-off" base current to the "on" collector current. The storage time will be approximately

$$\begin{array}{c} t_{\text{S}} = K_{\text{S}}' \; \text{In} \frac{I_{\text{B1}} \; + \; I_{\text{B2}}}{I_{\text{CS}}} \\ \frac{I_{\text{CS}}}{h_{\text{FF}}} \; + \; I_{\text{B2}} \end{array} \; , \label{eq:ts}$$

where  $I_{B1}$  is the "turn-on" base current,  $I_{B2}$  is the "turn-off" base current (assumed to be reverse current) and  $I_{CS}$  is the "on" collector current.

#### HOLE STORAGE TEST CIRCUIT



 $C_1$ , rated at 500 pF, includes probe or scope capacitance. This value should be measured with the differentiating network disconnected.

$$K_s' = \frac{C_I \ V_{OUT}}{I_E} = \frac{500}{I} \frac{\mu \mu coulombs}{mA}$$
 (These units are the equivalent of nsec.)

In the construction of the components described, the full intent of the specification will be met. The Sprague Electric Company, however, reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the design of its products. Components made under military approvals will be in accordance with the approval requirements.