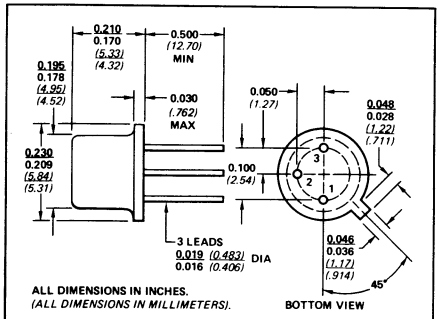
Performance Curves MA
See Page 4-1

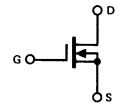
N-CHANNEL DEPLETION-TYPE MOS SILICON FIELD-EFFECT TRANSISTOR

- $R_{IN} > 10^{15}\ \Omega$
- I_{DSS} Change Typically - 15% From 25° to 100°C
- Audio and Radio Frequency Applications



TO-18

Substrate and case connected to source pin



PIN	OUT
1	S, B, C
2	G
3	D

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Source Voltage	20 V
Gate-to-Channel Voltage (Note 1)	±60 V
Drain Current	20 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature (Note 2)	300 mW
Storage Temperature Range	-65 to 200°C
Lead Temperature 1/16" From Case For 10 Sec	255°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	BV_{DSX}	Drain-Source Breakdown Voltage	20			V	$I_D = 1\ \mu A$, $V_{GS} = -10$ V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-3.5	-6.0		$V_{DS} = 10$ V, $I_D = 1\ \mu A$	
3		V_{GS}	Gate-Source Voltage	-0.7		-5.5		$V_{DS} = 10$ V, $I_D = 200\ \mu A$	
4		I_{DSS}	Saturation Drain Current	2		10	mA	$V_{DS} = 10$ V, $V_{GS} = 0$	
5		$I_{D(off)}$	Drain Cutoff Current			100	pA	$V_{DS} = 5$ V, $V_{GS} = -10$ V	
6		r_{GS}	Common-Source Parallel Input Resistance	10^{15}	10^{16}		Ω	$V_{DS} = 10$ V, $I_D = 0.15$ mA	
7		$r_{DS(on)}$	Drain-Source ON Resistance (Note 3)		300	550		$V_{GS} = 0$, $V_{DS} = 0$	f = 1 kHz
8					100			$V_{GS} = 10$ V, $V_{DS} = 0$	
9	DYNAMIC	g_{os}	Common-Source Output Conductance			120	μmho	$V_{DS} = 10$ V, $V_{GS} = 0$	f = 1 kHz
10		g_{fs}	Common-Source Forward Transconductance	1,400	2,000	2,800			
11		$\lvert y_{fs} \rvert$	Common-Source Forward Transadmittance	1,400			pF		f = 50 MHz
12		C_{iss}	Common-Source Input Capacitance (Output Shorted)		6.8	7.5			f = 140 kHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance			1.6			f = 1 MHz

* JEDEC registered data

MA

Notes

1 Permanent damage may result if voltages greater than ±60 volts are applied to the gate

2 Derate linearly to 175°C free-air temperature at rate of 2 mW/°C

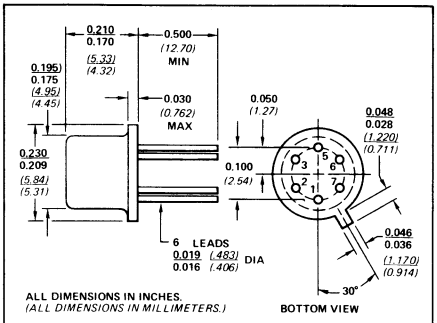
3 Not JEDEC registered data.

Performance Curves NRL
See Page 4-41

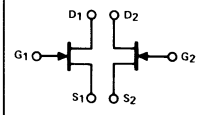
MATCHED DUAL N-CHANNEL SILICON JUNCTION FIELD-EFFECT TRANSISTORS

MATCHED FET PAIRS FOR DIFFERENTIAL AMPLIFIERS

- $I_G < 250$ pA (25 nA at 100°C)
- $g_{oss} < 20$ μmhos ($I_D = 700$ μA)
- Matched V_{GS}, ΔV_{GS}, and g_{fs}



TO-71



PIN	OUT	PIN	OUT
1	S_1	5	S_2
2	D_1	6	D_2
3	G_1	7	G_2

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage ..... -50 V
Gate Current ..... 50 mA
Total Device Dissipation
(Derate 1.7 mW/°C to 200°C) ..... 300 mW
Storage Temperature Range ..... -65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-1	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-1	μA		100°C
3		BV_{DGO}	Drain-Gate Breakdown Voltage	50			I_D = 1 μA, I_S = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-3	V	V_{DS} = 10 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0.2	-2.7		V_{DS} = 10 V, I_D = 100 μA	
6		I_G	Gate Operating Current		-250	pA	V_{DG} = 10 V, I_D = 700 μA	
7					-25	nA		100°C
8		I_{DSS}	Saturation Drain Current (Note 1)	1	10	mA	V_{DS} = 10 V, V_{GS} = 0	
9	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	1500	7500	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
10		g_{os}	Common-Source Output Conductance		35			
11		C_{iss}	Common-Source Input Capacitance		18	pF		
12		C_{rss}	Common-Source Reverse Transfer Capacitance		6			
13		g_{fs}	Common-Source Forward Transconductance	1500		μmho	V_{DG} = 10 V, I_D = 700 μA	f = 1 kHz
14		g_{oss}	Common-Source Output Conductance		20			
15		NF	Spot Noise Figure		2	dB	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz, R_G = 1 meg

		Characteristic		2N3921		2N3922		2N4084		2N4085		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max			
16	MATCH	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		15		15	mV	V_{DG} = 10 V, I_D = 700 μA	T_A = 0°C, T_B = 100°C
17		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Voltage Change with Temperature		10		25		10		25	μV/°C		
18		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	–		f = 1 kHz

*JEDEC registered data.

NOTE:
1. Pulse test duration = 2 ms.

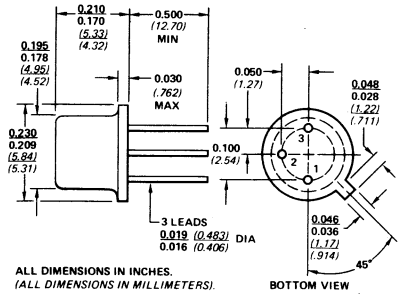
NRL

Performance Curves NC
See Page 4-23

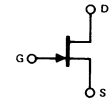
N-CHANNEL SILICON JUNCTION FIELD-EFFECT TRANSISTORS

FOR ANALOG SWITCHES, COMMUTATORS AND CHOPPERS

- $r_{DS(on)} < 25$ ohms (2N4856, 2N4859)
- $I_{D(off)} < 250$ pA



TO-18



PIN	OUT
1	S
2	D
3	G,C

*ABSOLUTE MAXIMUM RATINGS (25°C)

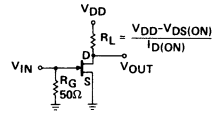
Reverse Gate-Drain or Gate-Source Voltage, 2N4856-8 ..... -40 V
Reverse Gate-Drain or Gate-Source Voltage, 2N4859-61 ..... -30 V
Gate Current ..... 50 mA
Total Device Dissipation at 25°C Case Temperature (Derate 10 mW/°C) ..... 1.8 W
Storage Temperature Range ..... -65 to +200°C
Lead Temperature (1/16" from case for 60 seconds) ..... 300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N4856,59 Min	2N4856,59 Max	2N4857,60 Min	2N4857,60 Max	2N4858,61 Min	2N4858,61 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS} Gate-Source Breakdown Voltage	2N4856-58	-40		-40		-40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2			2N4859-61	-30		-30		-30				
3		I_{GSS} Gate Reverse Current	2N4856-58		-250		-250		-250	pA	$V_{GS} = -20$ V, $V_{DS} = 0$	
4			2N4859-61		-500		-500		-500	nA	$V_{GS} = -15$ V, $V_{DS} = 0$	150°C
5		$I_{D(off)}$ Drain Cutoff Current			250		250		250	pA	$V_{DS} = 15$ V, $V_{GS} = -10$ V	
6					500		500		500	nA		150°C
7		$V_{GS(off)}$ Gate-Source Cutoff Voltage		-4	-10	-2	-6	-0.8	-4	V	$V_{DS} = 15$ V, $I_D = 0.5$ nA	
8		I_{DSS} Saturation Drain Current (Note 1)		50		20	100	8	80	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
9		$V_{DS(on)}$ Drain-Source ON Voltage			0.75 (20)		0.50 (10)		0.50 (5)	V (mA)	$V_{GS} = 0$, $I_D = (\ )$	
10	DYN	$r_{ds(on)}$ Drain-Source ON Resistance			25		40		60	ohm	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
11		C_{iss} Common-Source Input Capacitance			18		18		18	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
12		C_{rss} Common-Source Reverse Transfer Capacitance			8		8		8			
13	SWITCHING	t_d Turn-ON Delay Time			6 (20) [-10]		6 (10) [-6]		10 (5) [-4]	ns (ma) [V]	$V_{DD} = 10$ V, $R_L =$ 464 Ω 2N4856,59 / 953 Ω 2N4857,60 / 1910 Ω 2N4858,61	
14		t_r Rise Time			3 (20) [-10]		4 (10) [-6]		10 (5) [-4]	ns (mA) [V]	$V_{GS(on)} = 0$, $I_{D(on)} = (\ )$,	
15		t_{off} Turn-OFF Time			25 (20) [-10]		50 (10) [-6]		100 (5) [-4]	ns (mA) [V]	$V_{GS(off)} = (\ )$	

*JEDEC registered data.

NOTE:
1. Pulse test required, pulsewidth = 100 μs, duty cycle ⩽ 10%.



NC

INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75 ns
PULSE WIDTH 100 ns
PULSE DUTY CYCLE < 10%

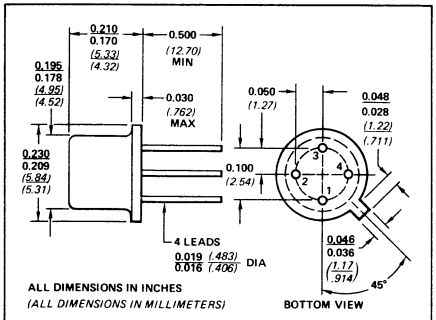
SAMPLING SCOPE
RISE TIME 0.75 ns
INPUT RESISTANCE 1 M
INPUT CAPACITANCE 2.5 pF

Performance Curves NU
See Page 4-47

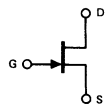
N-CHANNEL SILICON JUNCTION FIELD-EFFECT TRANSISTORS

FOR SMALL-SIGNAL AMPLIFIERS

- 2:1 I_{DSS} and g_{fs} Ranges
- $I_G < 1$ pA



TO-72



PIN	OUT
1	S
2	D
3	G
4	C

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage ..... -50 V
Gate Current ..... 10 mA
Total Device Dissipation (Derate 1.7 mW/°C) ..... 300 mW
Storage Temperature Range ..... -55 to +150°C
Maximum Operating Temperature ..... 150°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5647		2N5648		2N5649		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-10		-10		-10	pA	V_{GS} = -30 V, V_{DS} = 0	
2					-25		-25		-25	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.6	-1.8	-0.8	-2.4	-1	-3		V_{DS} = 15 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	0.3	0.6	0.5	1	0.8	1.6	mA	V_{DS} = 15 V, V_{GS} = 0	
6		I_G	Gate Operating Current		-1 (200)		-1 (400)		-1.5 (600)	pA (μA)	V_{DG} = 15 V, I_D = ( )	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	300	650	400	800	450	900	μmho	V_{DS} = 15 V, I_D = 200 μA, 2N5647; = 400 μA, 2N5648; = 600 μA, 2N5649	f = 1 kHz
8		g_{os}	Common-Source Output Conductance		5		7		10			
9		C_{rss}	Common-Source Reverse Transfer Capacitance		0.9		0.9		0.9	pF		f = 1 MHz
10		C_{iss}	Common-Source Input Capacitance		3		3		3			
11		$\bar{e}_n$	Equivalent Input Noise Voltage		0.1		0.1		0.1	$\frac{\mu V}{\sqrt{Hz}}$		f = 1 kHz
12		NF	Spot Noise Figure		1		1		1	dB		f = 1 kHz R_G=2.2 MΩ

*JEDEC registered data.

NU

NOTE:
1. Pulse test required pulsewidth 300 μs, duty cycle ≤ 3%.

n-channel enhancement-mode VMOS Power FETs *designed for . . .*

Siliconix

Performance Curves VNMA
See Section 3

- **High Speed Switching**
- **CMOS to High Current Interface**
- **TTL to High Current Interface**
- **High Frequency Linear Amplifiers**
- **Line Drivers**
- **DC to DC Converters**
- **Switching Power Supplies**

BENEFITS

- Directly Interfaces to CMOS, TTL, DTL and MOS Logic Families
  - Low Drive Current (I_{GSS} < 100 nA)
  - Threshold Voltage 0.8 to 2.0 V
- Permits More Efficient and Compact Switching Designs
  - Typical T_{ON} and T_{OFF} < 5 nsec
- Reduces Component Count and Design Time/Effort
  - Drives Inductive Loads Directly
  - Fan Out From a CMOS Logic Gate > 100
  - Easily Paralleled with Inherent Current Sharing Capability
  - High Gain
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Output Current Decreases as Temperature Increases

ABSOLUTE MAXIMUM RATINGS

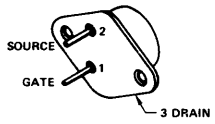
Maximum Drain-Source Voltage	
2N6656	35 V
2N6657	60 V
2N6658	90 V
Maximum Drain-Gate Voltage	
2N6656	35 V
2N6657	60 V
2N6658	90 V
Maximum Continuous Drain Current	2.0 A
Maximum Pulsed Drain Current (Note 1)	3.0 A
Maximum Gate-Source Voltage	*±15V**
Maximum Dissipation at 25°C Case Temperature	25 W
Linear Derating Factor	200 mW/°C
Temperature (Operating and Storage)	−55 to +150°C
Lead Temperature (1/16" from case for 10 sec)	300°C

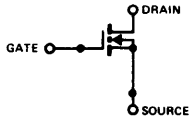
*JEDEC registered, but Siliconix guarantee ±30V

NOTE:

1. Pulse test — 80 μsec pulse, 1% duty cycle.

A-, Package
TO-3





2

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ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

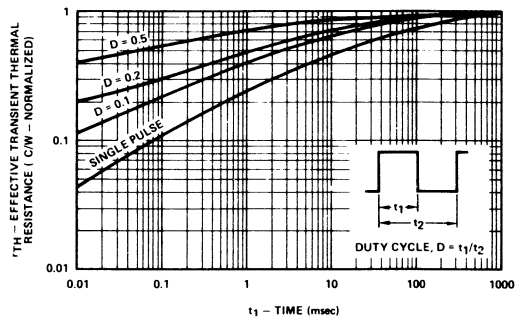
		Characteristic	2N6656 Min	2N6656 Typ	2N6656 Max	2N6657 Min	2N6657 Typ	2N6657 Max	2N6658 Min	2N6658 Typ	2N6658 Max	Unit	Test Conditions
1		BV_{DSS} Drain-Source Breakdown	35			60			90			V	V_{GS} = 0, I_D = 10 μA
2			35			60			90				V_{GS} = 0, I_D = 2.5 mA
3*		$V_{GS(th)}$ Gate Threshold Voltage	0.8		2.0	0.8		2.0	0.8		2.0		V_{DS} = V_{GS}, I_D = 1 mA
4*		I_{GSS} Gate-Body Leakage		0.5	100		0.5	100		0.5	100	nA	V_{GS} = 15 V, V_{DS} = 0
5*					500			500			500		V_{GS} = 15 V, V_{DS} = 0, T_A = 125 C (Note 2)
6*	STATIC	I_{DSS} Zero Gate Voltage Drain Current			10			10			10	μA	V_{DS} = Max. Rating, V_{GS} = 0
7*					500			500			500		V_{DS} = 0.8 Max. Rating, V_{GS} = 0, T_A = 125 C (Note 2)
8				100			100			100		nA	V_{DS} = 25 V, V_{GS} = 0
9*		$I_{D(on)}$ ON-State Drain Current (Note 1)	1.0	2		1.0	2		1.0	2		A	V_{DS} = 25 V, V_{GS} = 10 V
10		$V_{DS(on)}$ Drain-Source Saturation Voltage (Note 1)		0.3			0.3			0.4		V	V_{GS} = 5 V, I_D = 0.1 Amp
11				1.0	1.5		1.0	1.5		1.1	1.6		V_{GS} = 5V, I_D = 0.3 Amp
12				0.9			0.9			1.3			V_{GS} = 10 V, I_D = 0.5 Amp
13*				1.6	1.8		2.0	3.0		3.0	4.0		V_{GS} = 10 V, I_D = 1.0 Amp
14		$r_{DS(on)}$ Static Drain-Source ON-State Resistance		1.6	1.8		2.0	3.0		3.0	4.0	Ω	V_{GS} = 10 V, I_D = 1.0 Amp
15*		$r_{ds(on)}$ Small-Signal Drain-Source ON-State Resistance		1.6	1.8		2.0	3.0		3.0	4.0	Ω	V_{GS} = 10 V, I_D = 1.0, f = 1 kHz
16		g_{fs} Forward Transconductance (Note 1)	170	250		170	250		170	250		mΣ	V_{DS} = 24 V, I_D = 0.5 Amp
17*	DYNAMIC	C_{iss} Input Capacitance (Note 2)			50			50			50	pF	V_{GS} = 0, V_{DS} = 24 V, f = 1.0 MHz
18*		C_{ds} Drain-Source Capacitance (Note 2)			40			40			40		
19		C_{rss} Reverse Transfer Capacitance (Note 2)			10			10			10		V_{GS} = 0, V_{DS} = 24 V, f = 1.0 MHz
20*					35			35			35		V_{GS} = 0, V_{DS} = 0, f = 1.0 MHz
21*		$t_{d(on)}$ Turn-ON Delay Time (Note 2)		2	5		2	5		2	5	ns	See Switching Time Test Circuit VNMA, Section 3
22*		t_r Rise Time (Note 2)		2	5		2	5		2	5		
23*		$t_{d(off)}$ Turn-OFF Delay Time (Note 2)		2	5		2	5		2	5		
24*		t_f Fall Time (Note 2)		2	5		2	5		2	5		

*Indicates JEDEC registered data

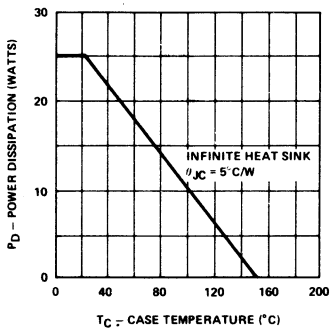
VNMA

NOTES:
1. Pulse test—80 μsec pulse, 1% duty cycle.
2. Sample test.

Thermal Response



Power Dissipation vs Case Temperature



DC Safe Operating Region T_C = 25°C