

2N497 • 2N498 • 2N656 • 2N657

NPN GENERAL PURPOSE HIGH VOLTAGE

DIFFUSED SILICON PLANAR* TRANSISTORS

GENERAL DESCRIPTION - These high voltage NPN double diffused silicon transistors are designed for use in high performance amplifier, oscillator and switching circuits.

**FOR IMPROVED PERFORMANCE
SEE FAIRCHILD 2N3108
OR 2N3114**

ABSOLUTE MAXIMUM RATINGS (25° C) [Note 1]

Maximum Temperatures

Storage Temperature

Operating Junction Temperature

Maximum Power Dissipation

Total Dissipation at Case Temperature 25° C [Note 2 & 3]
at Ambient Temperature 25° C

Maximum Voltages

V_{CB0} Collector to Base Voltage

V_{CEO} Collector to Emitter Voltage

V_{EBO} Emitter to Base Voltage

2N497/2N656

2N498/2N657

-65° C to +300° C

-65° C to +300° C

+200° C Maximum

+200° C Maximum

4.0 Watts

4.0 Watts

0.8 Watt

0.8 Watt

60 Volts

100 Volts

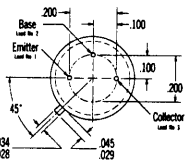
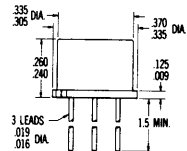
60 Volts

100 Volts

8.0 Volts

8.0 Volts

PHYSICAL DIMENSIONS
in accordance with
JEDEC (TO-5) outline



NOTES: All dimensions in inches
Leads are gold-plated copper
Collector internally connected to case

GUARANTEED ELECTRICAL CHARACTERISTICS (25° C unless otherwise noted)

Symbol	Characteristic	2N497		2N498		2N656		2N657		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
BV _{CBO}	Breakdown Voltage	60		100		60		100		Volts	I _C = 100 μA I _E = 0
BV _{CEO}	Breakdown Voltage	60		100		60		100		Volts	I _C = 250 μA I _B = 0
BV _{EBO}	Breakdown Voltage	8.0		8.0		8.0		8.0		Volts	I _E = 250 μA I _C = 0
I _{CBO}	Collector Cutoff Current		10		10		10		10	μA	I _E = 0 V _{CB} = 30 V
h _{FE}	Current Transfer Ratio	12	36	12	36	30	90	30	90		I _C = 200 mA V _{CE} = 10 V
h _{IE}	Input Impedance		500		500		500		500	ohms	I _B = 8.0 mA V _{CE} = 10 V
R _{CS}	Saturation Resistance		25		25		25		25	ohms	I _C = 200 mA I _B = 40 mA

TYPICAL ELECTRICAL CHARACTERISTICS (25° C unless otherwise noted)

Symbol	Characteristic	2N497-98		2N656-57	Units	Test Conditions
h _{FE}	DC Current Gain		27	60		I _C = 200 mA V _{CE} = 10 V
h _{FE}	DC Current Gain		20	45		I _C = 100 μA V _{CE} = 10 V
V _{BE} (sat)	Base Saturation Voltage		1.1	1.1	Volts	I _C = 200 mA I _B = 40 mA
C _{ob}	Collector Capacitance		13	13	pF	I _E = 0 V _{CB} = 10 V
C _{TE}	Emitter Transition Capacitance		60	60	pF	I _C = 0 V _{EB} = 0.5 V
I _{CBO}	Collector Cutoff Current		0.4	0.4	mμA	I _E = 0 V _{CB} = 90 V
I _{CBO}	Collector Cutoff Current (150° C)		1.5	1.5	μA	I _E = 0 V _{CB} = 90 V
h _{fe}	High Frequency Current Gain f = 20 MHz		2.5	3.5		I _C = 50 mA V _{CE} = 10 V
I _{EBO}	Emitter Current		0.1	0.1	mμA	I _C = 0 V _{EB} = 5.0 V

* Planar is a patented Fairchild process.

NOTES:

- (1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
- (2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operation.
- (3) These ratings give a maximum junction temperature of 200° C and junction-to-case thermal resistance of 43.8° C/Watt (derating factor of 22.8 mW/°C).

2N783

NPN HIGH-SPEED SWITCH

SILICON PLANAR* EPITAXIAL TRANSISTOR

**FOR IMPROVED PERFORMANCE
SEE FAIRCHILD 2N2369A**

GENERAL DESCRIPTION - The Fairchild 2N783 is an NPN silicon PLANAR epitaxial transistor designed specifically for high-speed, low-power saturated switching applications.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

Storage Temperature

-65°C to +300°C

Operating Junction Temperature

175°C Maximum

Maximum Power Dissipation

Total Dissipation at 25°C Case Temperature (Notes 2 and 3)

1.0 Watt

at 25°C Ambient Temperature (Notes 2 and 3)

0.3 Watt

Maximum Voltages and Current

V_{CBO} Collector to Base Voltage

40 Volts

V_{CER} Collector to Emitter Voltage ($R_{BE} = 10\Omega$)

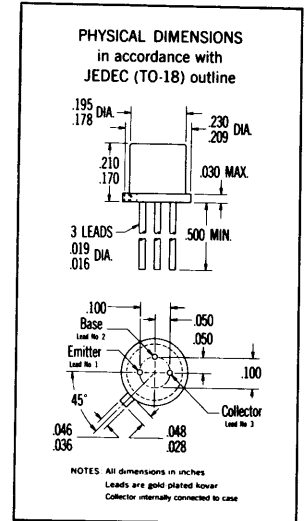
20 Volts

V_{EBO} Emitter to Base Voltage

5.0 Volts

I_C Collector Current

200 mA



ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

Symbol	Characteristic	Min.	Max.	Units	Test Conditions
h_{FE}	DC Current Gain	20 *	60		$I_C = 10 \text{ mA}$ $V_{CE} = 1.0 \text{ V}$
$V_{CE(sat)}$	Collector Saturation Voltage		0.25	Volts	$I_C = 10 \text{ mA}$ $I_B = 1.0 \text{ mA}$
$V_{BE(sat)}$	Base Saturation Voltage	0.7	0.9	Volts	$I_C = 10 \text{ mA}$ $I_B = 1.0 \text{ mA}$
I_{CBO}	Collector Cutoff Current		250	nA	$I_E = 0$ $V_{CB} = 25 \text{ V}$
$I_{CBO(150^\circ\text{C})}$	Collector Cutoff Current		30	μA	$I_E = 0$ $V_{CB} = 25 \text{ V}$
h_{fe}	High Frequency Current Gain ($f = 100 \text{ MHz}$)	2.0			$I_C = 10 \text{ mA}$ $V_{CE} = 10 \text{ V}$
C_{obo}	Output Capacitance ($f = 1.0 \text{ MHz}$)		3.5	pF	$I_E = 0$ $V_{CB} = 10 \text{ V}$
t_s	Storage Time (Note 4)		10	nsec	$I_C = 10 \text{ mA}$ $V_{CC} = 10 \text{ V}$
t_{on}	Turn On Time (Note 5)		16	nsec	$I_{B1} = 3.0 \text{ mA}$ $I_{B2} = 1.0 \text{ mA}$
t_{off}	Turn Off Time (Note 5)		30	nsec	$I_{B1} = 3.0 \text{ mA}$ $I_{B2} = 1.0 \text{ mA}$
BV_{CBO}	Collector to Base Breakdown Voltage	40		Volts	$I_E = 0$ $I_C = 100 \mu\text{A}$
BV_{CER}	Collector to Emitter Breakdown Voltage ($R_{BE} = 10\Omega$)	20		Volts	$I_C = 1.0 \text{ mA}$ $V_{BE} = 0$
BV_{EBO}	Emitter to Base Breakdown Voltage	5.0		Volts	$I_C = 0$ $I_E = 100 \mu\text{A}$

* Planar is a patented Fairchild process.

NOTES:

- (1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
- (2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.
- (3) These ratings give a maximum junction temperature of 175°C and junction-to-case thermal resistance of 150°C/Watt (derating factor of 6.67 mW/°C); junction-to-ambient thermal resistance of 500°C/Watt (derating factor of 2.0 mW/°C).
- (4) $I_{B1} = 10 \text{ mA}$, $I_{B2} = 10 \text{ mA}$, $R_L = 1 \text{ k}\Omega$, (see Figure 2).
- (5) $V_{CC} = 3.0 \text{ V}$, $R_L = 270\Omega$, (see Figure 1).



313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD TRANSISTOR — TYPE 2N783

FIGURE 1

TURN-ON AND TURN-OFF CIRCUIT

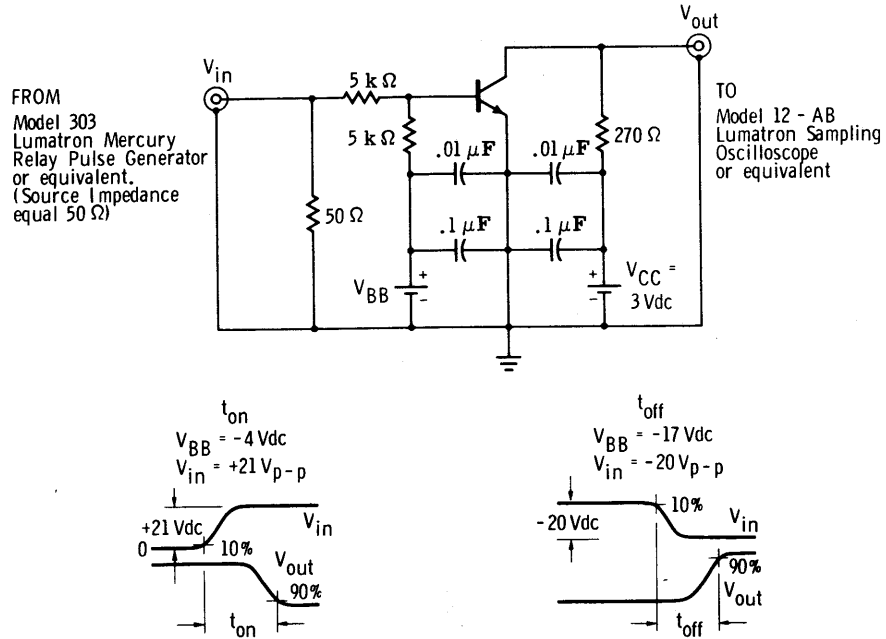
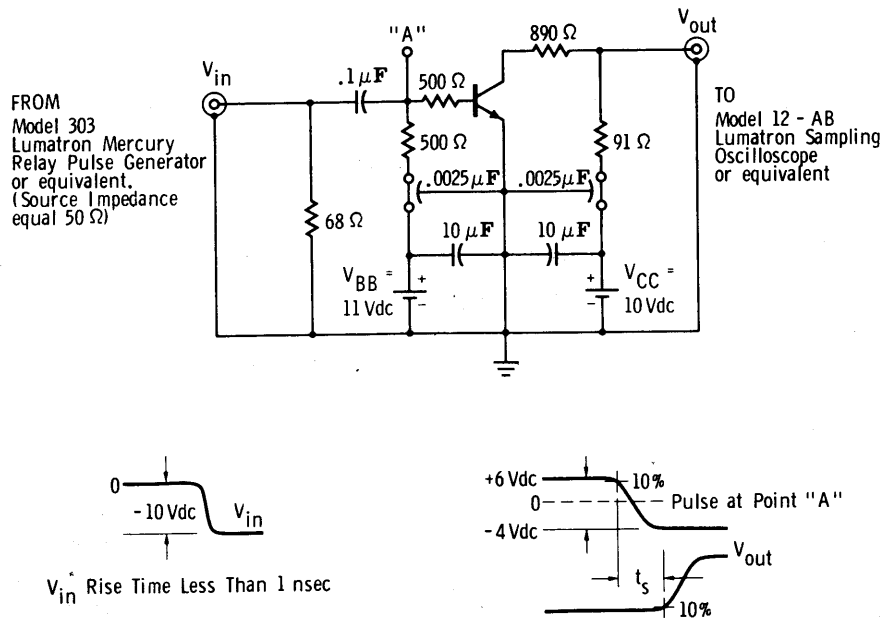


FIGURE 2

STORAGE TIME CIRCUIT



2N876 THROUGH 2N882

PNPN SILICON CONTROLLED RECTIFIERS

DIFFUSED SILICON PLANAR* THYRISTORS

- FORWARD CURRENT RATING OF 0.35 AMPS DC AT $T_C = 100^\circ\text{C}$
- BLOCKING VOLTAGE CAPABILITY TO 300 VOLTS
- MAXIMUM GATE TRIGGER CURRENT OF 200 μA AT $T_C = 25^\circ\text{C}$
- RELIABLE PLANAR CONSTRUCTION

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

†Storage Temperature	-65°C to +150°C
†Operating Temperature	-65°C to +150°C
†Lead Temperature (Soldering, 10 second time limit)	+230°C

Maximum Currents

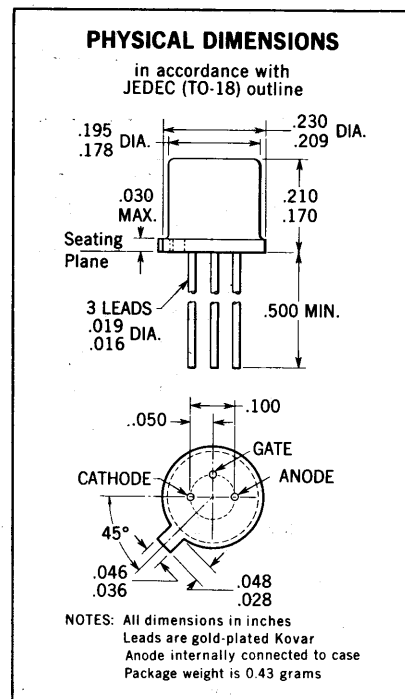
RMS Forward Current (180° Conduction Angle) (Note 2)	$T_C = 100^\circ\text{C}$	$I_{F(RMS)}$	430 mA
	$T_A = 25^\circ\text{C}$		300 mA
Continuous Forward Current (Note 2)	$T_C = 100^\circ\text{C}$	$I_{F(DC)}$	350 mA
	$T_A = 25^\circ\text{C}$		240 mA
Average Forward Current (180° Conduction Angle) (Note 2)	$T_C = 100^\circ\text{C}$	$I_{F(AV)}$	280 mA
	$T_A = 25^\circ\text{C}$		192 mA
†Peak Recurrent Forward Current (Repetition rate of 60 pps or higher, ≤ 0.01 duty cycle)	$T_C = 100^\circ\text{C}$	I_{FRM}	20 Amps

†Surge Current (Rectangular pulse of 0.2 ms duration, peak)	$T_C = 100^\circ\text{C}$	$I_{FM(surge)}$	20 Amps
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†Peak Forward Gate Current	$T_C = 100^\circ\text{C}$	I_{GFM}	250 mA
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Maximum Voltages ($T_C = -65^\circ\text{C}$ to $+100^\circ\text{C}$)

†Peak Reverse Gate Voltage	V_{GRM}	5.0 Volts
†DC Forward and Reverse Blocking Voltage	V_{FM}, V_{RM}	2N876 15 Volts 2N877 30 Volts 2N878 60 Volts 2N879 100 Volts 2N880 150 Volts 2N881 200 Volts 2N882 300 Volts



ELECTRICAL CHARACTERISTICS (25°C Case Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
† I_{FX}	Forward Blocking Current		0.004	10	μA	$V_{AK} = \text{Rated } V_{FM}, R_{GK} = 1.0 \text{ k}\Omega$
† $I_{FX}(125^\circ\text{C})$	Forward Blocking Current		1.5	100	μA	$V_{AK} = \text{Rated } V_{FM}, R_{GK} = 1.0 \text{ k}\Omega$
† I_{RX}	Reverse Blocking Current		0.004	10	μA	$V_{AK} = \text{Rated } V_{RM}, R_{GK} = 1.0 \text{ k}\Omega$
† $I_{RX}(125^\circ\text{C})$	Reverse Blocking Current		1.5	100	μA	$V_{AK} = \text{Rated } V_{RM}, R_{GK} = 1.0 \text{ k}\Omega$
† I_{GR}	Reverse Gate Current (except 2N882)		0.1	10	μA	$V_{GK} = -2.0 \text{ V}, I_A = 0$
† I_{GR}	Reverse Gate Current (2N882 only)		0.1	10	μA	$V_{GK} = -5.0 \text{ V}, I_A = 0$
† I_{GT}	Gate Trigger Current		100	200	μA	$V_{AA} = 5.0 \text{ V}, R_L = 100 \Omega, R_{GS} = 10 \text{ k}\Omega$
† V_{GT}	Gate Trigger Voltage	0.40	0.64	0.80	Volts	$V_{AA} = 5.0 \text{ V}, R_L = 100 \Omega, R_{GS} = 100 \Omega$
† I_{HX}	Holding Current		1.4	5.0	mA	$V_{AA} = 5.0 \text{ V}, I_G = -150 \mu\text{A}$
† V_F	On Voltage (Note 3)		1.0	1.5	Volts	$I_F = 200 \text{ mA}$
dV/dt	Critical Rate Of Rise Of Anode Voltage		95		V/ μs	$V_{AA} = \text{Rated } V_{FM}, R_{GK} = 1.0 \text{ k}\Omega$

†JEDEC Registered Values

*Planar is a patented Fairchild process.

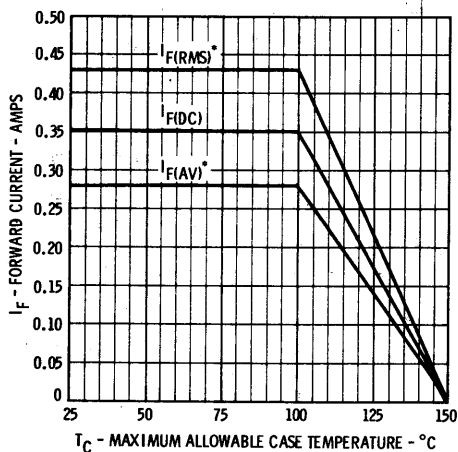
NOTES:

- (1) These ratings are limiting values above which the reliability of the device may be impaired.
- (2) These ratings give a maximum junction temperature of 150°C with the maximum average power dissipation and a maximum junction to case thermal resistance of 44.5°C/Watt and a junction to ambient thermal resistance of 350°C/Watt.
- (3) Pulse Conditions: Length = 300 μs ; Duty Cycle $\leq 2\%$.
- (4) Ambient temperature derating curves are derived with no external heat sink connected.

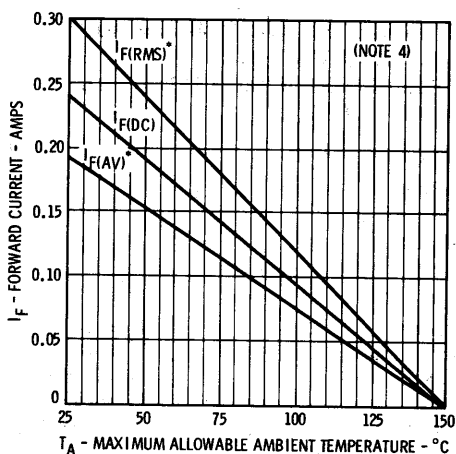
FAIRCHILD THYRISTORS 2N876 THROUGH 2N882

MAXIMUM RATINGS

FORWARD CURRENT VERSUS MAXIMUM ALLOWABLE CASE TEMPERATURE HALF WAVE CONDUCTION*



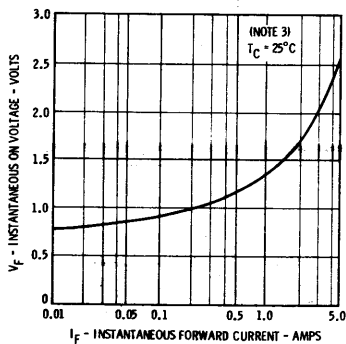
FORWARD CURRENT VERSUS MAXIMUM ALLOWABLE AMBIENT TEMPERATURE HALF WAVE CONDUCTION*



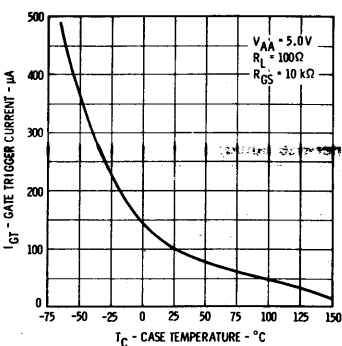
*180° Conduction Angle for Sinusoidal Current Waveform: 50 to 400 Hz.

TYPICAL ELECTRICAL CHARACTERISTICS

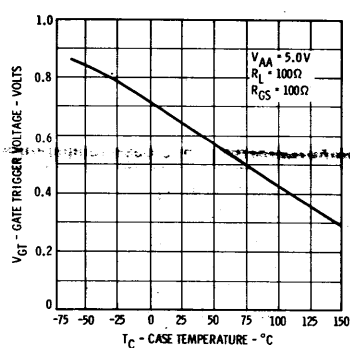
INSTANTANEOUS ON VOLTAGE VERSUS FORWARD CURRENT



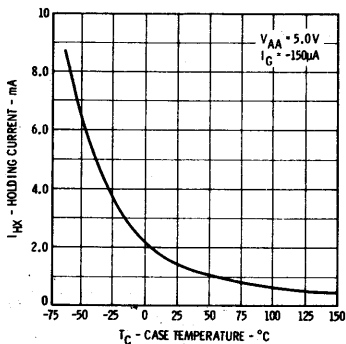
GATE TRIGGER CURRENT VERSUS CASE TEMPERATURE



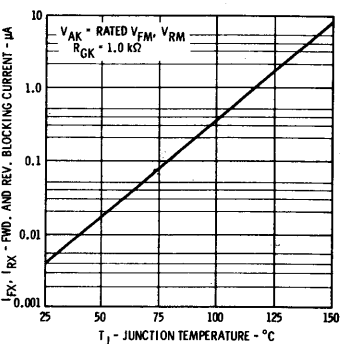
GATE TRIGGER VOLTAGE VERSUS CASE TEMPERATURE



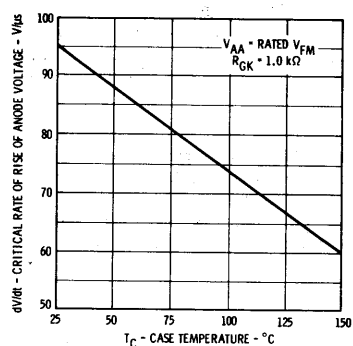
HOLDING CURRENT VERSUS CASE TEMPERATURE



FORWARD AND REVERSE BLOCKING CURRENT VERSUS JUNCTION TEMPERATURE



ALLOWABLE CRITICAL RATE OF RISE OF ANODE VOLTAGE VERSUS CASE TEMPERATURE



2N884 THROUGH 2N890

PNPN SILICON CONTROLLED RECTIFIERS

DIFFUSED SILICON PLANAR* THYRISTORS

- FORWARD CURRENT RATING OF 0.35 AMPS DC AT $T_C = 100^\circ\text{C}$
- BLOCKING VOLTAGE CAPABILITY TO 300 VOLTS
- MAXIMUM GATE TRIGGER CURRENT OF 20 μA AT $T_C = 25^\circ\text{C}$
- RELIABLE PLANAR CONSTRUCTION

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

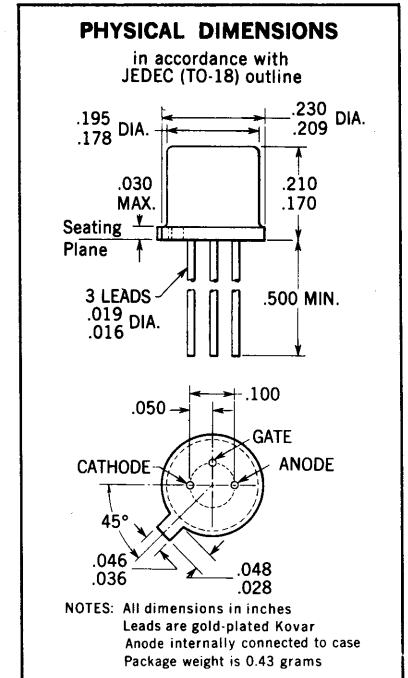
†Storage Temperature	-65°C to +150°C
†Operating Temperature	-65°C to +150°C
†Lead Temperature (Soldering, 10 second time limit)	+230°C

Maximum Currents

RMS Forward Current (180° Conduction Angle) (Note 2)	$T_C = 100^\circ\text{C}$	$I_{F(RMS)}$	430 mA
Continuous Forward Current (Note 2)	$T_A = 25^\circ\text{C}$	$I_{F(DC)}$	300 mA
Average Forward Current (180° Conduction Angle) (Note 2)	$T_C = 100^\circ\text{C}$	$I_{F(AV)}$	350 mA
†Peak Recurrent Forward Current (Repetition rate 60 pps or higher, ≤ 0.01 duty cycle)	$T_A = 25^\circ\text{C}$	I_{FRM}	240 mA
†Surge Current (Rectangular pulse of 0.2 ms duration, peak)	$T_C = 100^\circ\text{C}$	$I_{FM(surge)}$	280 mA
†Peak Forward Gate Current	$T_C = 100^\circ\text{C}$	I_{GFM}	192 mA
			20 Amps

Maximum Voltages ($T_C = -65^\circ\text{C}$ to $+100^\circ\text{C}$)

†Peak Reverse Gate Voltage	V_{GRM}	5.0 Volts*
†DC Forward and Reverse Blocking Voltage	V_{FM}, V_{RM}	2N884 15 Volts 2N885 30 Volts 2N886 60 Volts 2N887 100 Volts 2N888 150 Volts 2N889 200 Volts 2N890 300 Volts



ELECTRICAL CHARACTERISTICS (25°C Case Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
† I_{FX}	Forward Blocking Current		0.004	1.0	μA	$V_{AK} = \text{Rated } V_{FM}, R_{GK} = 1.0 \text{ k}\Omega$
† $I_{FX}(125^\circ\text{C})$	Forward Blocking Current		1.5	20	μA	$V_{AK} = \text{Rated } V_{FM}, R_{GK} = 1.0 \text{ k}\Omega$
† I_{RX}	Reverse Blocking Current		0.004	1.0	μA	$V_{AK} = \text{Rated } V_{RM}, R_{GK} = 1.0 \text{ k}\Omega$
† $I_{RX}(125^\circ\text{C})$	Reverse Blocking Current		1.5	20	μA	$V_{AK} = \text{Rated } V_{RM}, R_{GK} = 1.0 \text{ k}\Omega$
† I_{GR}	Reverse Gate Current (except 2N890)		0.1	10	μA	$V_{GK} = -2.0 \text{ V}, I_A = 0$
† I_{GR}	Reverse Gate Current (2N890 only)		0.1	10	μA	$V_{GK} = -5.0 \text{ V}, I_A = 0$
† I_{GT}	Gate Trigger Current		10	20	μA	$V_{AA} = 5.0 \text{ V}, R_L = 100 \Omega, R_{GS} = 10 \text{ k}\Omega$
† V_{GT}	Gate Trigger Voltage	0.44	0.57	0.60	Volts	$V_{AA} = 5.0 \text{ V}, R_L = 100 \Omega, R_{GS} = 100 \Omega$
† I_{HX}	Holding Current	0.1	0.15	1.0	mA	$V_{AA} = 5.0 \text{ V}, I_G = -50 \mu\text{A}$
† V_F	On Voltage (Note 3)		1.0	1.5	Volts	$I_F = 200 \text{ mA}$
dV/dt	Critical Rate of Rise of Anode Voltage		95		V/ μs	$V_{AA} = \text{Rated } V_{FM}, R_{GK} = 1.0 \text{ k}\Omega$

†JEDEC Registered Values

*Planar is a patented Fairchild process

NOTES:

- (1) These ratings are limiting values above which the reliability of the device may be impaired.
- (2) These ratings give a maximum junction temperature of 150°C with the maximum average power dissipation and a maximum junction to case thermal resistance of 44.5°C/Watt and a junction to ambient thermal resistance of 350°C/Watt.
- (3) Pulse Conditions: Length = 300 μs ; Duty Cycle $\leq 2\%$.
- (4) Ambient temperature derating curves are derived with no external heat sink connected.

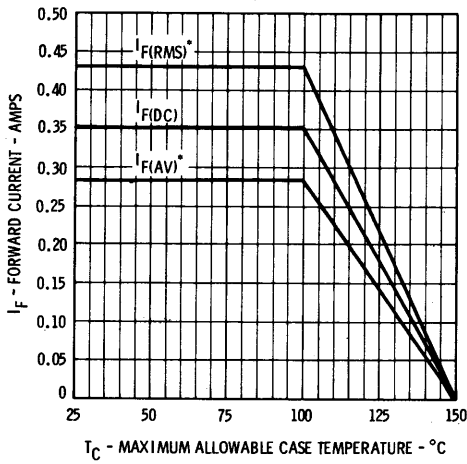
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SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

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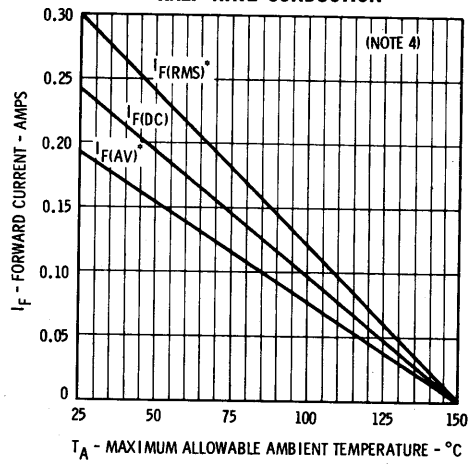
FAIRCHILD THYRISTORS 2N884 THROUGH 2N890

MAXIMUM RATINGS

FORWARD CURRENT VERSUS MAXIMUM ALLOWABLE CASE TEMPERATURE HALF WAVE CONDUCTION*



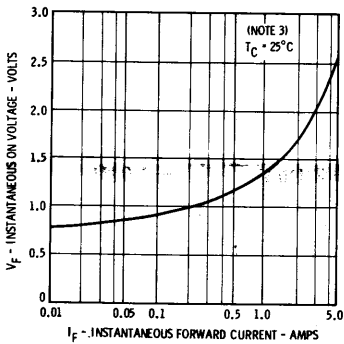
FORWARD CURRENT VERSUS MAXIMUM ALLOWABLE AMBIENT TEMPERATURE HALF WAVE CONDUCTION*



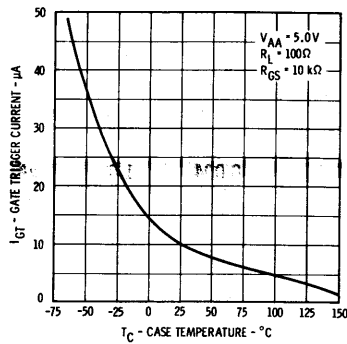
*180° Conduction Angle for Sinusoidal Current Waveform: 50 to 400 Hz.

TYPICAL ELECTRICAL CHARACTERISTICS

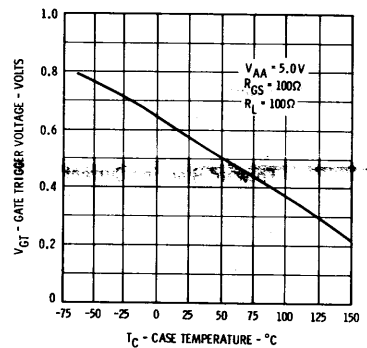
INSTANTANEOUS ON VOLTAGE VERSUS FORWARD CURRENT



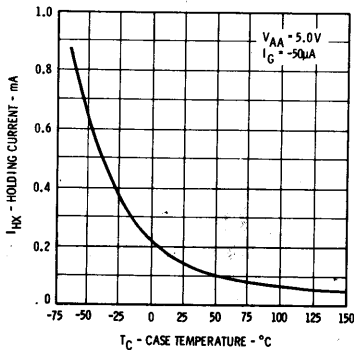
GATE TRIGGER CURRENT VERSUS CASE TEMPERATURE



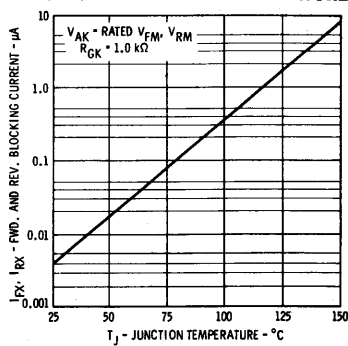
GATE TRIGGER VOLTAGE VERSUS CASE TEMPERATURE



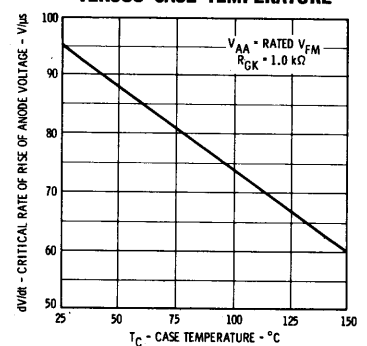
HOLDING CURRENT VERSUS CASE TEMPERATURE



FORWARD AND REVERSE BLOCKING CURRENT VERSUS JUNCTION TEMPERATURE



ALLOWABLE CRITICAL RATE OF RISE OF ANODE VOLTAGE VERSUS CASE TEMPERATURE



2N892 • 2N894 • 2N896 • 2N898 • 2N900

PNP SILICON CONTROLLED RECTIFIERS

DIFFUSED SILICON PLANAR* THYRISTORS

- CHARACTERIZED FOR TURN-OFF CAPABILITY
- FORWARD CURRENT RATING OF 0.3 AMPS AT $T_C = 75^\circ\text{C}$
- MAXIMUM GATE TRIGGER CURRENT OF 50 μA AT $T_C = 25^\circ\text{C}$
- RELIABLE PLANAR CONSTRUCTION

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

†Storage Temperature	-65°C to +150°C
†Operating Temperature	-65°C to +125°C
†Lead Temperature (Soldering, 10 second time limit)	+230°C

Maximum Currents

RMS Forward Current	$T_C = 75^\circ\text{C}$	$I_{F(RMS)}$	300 mA
(180° Conduction Angle) (Note 2)	$T_A = 25^\circ\text{C}$		188 mA
Continuous Forward Current	† $T_C = 75^\circ\text{C}$	$I_{F(DC)}$	250 mA
(Note 2)	$T_A = 25^\circ\text{C}$		145 mA
Average Forward Current	$T_C = 75^\circ\text{C}$	$I_{F(AV)}$	190 mA
(180° Conduction Angle) (Note 2)	$T_A = 25^\circ\text{C}$		120 mA
†Peak Recurrent Forward Current	$T_C = 75^\circ\text{C}$	I_{FRM}	10 Amps
(Repetition rate of 60 pps or higher, ≤ 0.01 duty cycle)			

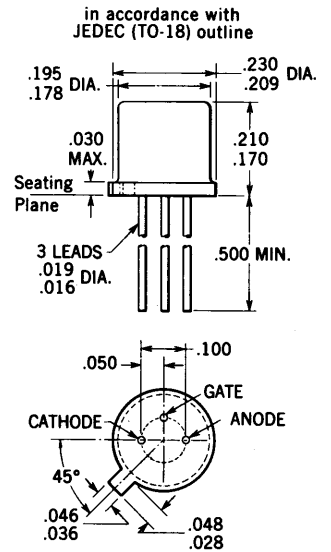
†Surge Current	$T_C = 75^\circ\text{C}$	$I_{FM(surge)}$	20 Amps
(Rectangular pulse of 0.2 ms duration, peak)			

†Peak Forward Gate Current	$T_C = 75^\circ\text{C}$	I_{GFM}	250 mA
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Maximum Voltages ($T_C = -65^\circ\text{C}$ to $+75^\circ\text{C}$)

†Peak Reverse Gate Voltage	V_{GRM}	5.0 Volts
†DC Reverse Blocking Voltage	V_{RM}	15 Volts
†DC Forward Blocking Voltage	V_{FM}	2N892 15 Volts
		2N894 30 Volts
		2N896 60 Volts
		2N898 100 Volts
		2N900 200 Volts

PHYSICAL DIMENSIONS



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Anode internally connected to case
Package weight is 0.43 grams

ELECTRICAL CHARACTERISTICS (25°C Case Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
† I_{RX}	Reverse Blocking Current		0.004	10	μA	$V_{AK} = -15\text{ V}$, $R_{GK} = 1.0\text{ k}\Omega$
† I_{FX}	Forward Blocking Current		0.004	10	μA	$V_{AK} = \text{Rated } V_{FM}$, $R_{GK} = 1.0\text{ k}\Omega$
† $I_{FX}(125^\circ\text{C})$	Forward Blocking Current		2.0	100	μA	$V_{AK} = \text{Rated } V_{FM}$, $R_{GK} = 1.0\text{ k}\Omega$
† I_{GR}	Reverse Gate Current		0.1	10	μA	$V_{GK} = -5.0\text{ V}$, $I_A = 0$
† I_{GT}	Gate Trigger Current		20	50	μA	$V_{AA} = 5.0\text{ V}$, $R_L = 100\ \Omega$, $R_{GS} = 10\text{ k}\Omega$
† V_{GT}	Gate Trigger Voltage	0.4	0.64	0.7	Volts	$V_{AA} = 5.0\text{ V}$, $R_L = 100\ \Omega$, $R_{GS} = 100\ \Omega$
† I_{GQ}	Gate Turn-Off Current			2.0	mA	$I_F = 4.0\text{ mA}$
† V_{GQ}	Gate Turn-Off Voltage			1.5	Volts	$I_F = 4.0\text{ mA}$
† V_F	On Voltage (Note 3)		1.05	2.0	Volts	$I_F = 250\text{ mA}$
† V_F	On Voltage (Note 3)		0.75	1.0	Volts	$I_F = 4.0\text{ mA}$
† t_{gq}	Gate Controlled Turn-Off Time (Note 4)			15	μs	$I_F = 4.0\text{ mA}$, $V_{GQ} = 4.0\text{ V}$

†JEDEC Registered Values

*Planar is a patented Fairchild process

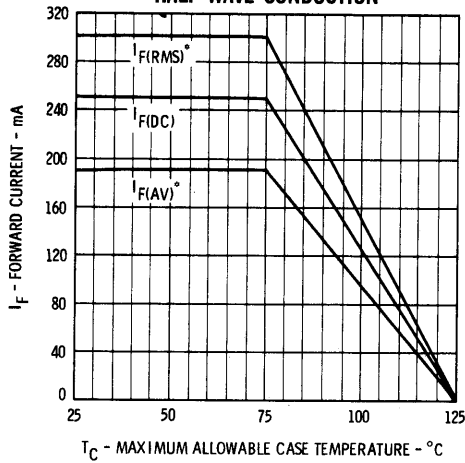
NOTES:

- (1) These ratings are limiting values above which the reliability of the device may be impaired.
- (2) These ratings give a maximum junction temperature of 125°C with the maximum average power dissipation and a maximum junction to case thermal resistance of 44.5°C/Watt and a junction to ambient thermal resistance of 350°C/Watt.
- (3) Pulse Conditions: Length = 300 μs ; Duty Cycle $\leq 2\%$.
- (4) Measured in test circuit shown on page 2.
- (5) Ambient temperature derating curves are derived with no external heat sink connected.

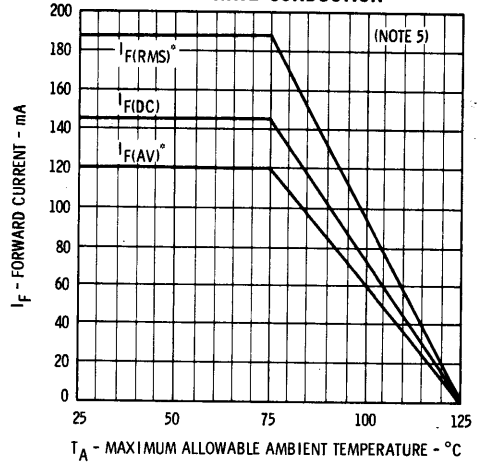
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MAXIMUM RATINGS

FORWARD CURRENT VERSUS MAXIMUM ALLOWABLE CASE TEMPERATURE HALF WAVE CONDUCTION*



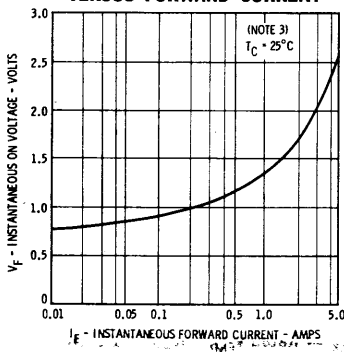
FORWARD CURRENT VERSUS MAXIMUM ALLOWABLE AMBIENT TEMPERATURE HALF WAVE CONDUCTION*



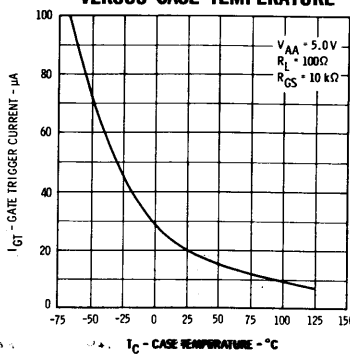
*180° Conduction Angle for Sinusoidal Current Waveform: 50 to 400 Hz.

TYPICAL ELECTRICAL CHARACTERISTICS

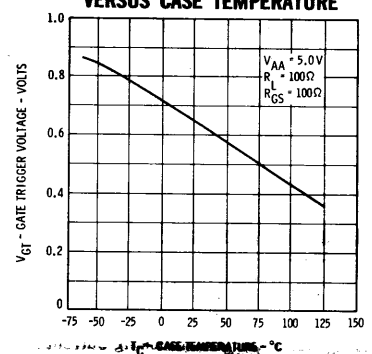
INSTANTANEOUS ON VOLTAGE VERSUS FORWARD CURRENT



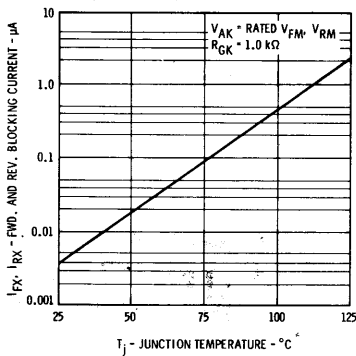
GATE TRIGGER CURRENT VERSUS CASE TEMPERATURE



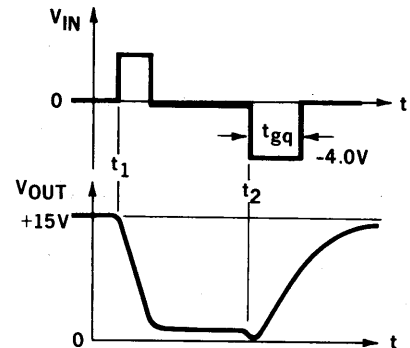
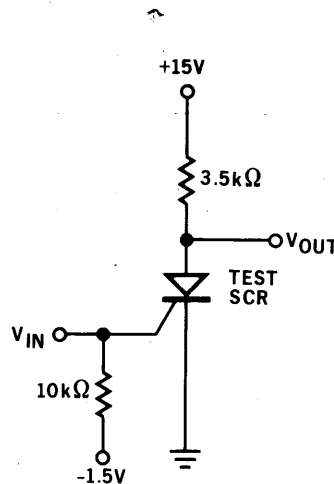
GATE TRIGGER VOLTAGE VERSUS CASE TEMPERATURE



FORWARD AND REVERSE BLOCKING CURRENT VERSUS JUNCTION TEMPERATURE



GATE CONTROLLED TURN-OFF TIME TEST CIRCUIT



Time t_{gq} is the maximum negative pulse duration required to turn-off all devices.

2N948 THROUGH 2N951

PNPN SILICON CONTROLLED RECTIFIERS

DIFFUSED SILICON PLANAR* THYRISTORS

- FORWARD CURRENT RATING OF 0.26 AMPS DC AT $T_C = 125^\circ\text{C}$
- BLOCKING VOLTAGE CAPABILITY TO 200 VOLTS
- MAXIMUM GATE TRIGGER CURRENT OF $20\ \mu\text{A}$ AT $T_C = 25^\circ\text{C}$
- RELIABLE PLANAR CONSTRUCTION

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

†Storage Temperature	-65°C to +150°C
†Operating Temperature	-65°C to +150°C
†Lead Temperature (Soldering, 10 second time limit)	+230°C

Maximum Currents and Power

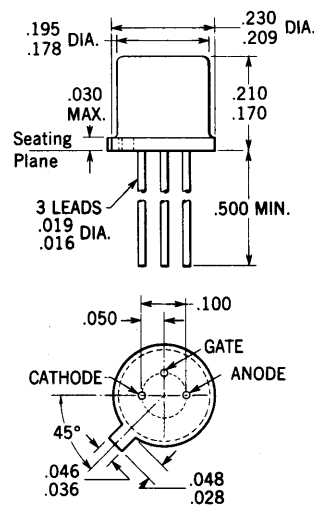
RMS Forward Current	$T_C = 125^\circ\text{C}$	$I_{F(RMS)}$	314 mA
(180° Conduction Angle) (Note 2)	$T_A = 25^\circ\text{C}$		236 mA
Continuous Forward Current	$T_C = 125^\circ\text{C}$	$I_{F(DC)}$	260 mA
(Note 2)	$T_A = 25^\circ\text{C}$		180 mA
Average Forward Current	$T_C = 75^\circ\text{C}$	$I_{F(AV)}$	200 mA
(180° Conduction Angle) (Note 2)	$T_A = 25^\circ\text{C}$		150 mA
†Peak Recurrent Forward Current	$T_C = 110^\circ\text{C}$	I_{FRM}	660 mA
†Surge Current	$T_C = 75^\circ\text{C}$	$I_{FM(surge)}$	1.0 Amp
(½ cycle sine wave, 60 Hz, peak)			
†Peak Forward Gate Current	$T_C = 125^\circ\text{C}$	I_{GFM}	100 mA
†Peak Gate Power Dissipation	$T_C = 125^\circ\text{C}$	P_{GM}	200 mW
†Average Gate Power Dissipation	$T_C = 125^\circ\text{C}$	$P_{G(AV)}$	20 mW

Maximum Voltages ($T_C = +25^\circ\text{C}$ to $+125^\circ\text{C}$)

†Peak Reverse Gate Voltage	V_{GRM}	5.0 Volts
†DC Forward and Reverse Blocking Voltages	V_{FM}, V_{RM}	2N948 30 Volts 2N949 60 Volts 2N950 100 Volts 2N951 200 Volts

PHYSICAL DIMENSIONS

in accordance with JEDEC (TO-18) outline



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Anode internally connected to case
Package weight is 0.43 grams

ELECTRICAL CHARACTERISTICS (25°C Case Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	TYP.	MAX.	UNITS	TEST CONDITIONS
I_{FX}	Forward Blocking Current	0.004	1.0	μA	$V_{AK} = \text{Rated } V_{FM}, I_G = -20\ \mu\text{A}$
$I_{FX}(125^\circ\text{C})$	Forward Blocking Current	1.5	20	μA	$V_{AK} = \text{Rated } V_{FM}, I_G = -20\ \mu\text{A}$
I_{RO}	Reverse Blocking Current	0.004	1.0	μA	$V_{AK} = \text{Rated } V_{RM}, I_G = 0$
$I_{RO}(125^\circ\text{C})$	Reverse Blocking Current	1.5	20	μA	$V_{AK} = \text{Rated } V_{RM}, I_G = 0$
I_{GR}	Reverse Gate Current	0.001	10	mA	$V_{GK} = -5.0\ \text{V}, I_A = 0$
I_{GT}	Gate Trigger Current	10	20	μA	$V_{AA} = 10\ \text{V}, R_L = 100\ \Omega$
I_{VGT}	Gate Trigger Voltage	0.59	1.0	Volts	$V_{AA} = 10\ \text{V}, R_L = 100\ \Omega$
I_{HO}	Holding Current	0.14	1.0	mA	$R_L = 1.0\ \text{k}\Omega, I_G = 0$
V_F	On Voltage (Note 3)	1.0	2.0	Volts	$I_F = 200\ \text{mA}$
V_F	On Voltage (Note 3)	0.75	1.2	Volts	$I_F = 10\ \text{mA}$
dV/dt	Critical Rate of Rise of Anode Voltage	95		V/ μs	$V_{AA} = \text{Rated } V_{FM}, R_{GK} = 1.0\ \text{k}\Omega$

†JEDEC Registered Values

*Planar is a patented Fairchild process

NOTES:

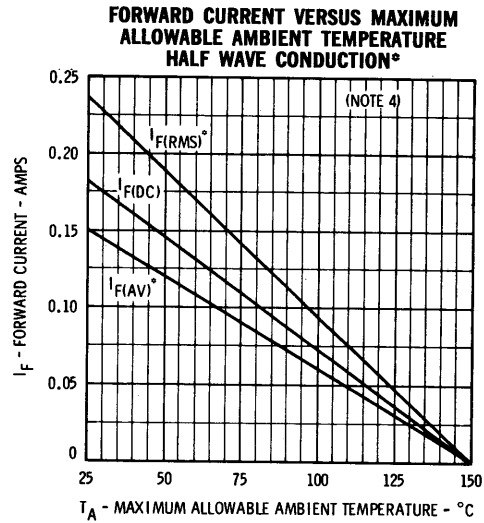
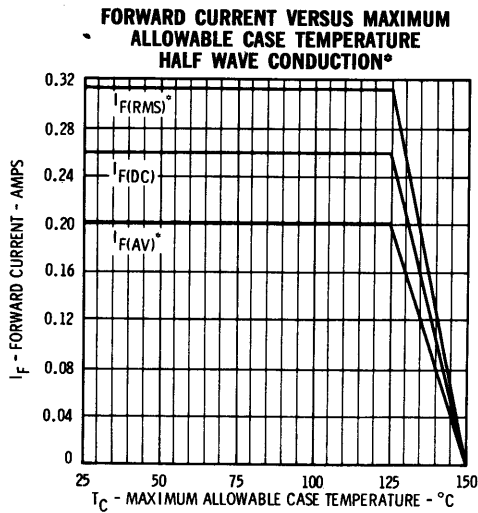
- (1) These ratings are limiting values above which the reliability of the device may be impaired.
- (2) These ratings give a maximum junction temperature of 150°C with the maximum average power dissipation and a maximum junction to case thermal resistance of $44.5^\circ\text{C}/\text{Watt}$ and a junction to ambient thermal resistance of $350^\circ\text{C}/\text{Watt}$.
- (3) Pulse Conditions: Length = 300 μs ; Duty Cycle $\leq 2\%$.
- (4) Ambient temperature derating curves are derived with no external heat sink connected.

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313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD THYRISTORS 2N948 THROUGH 2N951

MAXIMUM RATINGS



*180° Conduction Angle for Sinusoidal Current Waveform: 50 to 400 Hz.

TYPICAL ELECTRICAL CHARACTERISTICS

