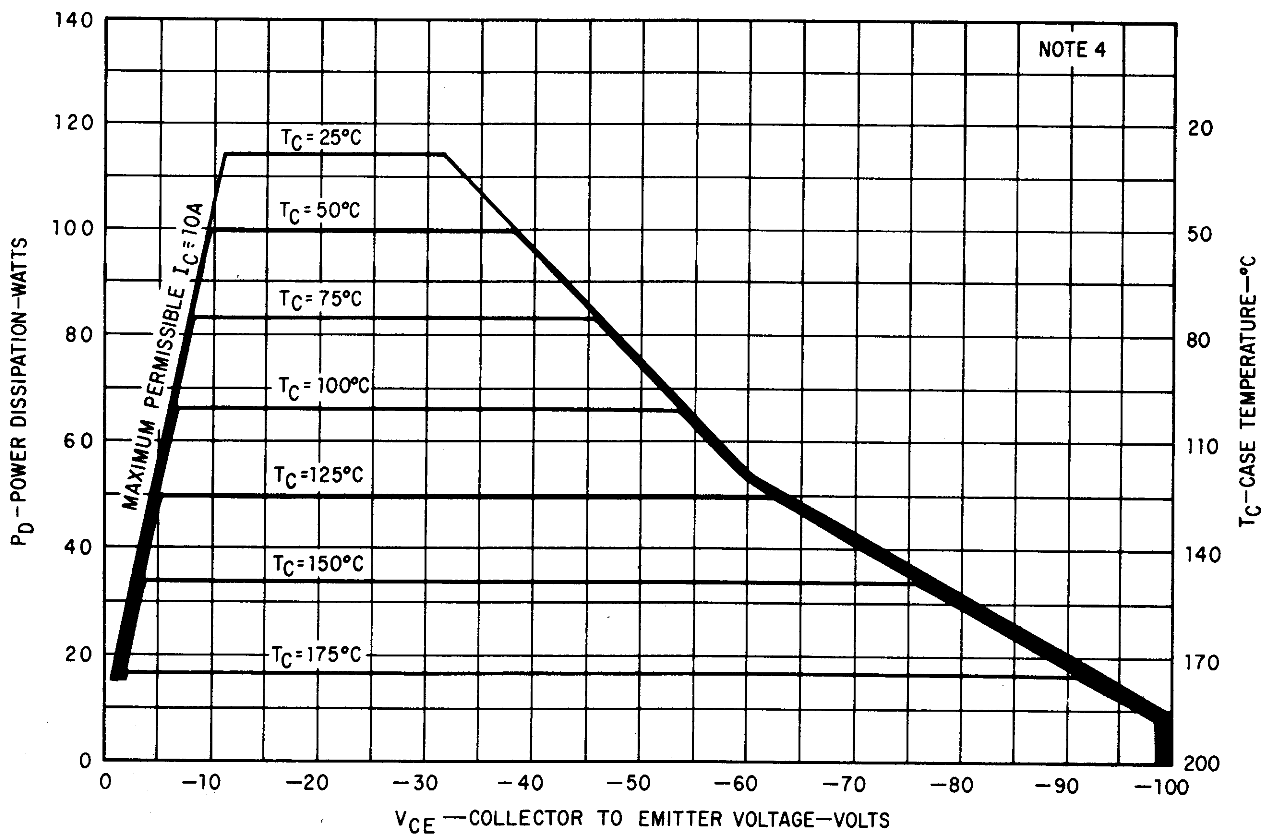
ELECTRICAL CHARACTERISTICS (25°C Case Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N5290 MIN.	2N5290 MAX.	2N5291 MIN.	2N5291 MAX.	UNITS	TEST CONDITIONS	
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 3)		−1.8		−1.8	Volts	$I_C = 5.0$ A	$I_B = 0.5$ A
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 3)		−2.2		−2.2	Volts	$I_C = 10$ A	$I_B = 1.0$ A
$V_{BE(on)}$	Pulsed Base Emitter "ON" Voltage (Note 3)		−1.8		−1.8	Volts	$I_C = 5.0$ A	$V_{CE} = -5.0$ V
I_{CES}	Collector Cutoff Current		1.0		1.0	μA	$V_{CE} = -80$ V	$V_{BE} = 0$
I_{EBO}	Emitter Cutoff Current		1.0		1.0	μA	$I_C = 0$	$V_{EB} = -4.0$ V
I_{CEX}(150°C)	Collector Reverse Current		500		500	μA	$V_{CE} = -80$ V	$V_{EB} = -2.0$ V
C_{cb}	Collector to Base Capacitance		500		500	pF	$I_E = 0$	$V_{CB} = -10$ V
I_{CES}	Collector Cutoff Current		1.0		1.0	mA	$V_{CE} = -100$ V	$V_{BE} = 0$
I_{EBO}	Emitter Cutoff Current		1.0		1.0	mA	$I_C = 0$	$V_{EB} = -5.5$ V
I_{CEO}	Collector Cutoff Current		50		50	μA	$I_B = 0$	$V_{CE} = -60$ V
h_{fe}	Small Signal Current Gain (f = 1.0 kHz)	20		50			$I_C = 200$ mA	$V_{CE} = -5.0$ V

NOTES:
(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
(2) This rating refers to a high current point where collector to emitter voltage is lowest.
(3) Pulse Conditions: length = 300 μs; duty cycle = 1%.
(4) Contact factory for maximum permissible power under pulsed or reverse biased operating conditions.

MAXIMUM PERMISSIBLE DC FORWARD BIASED POWER DISSIPATION

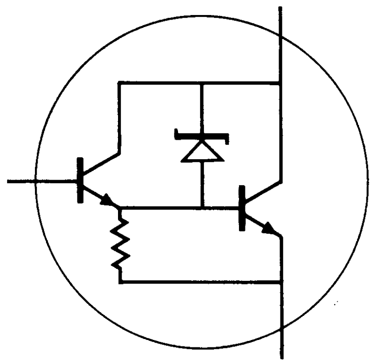


2N5425 • 2N5426

NPN POWER INDUCTIVE LOAD DRIVERS

DIFFUSED SILICON PLANAR* EPITAXIAL TRANSISTORS

GENERAL DESCRIPTION — The 2N5425 and 2N5426 are monolithic darlington transistors with integrated base to emitter resistors added for stability. The output devices are of the discrete emitter technology for high forward biased safe operating area. Clamping is achieved by means of a hybrid zener diode connected from collector to base on the output device. These transistors are housed in a special BeO based TO-9 package for higher power dissipation capability.



A SELF-CLAMPED MONOLITHIC DARLINGTON INDUCTIVE LOAD DRIVER
SPECIFICALLY DESIGNED TO DRIVE:

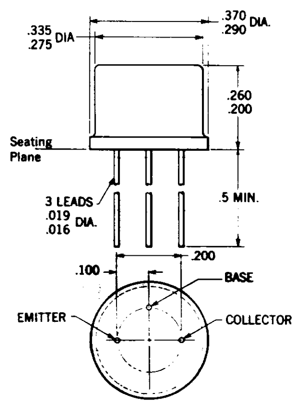
- **Solenoid Hammers**
- **Relays**
- **Stepping Motors**

WITH THE FOLLOWING SPECIAL FEATURES:

- **Integrated Circuit Compatibility — 5 mA Drives 5 Amps**
- **Zener Clamping — At 60 Volts Minimum**
- **Base-Emitter Termination — R_{BE} 100 Ohms Nominal**
- **Special Low R_{TH} Beryllia Based TO-9**

- **HIGH CURRENT . . . . 5 AMPS**
- **HIGH VOLTAGE . . . . > 60 VOLTS**
- **HIGH GAIN . . . . > 1000 AT 5 A.**
- **HIGH POWER . . . . 32.5 WATTS AT 70°C**
- **FAST SWITCHING . . . . < 2.0 μs AT 5 A.**
- **LOW SATURATION VOLTAGE . . . < 2.5 V AT 5 A.**

PHYSICAL DIMENSIONS
In Accordance With
JEDEC (TO-9) Outline



NOTES: All dimensions in inches
Leads are tin-plated Kovar
All leads electrically isolated from case

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures		
Storage Temperature Range		−65°C to +200°C
Operating Junction Temperature		+200°C
Lead Temperature (Soldering, 60 seconds time limit)		+300°C
Maximum Power Dissipation		
Total Dissipation at 70°C Case Temperature, $V_{CE} = 25$ V (See Safe Area Curve)		32.5 Watts
Maximum Voltages and Currents		
V_{CBO}	Collector to Base Voltage	60 Volts
V_{CEO}	Collector to Emitter Voltage	60 Volts
V_{EBO}	Emitter to Base Voltage	7.0 Volts
I_C	Collector Current	5.0 Amps
I_B	Base Current	100 mAmps

Electrical Characteristics on Page 2.

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (25°C Case Temperature unless otherwise noted)

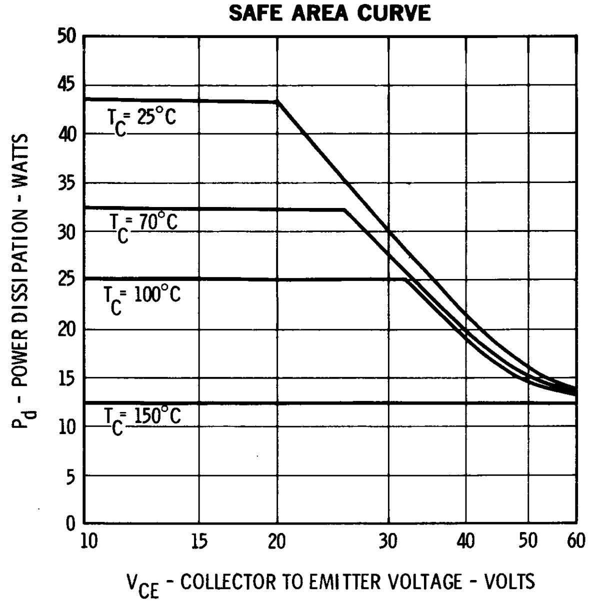
SYMBOL	CHARACTERISTIC	2N5426 MIN.	2N5426 TYP.	2N5426 MAX.	2N5425 MIN.	2N5425 TYP.	2N5425 MAX.	UNITS	TEST CONDITIONS
$V_{CEO(sus)}$	Collector to Emitter Sustaining Voltage	60			60			Volts	$I_C = 50$ mA, $I_B = 0$
BV_{EBO}	Emitter to Base Breakdown Voltage	7.0			7.0			Volts	$I_C = 0$, $I_E = 100\ \mu A$
BV_{CEX}	Collector to Emitter Breakdown Voltage ($T_C = 70°C$) (Fig. 1)	60			60			Volts	$I_C = 5.0$ A, $V_{BE} = \leq 0.3$ V
I_{CBO}	Collector Cutoff Current			1.0			1.0	μA	$V_{CB} = 50$ V, $I_E = 0$
I_{EBO}	Emitter Cutoff Current			1.0			1.0	μA	$V_{EB} = 5.0$ V, $I_C = 0$
I_{CEO}	Collector Leakage Current			10			10	μA	$V_{CE} = 50$ V, $I_B = 0$
I_{CES}	Collector Leakage Current ($T_C = 150°C$)			1.0			1.0	mA	$V_{CE} = 50$ V, $V_{BB} = 0$
t_{on}	Turn On Time (Fig. 2)			300			300	ns	$I_C = 5$ A, $I_B = 10$ mA
t_{off}	Turn Off Time (Fig. 2)			2000			2000	ns	$I_C = 5$ A, $I_{B1} = I_{B2} = 10$ mA
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Notes 2 & 3)	1.4	1.8	2.2				Volts	$I_C = 5.0$ A, $I_B = 5.0$ mA
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Notes 2 & 3)					2.2	2.5	Volts	$I_C = 5.0$ A, $I_B = 10$ mA
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Notes 2 & 3)	1.5		2.5				Volts	$I_C = 5.0$ A, $I_B = 5.0$ mA
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Notes 2 & 3)						3.0	Volts	$I_C = 5.0$ A, $I_B = 10$ mA
h_{fe}	High Frequency Current Gain (f = 20 MHz)	2.5	20		2.5	20			$I_C = 500$ mA, $V_{CE} = 10$ V
C_{cb}	Collector to Base Capacitance		8	15			15	pF	$V_{CB} = 10$ V, $I_E = 0$
C_{eb}	Emitter to Base Capacitance		25	50			50	pF	$V_{EB} = 0.5$ V, $I_C = 0$

NOTES:

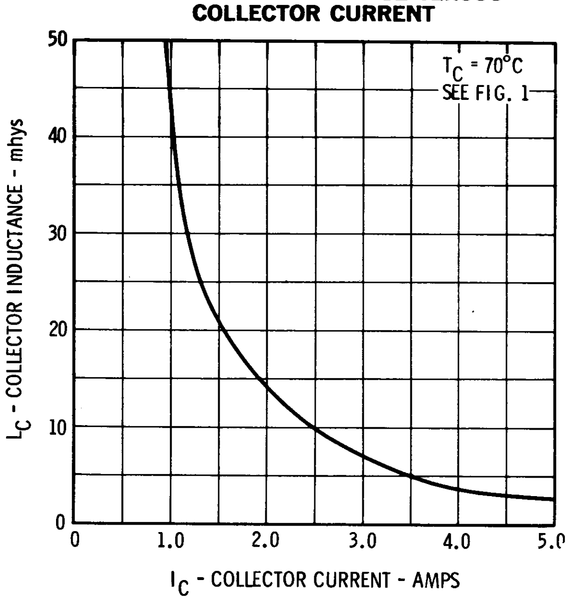
(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
(2) Point of measurement: ¼" from header.
(3) Pulse Conditions: length = 300 μs; duty cycle = 1%.

MAXIMUM PERMISSIBLE POWER DISSIPATION

SAFE AREA CURVE

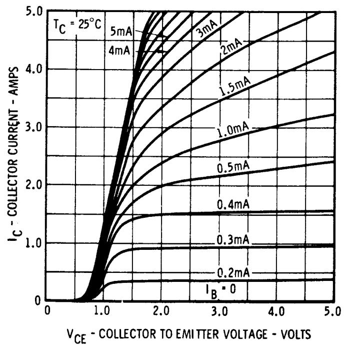


COLLECTOR INDUCTANCE VERSUS COLLECTOR CURRENT

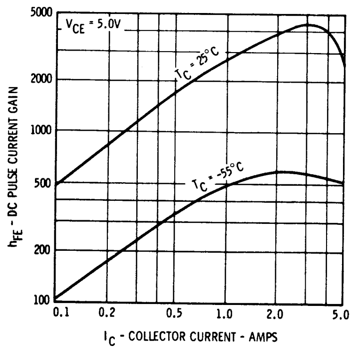


TYPICAL ELECTRICAL CHARACTERISTICS
2N5425 • 2N5426

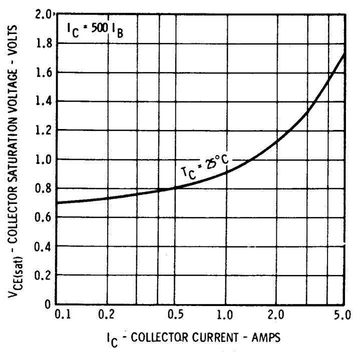
COLLECTOR CHARACTERISTICS SATURATION REGION



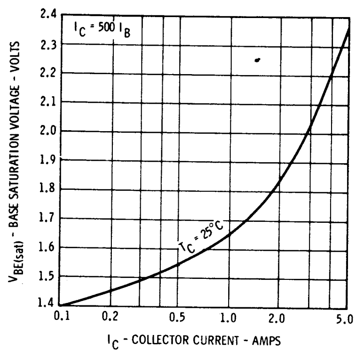
DC PULSE CURRENT GAIN VERSUS COLLECTOR CURRENT



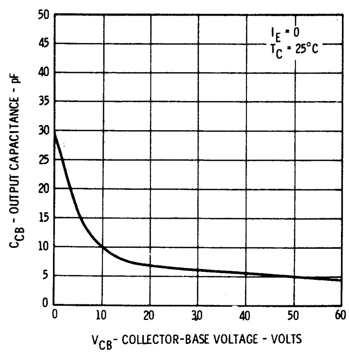
COLLECTOR SATURATION VOLTAGE VERSUS PULSED COLLECTOR CURRENT



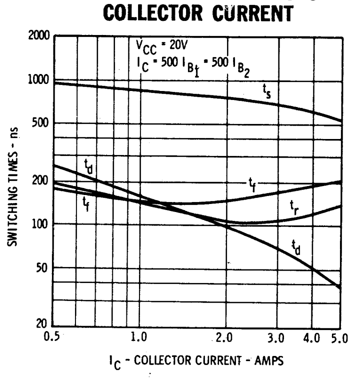
BASE SATURATION VOLTAGE VERSUS PULSED COLLECTOR CURRENT



OUTPUT CAPACITANCE VERSUS COLLECTOR-BASE VOLTAGE

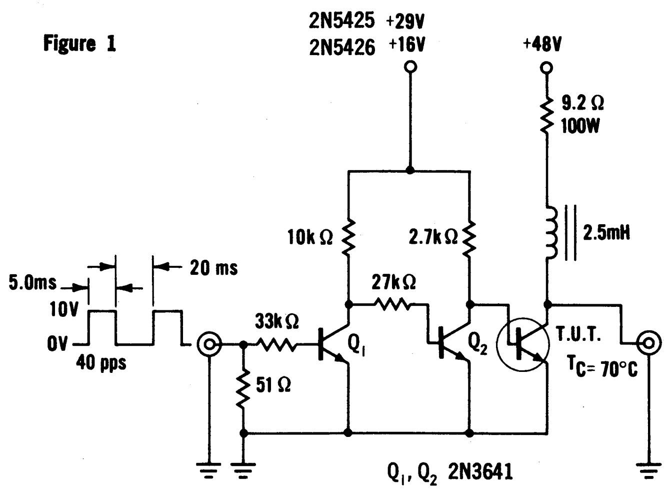


SWITCHING TIMES VERSUS COLLECTOR CURRENT



INDUCTIVE TEST CIRCUIT

Figure 1



SWITCHING TIME TEST CIRCUIT

Figure 2