

2N5527 2N5531

NPN SILICON POWER TRANSISTORS RADIATION RESISTANT

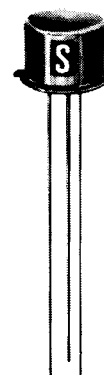
5 AMPERES

FEATURES

MEDIUM POWER
RADIATION EXPOSURE LEVEL TO 5×10^{14} nvt
TOTAL NEUTRON FLUX GREATER THAN 10 KEV

APPLICATIONS

POWER AMPLIFIER
RADIATION ENVIRONMENTS
ULTRA HIGH FREQUENCY



TO-5

ABSOLUTE MAXIMUM RATINGS

		<u>2N5527</u>	<u>2N5531</u>
V_{CB0}	COLLECTOR-BASE VOLTAGE	60 V	90 V
V_{CE0}	COLLECTOR-EMITTER VOLTAGE	40 V	75 V
V_{EB0}	EMITTER-BASE VOLTAGE	3 V	3 V
I_C	CONTINUOUS COLLECTOR CURRENT	5 A	5 A
I_B	CONTINUOUS BASE CURRENT	1 A	1 A
T_J	OPERATING JUNCTION TEMPERATURE	_____ -65°C to +200°C _____	
T_{stg}	STORAGE TEMPERATURE	_____ -65°C to +200°C _____	
$R_{\theta JC}$	THERMAL RESISTANCE, JUNCTION TO CASE	35°C/W	
P_D	POWER DISSIPATION (25°C)	5 W	

8-83-2R

RADIATION RESISTANT NPN SILICON POWER TRANSISTORS

2N5527 2N5531

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

CHARACTERISTICS	SYMBOL	MIN.	MAX.	UNITS
COLLECTOR-EMITTER SUSTAINING VOLTAGE ⁽¹⁾ ($I_C = 50\text{ mA}$)	$V_{CE(sus)}$	2N5527 40		V
		2N5531 75		V
($I_C = 50\text{ mA}$, NOTE 2)		2N5527 40		V
		2N5531 75		V
COLLECTOR-CUTOFF CURRENT ($V_{CE} = 30\text{V}$, $V_{BE} = 0$, $T_C = 100^\circ\text{C}$)	I_{CEX}		1.0	mA
COLLECTOR-CUTOFF CURRENT ($V_{CB} = \text{RATED}$)	I_{CBO}		1.0	mA
			1.0	mA
COLLECTOR-CUTOFF CURRENT ($V_{CB} = 30\text{V}$)	I_{CBO}		0.1	mA
			1.0	mA
COLLECTOR-CUTOFF CURRENT ($V_{CE} = \text{RATED}$)	I_{CEO}		50	mA
EMITTER CUTOFF CURRENT ($V_{EB} = 3.0\text{V}$)	I_{EBO}		1.0	mA
			1.0	mA
EMITTER FLOATING POTENTIAL ($V_{CB} = \text{RATED}$, $I_E = 0$)	V_{EBF}		1.0	V
DC CURRENT GAIN ⁽¹⁾ ($V_{CE} 5.0\text{V}$, $I_C = 0.5\text{A}$)	h_{FE}	2N5527 40	300	
($V_{CE} 5.0\text{V}$, $I_C = 0.5\text{A}$)		2N5531 25	300	
($V_{CE} 5.0\text{V}$, $I_C = 3.0\text{A}$)		2N5527 40	200	
($V_{CE} 5.0\text{V}$, $I_C = 3.0\text{A}$)		2N5531 30	150	
($V_{CE} 5.0\text{V}$, $I_C = 5.0\text{A}$)		2N5527 25		
($V_{CE} 5.0\text{V}$, $I_C = 5.0\text{A}$)		2N5531 20		
($V_{CE} 5.0\text{V}$, $I_C = 3.0\text{A}$ NOTE 2)		2N5527 15		
($V_{CE} 5.0\text{V}$, $I_C = 3.0\text{A}$ NOTE 2)		2N5531 7.0		
COLLECTOR-EMITTER SATURATION VOLTAGE ⁽¹⁾ ($I_C = 3.0\text{A}$, $I_B = 0.3\text{A}$)	$V_{CE(sat)}$	2N5527	1.25	V
($I_C = 3.0\text{A}$, $I_B = 0.5\text{A}$)		2N5531	1.25	V
($I_C = 5.0\text{A}$, $I_B = 0.2\text{A}$)		2N5527	5.0	V
($I_C = 5.0\text{A}$, $I_B = 0.25\text{A}$)		2N5531	5.0	V
($I_C = 3.0\text{A}$, $I_B = 0.3\text{A}$, NOTE 2)		2N5527	2.0	V
($I_C = 3.0\text{A}$, $I_B = 0.5\text{A}$, NOTE 2)		2N5531	3.0	V
BASE-EMITTER SATURATION VOLTAGE ⁽¹⁾ ($I_C = 3.0\text{A}$, $I_B = 0.3\text{A}$)	$V_{BE(sat)}$	2N5527	1.5	V
($I_C = 3.0\text{A}$, $I_B = 0.5\text{A}$)		2N5531	1.5	V
BASE-EMITTER VOLTAGE ($V_{CE} = 5.0\text{V}$, $I_C = 3.0\text{A}$)	V_{BE}		1.5	V
MAGNITUDE OF SMALL SIGNAL GAIN ($V_{CE} = 28\text{V}$, $I_C = 0.5\text{A}$, $f = 25\text{ MHz}$)	$ h_{fe} $	8.0		
SMALL SIGNAL GAIN ($V_{CB} = 5.0\text{V}$, $I_C = 0.5\text{A}$, $f = 1.0\text{ KHz}$)	h_{fe}	2N5527 20		
		2N5531 15		
OUTPUT CAPACITANCE ($V_{CB} = 30\text{V}$, $f = 1.0\text{ MHz}$)	C_{obo}		75	pF
PROMPT PRIMARY PHOTO CURRENT ($\dot{\gamma} = 1 \times 10^{19}\text{ R/sec}$, $\epsilon \geq 1.0\text{ MeV}$, $V_{CB} = 10\text{V}$)	I_{ppc}		500	mA(PK)

Note 1: Pulsed 300 μsec , 1.8 Duty Cycle

Note 2: After exposure, $1 \times 10^{14}\text{ nvt}$, FLUX $\geq 10\text{ KEV}$

RADIATION RESISTANT NPN SILICON POWER TRANSISTORS

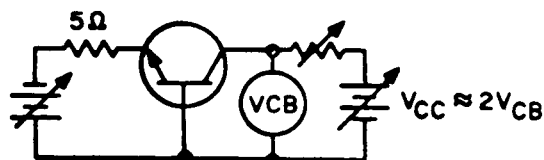
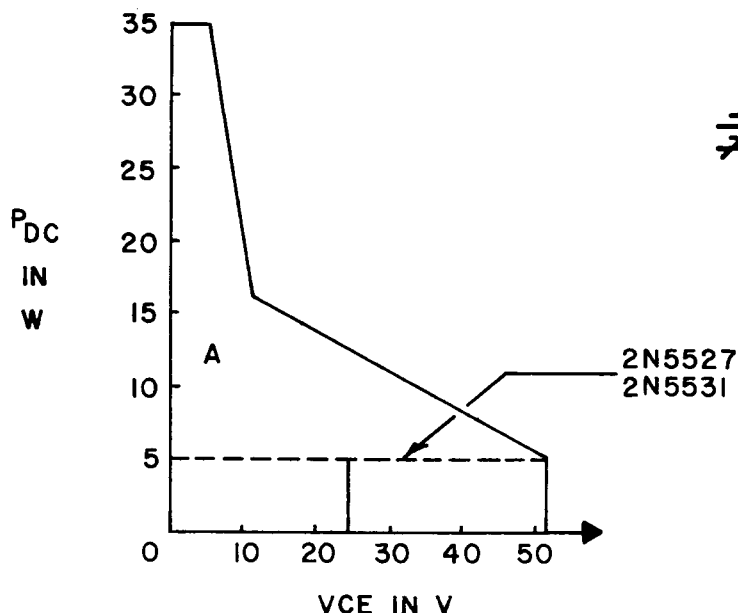
2N5527 2N5531

SAFE OPERATING AREA (SOAR) CONTINUOUS DC OPERATION

SOAR VALUES

TYPE NUMBER	V1 V	V2 V
2N5527	30	60
2N5531	65	90

- Conditions:
1. $T_J = T_{CASE} + \Theta_{J-C} P_{DC} \leq 200^\circ\text{C}$
 2. $P_{DC} = P_{DC}$ max rating for specified transistor type
 3. $P_{DC} = P_{DC} = f(V_{CE})$ Area A
 4. $V_{CE} = 0.8V_1$ rating for specified transistor type

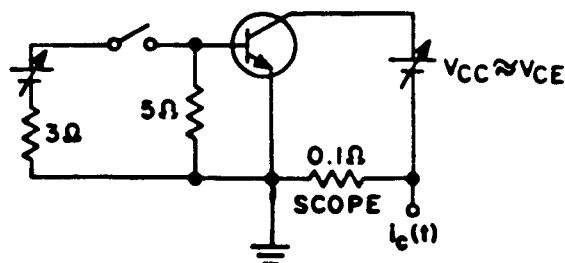
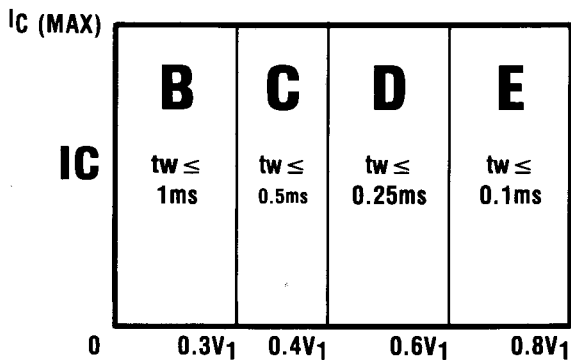


PULSED OPERATION

- Conditions:
1. $T_J = T_{CASE} + \Theta_{J-C} P_{avg} \leq 200^\circ\text{C}$
 2. $P_{avg} = \frac{1}{2\text{ms}} \int_0^{2\text{ms}} i_c v_{ce} dt \leq \text{the allowed DC}$

power dissipation for a V_{CE} equal to the highest v_{ce} applied to the transistor

3. Operation in the active region should be limited to a maximum pulse width of $t_w = 1$ ms for Area B, $t_w = 0.5$ ms for Area C, $t_w = 0.25$ ms for Area D, and $t_w = 0.10$ ms for Area E. $t_r \leq 20 \mu\text{s}$ and $t_f \leq 20 \mu\text{s}$ for Areas B-E.

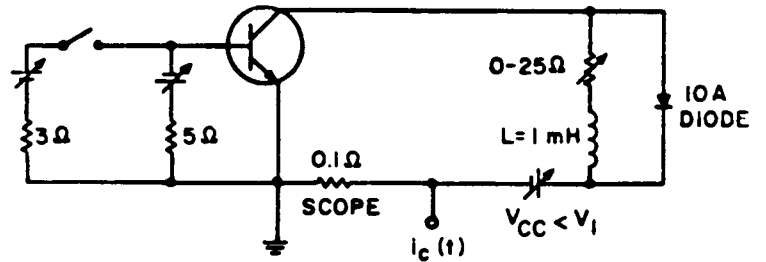
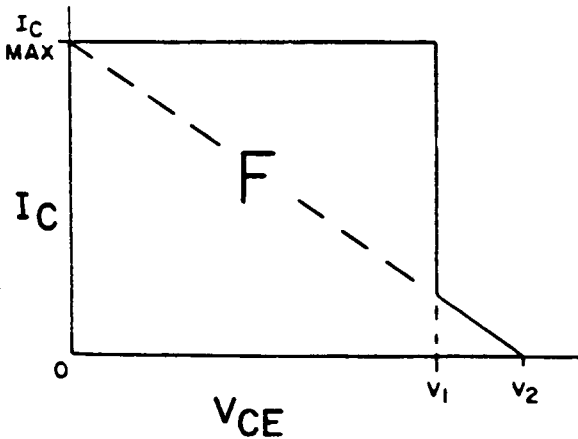


RESISTIVE AND CLAMPED INDUCTIVE SWITCHING

(Switching from saturation to cutoff)

Conditions:

1. $T_J = T_C + \Theta_{J-C} P_{avg} \leq 200^\circ\text{C}$
2. $P_{avg} = \frac{1}{2\text{ms}} \int_0^{2\text{ms}} i_c v_{ce} dt \leq \text{PDC max.}$
3. For the resistive loadline, $L = 0$ and $V_{CC} = V_2$
4. $t_r \leq 2\mu\text{s}$, $t_f \leq 2\mu\text{s}$ in Area F

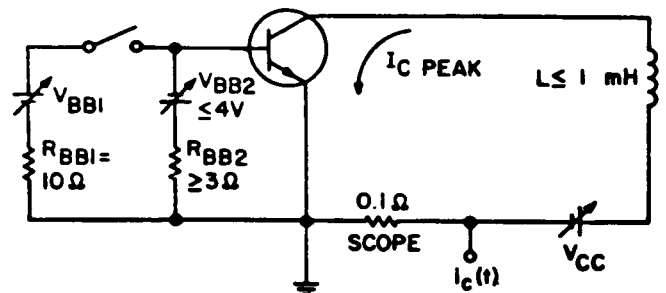
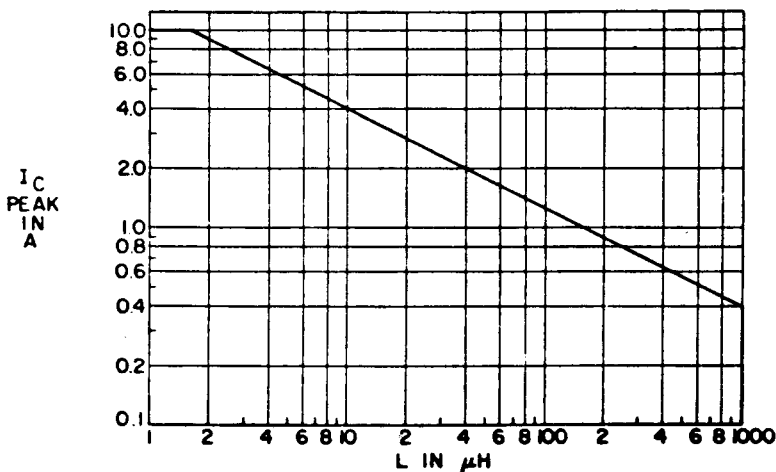


UNCLAMPED SWITCHING

(Switching from saturation to cutoff)

Conditions:

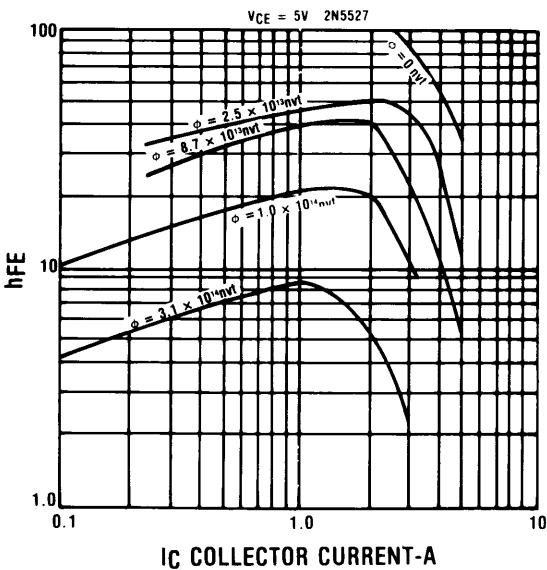
1. $T_J = T_C + \Theta_{J-C} P_{avg} \leq 200^\circ\text{C}$
2. $P_{avg} = \frac{1}{2\text{ms}} \int_0^{2\text{ms}} i_c v_{ce} dt \leq \text{PDC max.}$
3. $I_C \text{ peak} \leq I_C \text{ max rating for specified transistor type}$
4. $\frac{1}{2} L I_C^2 \leq 80\mu\text{Ws}$



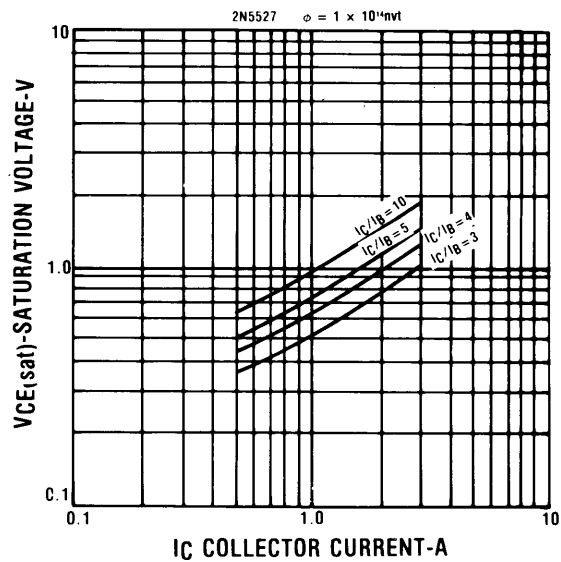
RADIATION RESISTANT NPN SILICON POWER TRANSISTORS

2N5527 2N5531

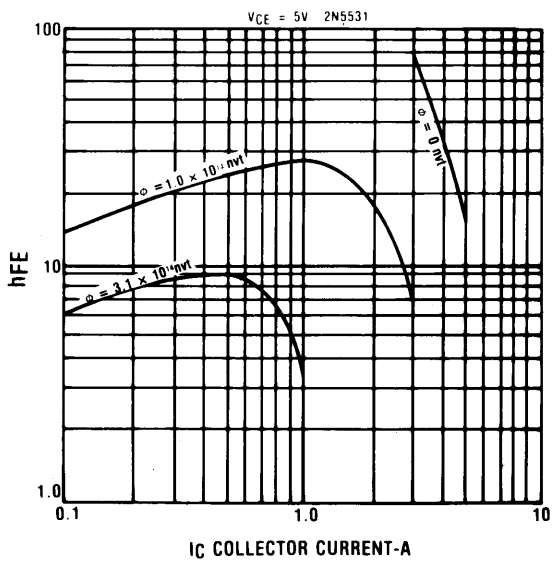
TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO



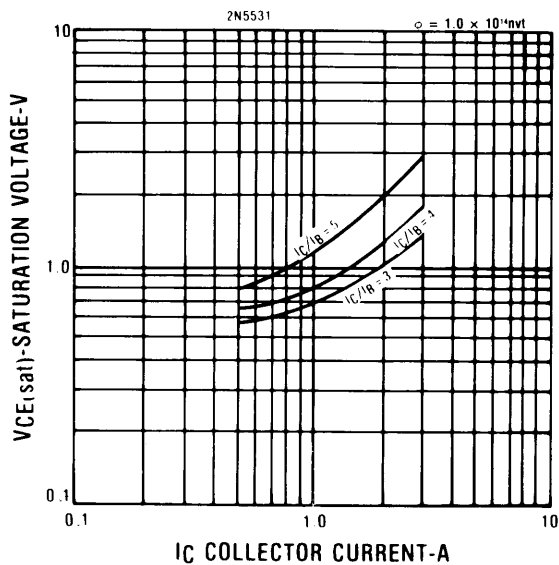
TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE



TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO



TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE



RADIATION RESISTANT NPN SILICON POWER TRANSISTORS

2N5529 2N5530 2N5533 2N5534

NPN SILICON POWER TRANSISTORS RADIATION RESISTANT

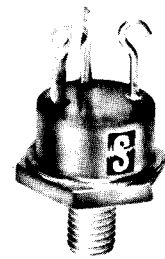
10 AMPERES

FEATURES

HIGH POWER
RADIATION EXPOSURE LEVEL TO 5×10^{14} nvt
TOTAL NEUTRON FLUX GREATER THAN 10 KEV

APPLICATIONS

POWER AMPLIFIER
RADIATION ENVIRONMENTS
ULTRA HIGH FREQUENCY



TO-61

*All leads isolated from case

ABSOLUTE MAXIMUM RATINGS

		2N5529 2N5530*	2N5533 2N5534*
V_{CB0}	COLLECTOR-BASE VOLTAGE	60 V	90 V
V_{CE0}	COLLECTOR-EMITTER VOLTAGE	40 V	75 V
V_{EB0}	EMITTER-BASE VOLTAGE	3 V	3 V
I_C	CONTINUOUS COLLECTOR CURRENT	10 A	10 A
I_B	CONTINUOUS BASE CURRENT	4 A	4 A
T_J	OPERATING JUNCTION TEMPERATURE	_____ -65°C to +200°C _____	
T_{stg}	STORAGE TEMPERATURE	_____ -65°C to +200°C _____	
$R_{\theta JC}$	THERMAL RESISTANCE, JUNCTION TO CASE	5°C/W	
P_D	POWER DISSIPATION (25°C)	35 W	

8-83-2R

RADIATION RESISTANT NPN SILICON POWER TRANSISTORS

2N5529 2N5530 2N5533 2N5534

ELECTRICAL CHARACTERISTICS (T_C = 25°C UNLESS OTHERWISE NOTED)

CHARACTERISTICS	SYMBOL	MIN.	MAX.	UNITS
COLLECTOR-EMITTER SUSTAINING VOLTAGE ⁽¹⁾ (I _C = 50 mA) 2N5529, 2N5530 2N5533, 2N5534 (I _C = 50 mA, NOTE 2) 2N5529, 2N5530 2N5533, 2N5534	V _{CE0(sus)}	40 75 40 75		V V V V
COLLECTOR-CUTOFF CURRENT (V _{CE} = 30V, V _{BE} = 0, T _C = 100°C)	I _{CEX}		1.0	mA
COLLECTOR-CUTOFF CURRENT (V _{CB} = RATED) (V _{CB} = RATED, NOTE 2)	I _{CBO}		1.0 1.0	mA mA
COLLECTOR-CUTOFF CURRENT (V _{CB} = 30V) (V _{CB} = 30V, NOTE 2)	I _{CBO}		0.1 1.0	mA mA
COLLECTOR-CUTOFF CURRENT (V _{CE} = RATED)	I _{CEO}		50	mA
EMITTER CUTOFF CURRENT (V _{EB} = 3.0V) (V _{EB} = 3.0V, NOTE 2)	I _{EBO}		1.0 1.0	mA mA
EMITTER FLOATING POTENTIAL (V _{CB} = RATED, I _E = 0)	V _{EBF}		1.0	V
DC CURRENT GAIN ⁽¹⁾ (V _{CE} 5.0V, I _C = 0.5A) 2N5529, 2N5530 (V _{CE} 5.0V, I _C = 0.5A) 2N5533, 2N5534 (V _{CE} 5.0V, I _C = 3.0A) 2N5529, 2N5530 (V _{CE} 5.0V, I _C = 3.0A) 2N5533, 2N5534 (V _{CE} 5.0V, I _C = 5.0A) 2N5529, 2N5530 (V _{CE} 5.0V, I _C = 5.0A) 2N5533, 2N5534 (V _{CE} 2.0V, I _C = 10A) 2.5 (V _{CE} 5.0V, I _C = 3.0A NOTE 2) 2N5529, 2N5530 (V _{CE} 5.0V, I _C = 3.0A NOTE 2) 2N5533, 2N5534	h _{FE}	40 25 40 30 25 20 2.5 15 7.0	300 300 200 150	
COLLECTOR-EMITTER SATURATION VOLTAGE ⁽¹⁾ (I _C = 3.0A, I _B = 0.3A) 2N5529, 2N5530 (I _C = 0.5A, I _B = 4.0A) 2N5533, 2N5534 (I _C = 10A, I _B = 4.0A) (I _C = 3.0A, I _B = 0.3A, NOTE 2) 2N5529, 2N5530 (I _C = 3.0A, I _B = 0.5A, NOTE 2) 2N5533, 2N5534	V _{CE(sat)}		1.25 1.25 2.0 2.0 3.0	V V V V V
BASE-EMITTER SATURATION VOLTAGE ⁽¹⁾ (I _C = 3.0A, I _B = 0.3A) 2N5529, 2N5530 (I _C = 3.0A, I _B = 0.5A) 2N5533, 2N5534	V _{BE(sat)}		1.5 1.5	V V
BASE-EMITTER VOLTAGE (V _{CE} = 5.0V, I _C = 3.0A) (V _{CE} = 5.0V, I _C = 5.0A)	V _{BE}		1.5 3.0	V V
MAGNITUDE OF SMALL SIGNAL GAIN (V _{CE} = 28V, I _C = 0.5A, f = 25 MHz)	[h _{fe}]	8.0		
SMALL SIGNAL GAIN (V _{CE} = 5.0V, I _C = 3.0A, f = 1.0 KHz) 2N5529, 2N5530 2N5533, 2N5534	h _{fe}	20 15		
OUTPUT CAPACITANCE (V _{CB} = 30V, f = 1.0 MHz)	C _{obo}		75	pF

Note 1: Pulsed 300 μsec, 1.8% Duty Cycle

Note 2: After exposure 1 × 10¹⁴ nvt, FLUX ≥ 10 KEV

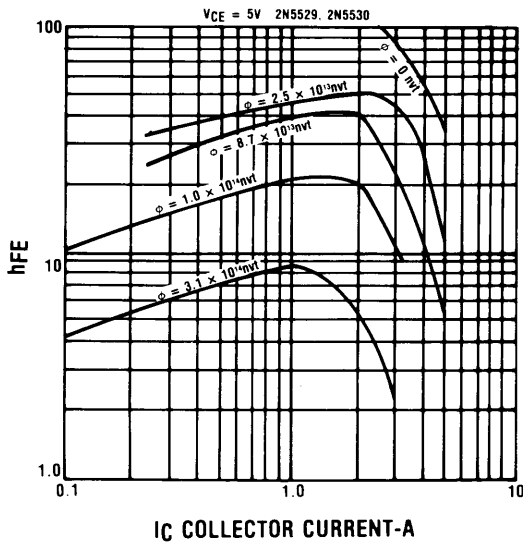
RADIATION RESISTANT NPN SILICON POWER TRANSISTORS

2N5529 2N5530 2N5533 2N5534

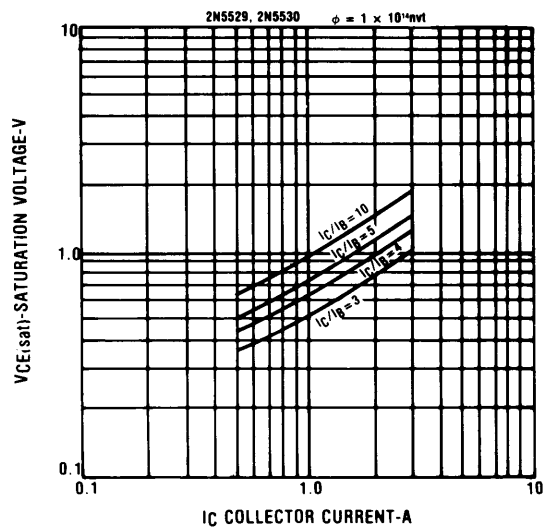
ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

CHARACTERISTICS	SYMBOL	MIN.	MAX.	UNITS
PROMPT PRIMARY PHOTOCURRENT ($\dot{\gamma} = 1 \times 10^9$ R/sec, $\epsilon \geq 1\text{Mev}$, $V_{CB} = 10\text{V}$)	I_{ppc}		500	mA(PK)

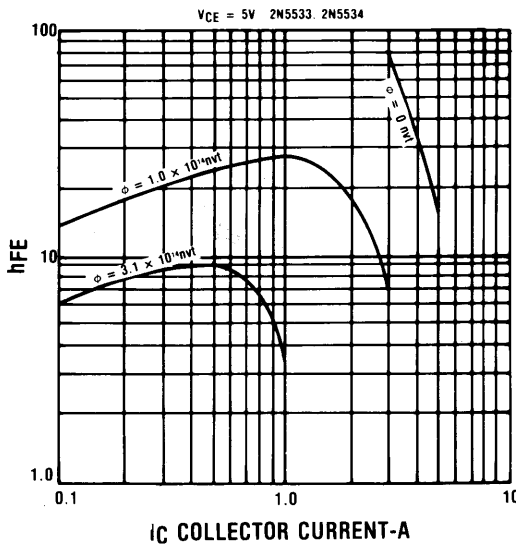
TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO



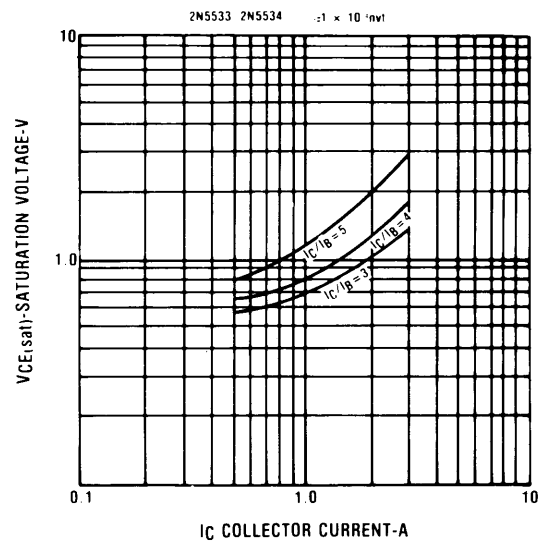
TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE



TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO



TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE



RADIATION RESISTANT NPN SILICON POWER TRANSISTORS

2N5529 2N5530 2N5533 2N5534

SAFE OPERATING AREA (SOAR) INFORMATION

The Safe Operating Area (SOAR) principle is a method of specifying the exact transistor to use in an amplifier, switching or DC application. SOAR defines the region which encloses all of the points representing simultaneous values of the collector current and the collector-to-emitter voltage which a transistor can safely handle under specified conditions for base current, time, junction temperature and average power dissipation. With transistors specified under the Solitron SOAR technique, secondary breakdown is virtually eliminated.

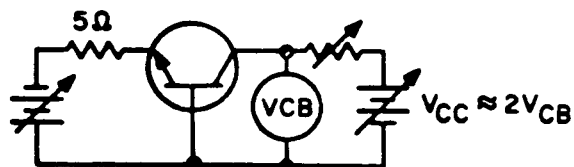
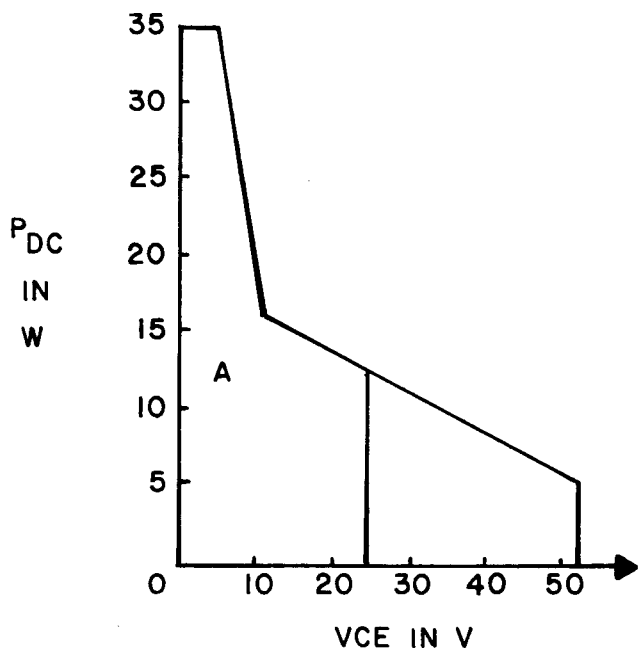
The suggested test circuits are shown for each type of SOAR operation. Any other thermally stable circuit may also be used as long as the SOAR conditions and maximum ratings are observed.

SOAR VALUES

TYPE NUMBER	V1 V	V2 V
2N5530	30	60
2N5534	65	90

CONTINUOUS DC OPERATION

- Conditions:
1. $T_J = T_{CASE} + \Theta_{J-C} P_{DC} \leq 200^\circ C$
 2. $P_{DC} \leq P_{DC \text{ max rating for specified transistor type}}$
 3. $P_{DC} \leq P_{DC} = f(V_{CE}) \text{ Area A}$
 4. $V_{CE} \leq 24V$ (2N5529, 2N5530)
52V (2N5533, 2N5534)



RADIATION RESISTANT NPN SILICON POWER TRANSISTORS

2N5529 2N5530 2N5533 2N5534

PULSED OPERATION

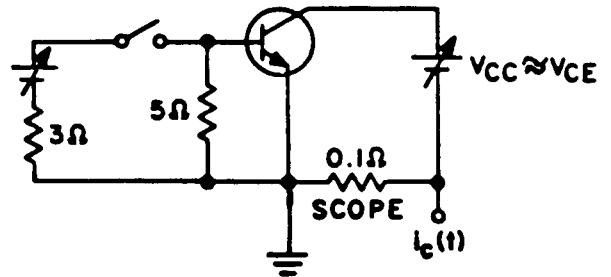
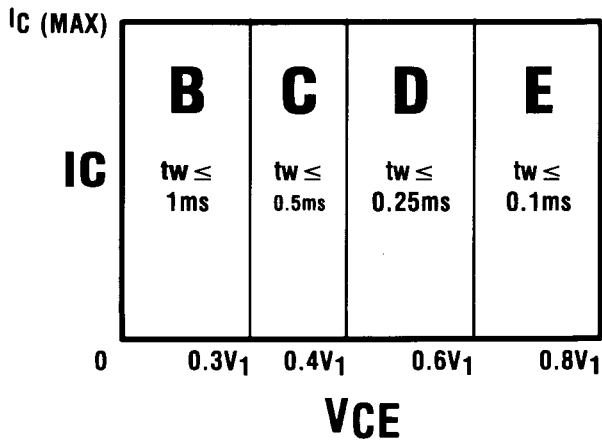
Conditions:

1. $T_J = T_{CASE} + \Theta_{J-C} P_{avg} \leq 200^\circ C$

2. $P_{avg} = \frac{1}{2ms} \int_0^{2ms} i_c v_{ce} dt \leq \text{the allowed DC}$

power dissipation for a V_{CE} equal to the highest v_{ce} applied to the transistor

3. Operation in the active region should be limited to a maximum pulse width of $t_w = 1 \text{ ms}$ for Area B, $t_w = 0.5 \text{ ms}$ for Area C, $t_w = 0.25 \text{ ms}$ for Area D, and $t_w = 0.10 \text{ ms}$ for Area E. $t_r \leq 20 \mu s$ and $t_f \leq 20 \mu s$ for Areas B-E.



RESISTIVE AND CLAMPED INDUCTIVE SWITCHING

(Switching from saturation to cutoff)

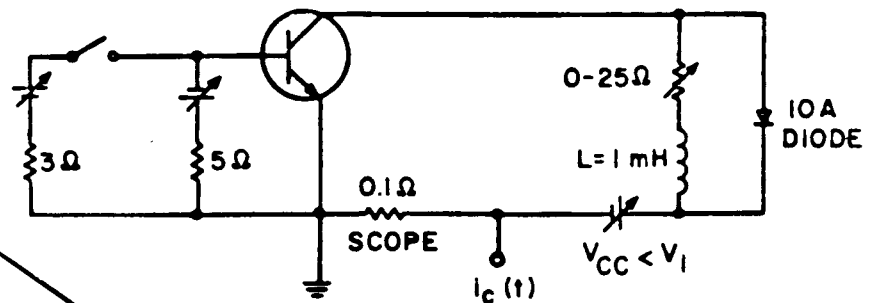
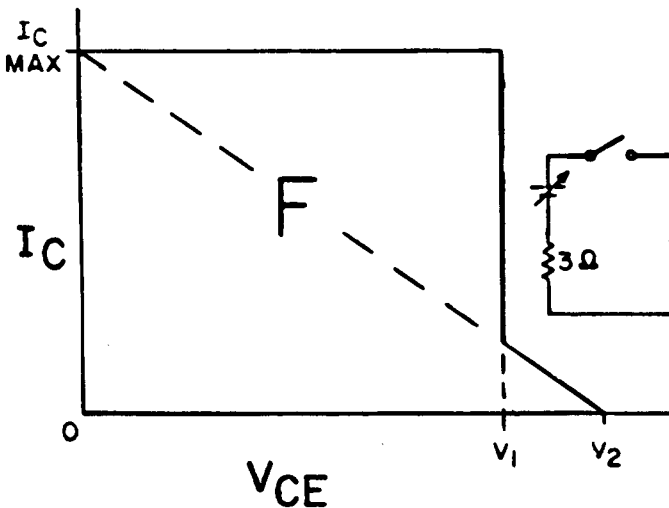
Conditions:

1. $T_J = T_C + \Theta_{J-C} P_{avg} \leq 200^\circ C$

2. $P_{avg} = \frac{1}{2ms} \int_0^{2ms} i_c v_{ce} dt \leq \text{PDC max.}$

3. For the resistive loadline, $L = 0$ and $V_{CC} = V_2$

4. $t_r \leq 2 \mu s$, $t_f \leq 2 \mu s$ in Area F



RADIATION RESISTANT NPN SILICON POWER TRANSISTORS

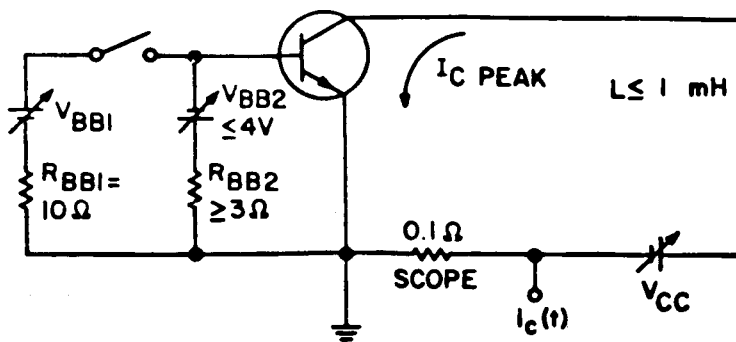
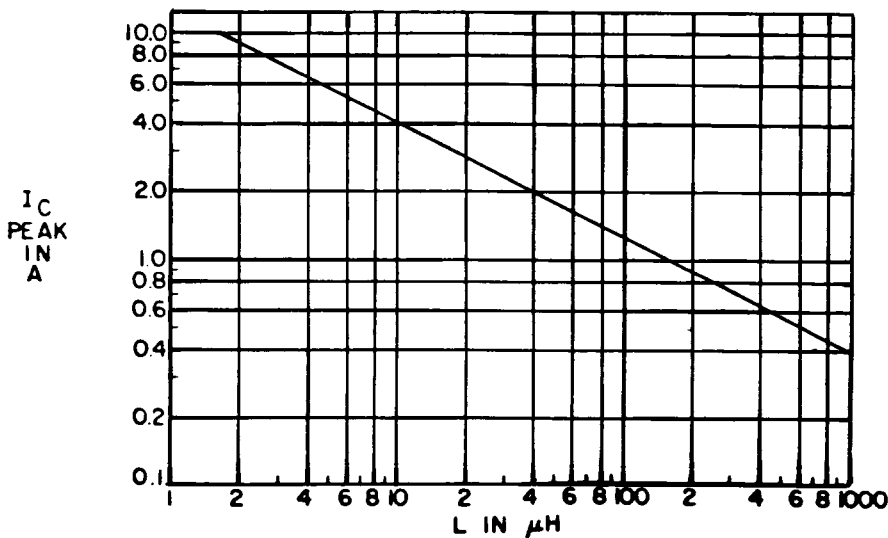
2N5529 2N5530 2N5533 2N5534

UNCLAMPED SWITCHING

(Switching from saturation to cutoff)

Conditions:

1. $T_J = T_C + \Theta_{J-C} P_{avg} \leq 200^\circ\text{C}$
2. $P_{avg} = \frac{1}{2\text{ms}} \int_0^{2\text{ms}} i_c v_{ce} dt \leq P_{DC \text{ max.}}$
3. $I_C \text{ peak} \leq I_C \text{ max rating for specified transistor type}$
4. $\frac{1}{2} I_C^2 \leq 80 \mu\text{Ws}$



2N5535 2N5536 2N5537 2N5538

NPN SILICON POWER TRANSISTORS RADIATION RESISTANT

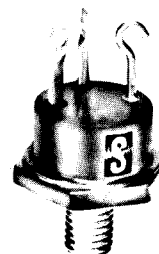
20 AMPERES

FEATURES

HIGH POWER
RADIATION EXPOSURE LEVEL TO 5×10^{14} nvt
TOTAL NEUTRON FLUX GREATER THAN 10 KEV

APPLICATIONS

POWER AMPLIFIER
RADIATION ENVIRONMENTS
ULTRA HIGH FREQUENCY



TO-18

*All leads isolated from case

ABSOLUTE MAXIMUM RATINGS

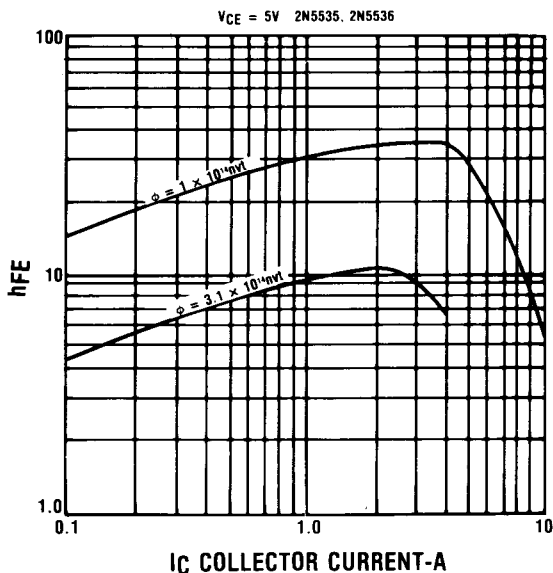
		2N5535 2N5536*	2N5537 2N5538*
V_{CB0}	COLLECTOR-BASE VOLTAGE	60 V	90 V
V_{CE0}	COLLECTOR-EMITTER VOLTAGE	50 V	75 V
V_{EB0}	EMITTER-BASE VOLTAGE	3 V	3 V
I_C	CONTINUOUS COLLECTOR CURRENT	20 A	20 A
I_B	CONTINUOUS BASE CURRENT	8 A	.8 A
T_J	OPERATING JUNCTION TEMPERATURE	_____ -65°C to +200°C _____	
T_{stg}	STORAGE TEMPERATURE	_____ -65°C to +200°C _____	
$R_{\theta JC}$	THERMAL RESISTANCE, JUNCTION TO CASE	3.5°C/W	
P_D	POWER DISSIPATION (25°C)	50 W	

8-83-3R

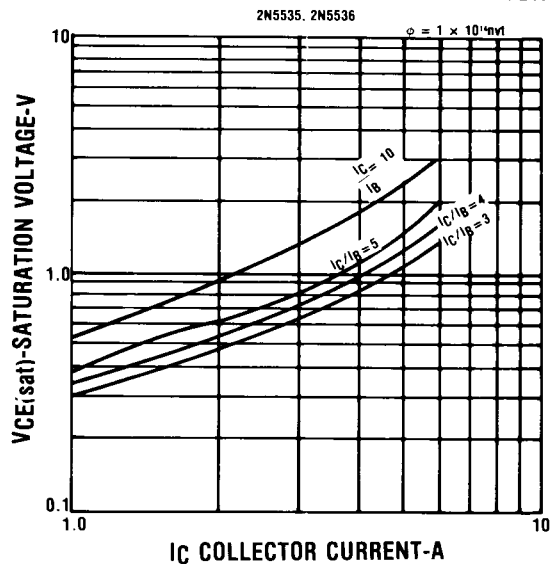
RADIATION RESISTANT NPN SILICON POWER TRANSISTORS

2N5535 2N5536 2N5537 2N5538

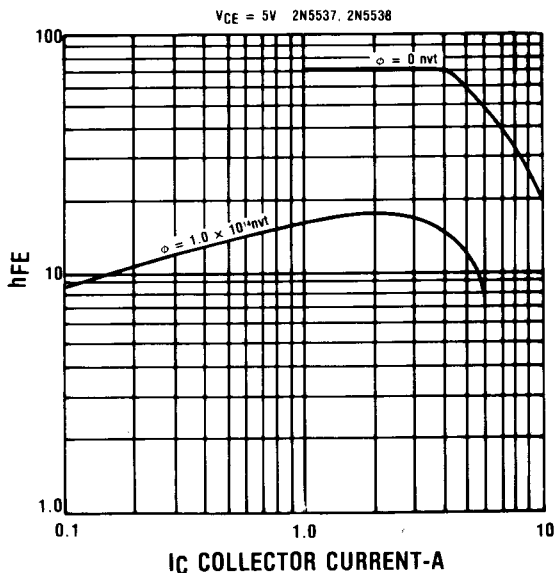
TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO



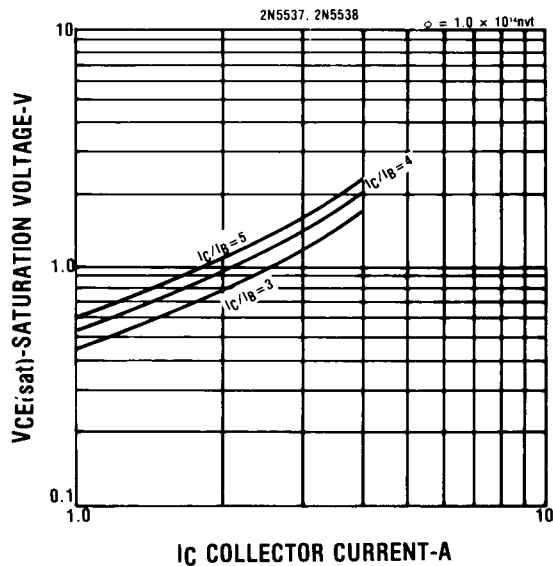
TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE



TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO



TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE



RADIATION RESISTANT NPN SILICON POWER TRANSISTORS

2N5535 2N5536 2N5537 2N5538

SAFE OPERATING AREA (SOAR) INFORMATION

The Safe Operating Area (SOAR) principle is a method of specifying the exact transistor to use in an amplifier, switching or DC application. SOAR defines the region which encloses all of the points representing simultaneous values of the collector current and the collector-to-emitter voltage which a transistor can safely handle under specified conditions for base current, time, junction temperature and average power dissipation. With transistors specified under the Solitron SOAR technique, secondary breakdown is virtually eliminated.

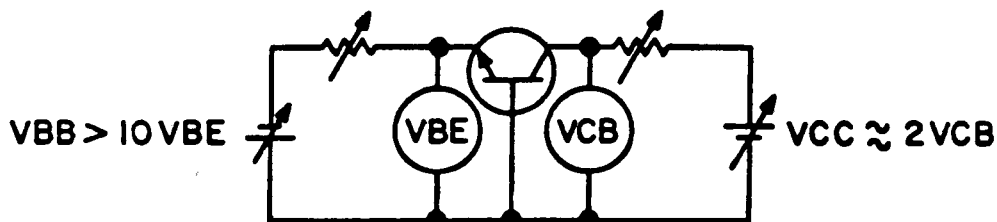
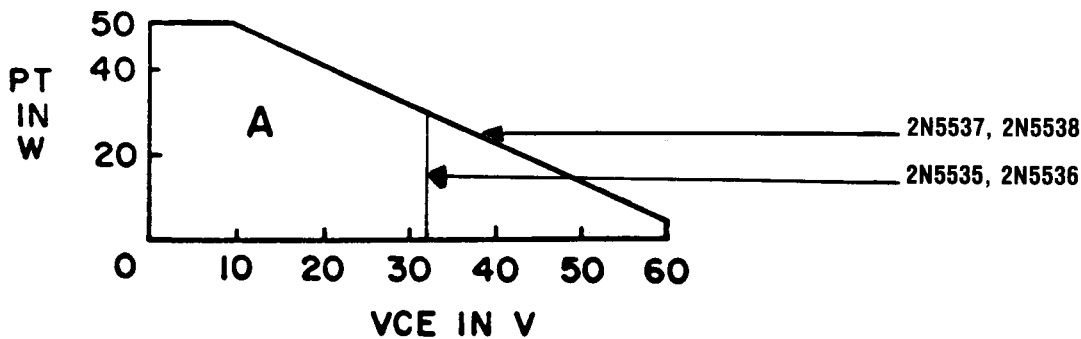
The suggested test circuits are shown for each type of SOAR operation. Any other thermally stable circuit may also be used as long as the SOAR conditions and maximum ratings are observed.

SOAR VALUES

TYPE NUMBER	V1 V	V2 V
2N5535	40	60
2N5536	40	60
2N5537	65	90
2N5538	65	90

CONTINUOUS DC OPERATION

- Conditions:**
1. $T_J = T_{CASE} + \Theta_{J-C} P_{DC} \leq 200^\circ\text{C}$
 2. $V_{CE} \leq 0.8 V_1$ rating for specified transistor type
 3. $P_T \leq P_T$ max rating for specified transistor type.
 4. $I_C \leq 20\text{A}$
 5. $P_T \leq P_T = f(V_{CE})$ Area A



RADIATION RESISTANT NPN SILICON POWER TRANSISTORS

2N5535 2N5536 2N5537 2N5538

PULSED FORWARD BIASED OPERATION

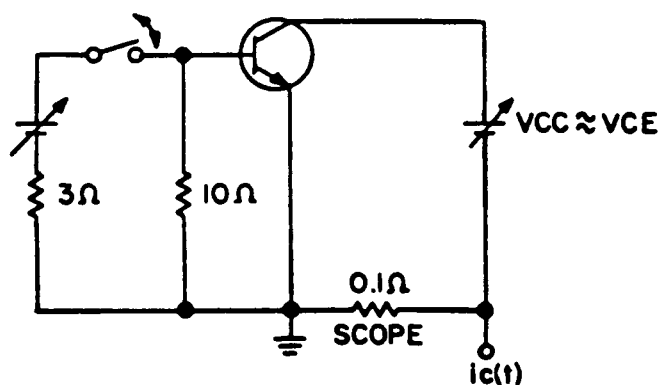
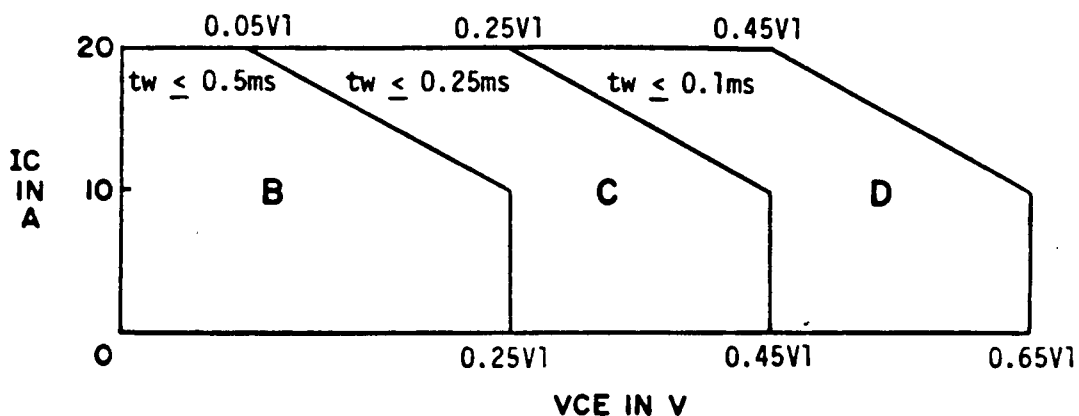
Conditions:

1. $T_J = T_{CASE} + \Theta_{J-C} P_{avg} \leq 200^\circ C$

2. $P_{avg} = \frac{1}{4 \text{ ms}} \int_0^{4 \text{ ms}} i_c v_{ce} dt \leq \text{the allowed continuous DC power dissipation}$

for a V_{CE} equal to the highest v_{ce} applied to the transistor.

3. Operation in the active region should be limited to a maximum pulse width of $t_w = 0.5 \text{ ms}$ for Area B, $t_w = 0.25 \text{ ms}$ for Area C and $t_w = 0.1 \text{ ms}$ for Area D. $t_r \leq 5 \mu s$ and $t_f \leq 5 \mu s$ for Areas B-D.



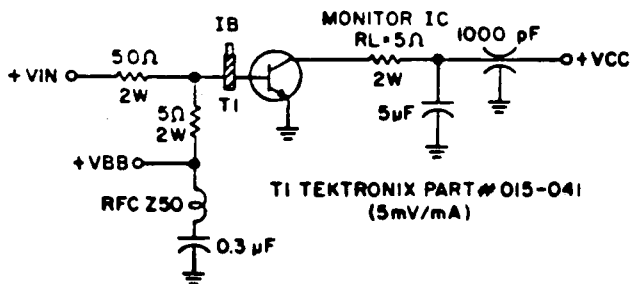
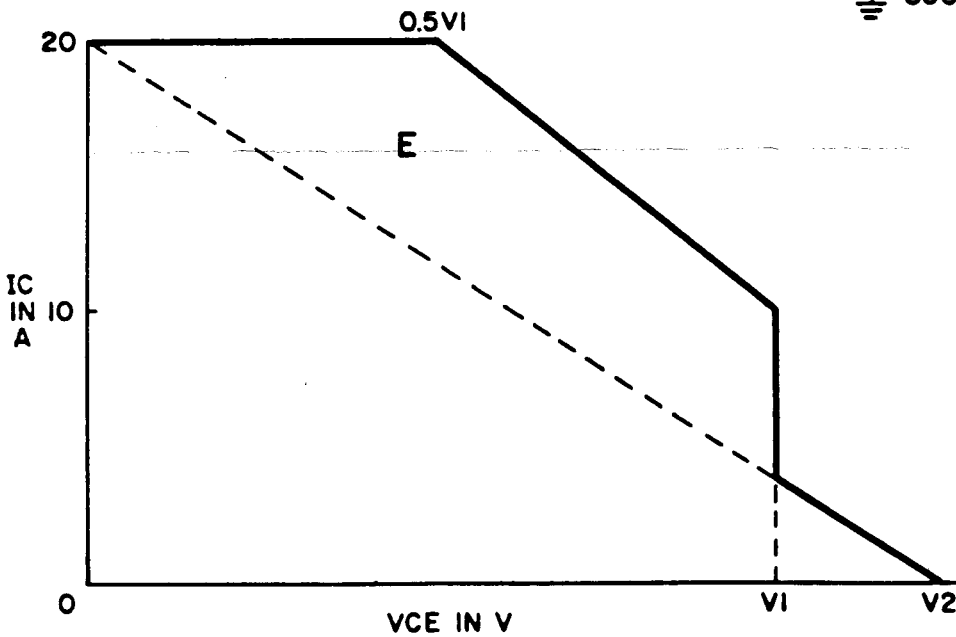
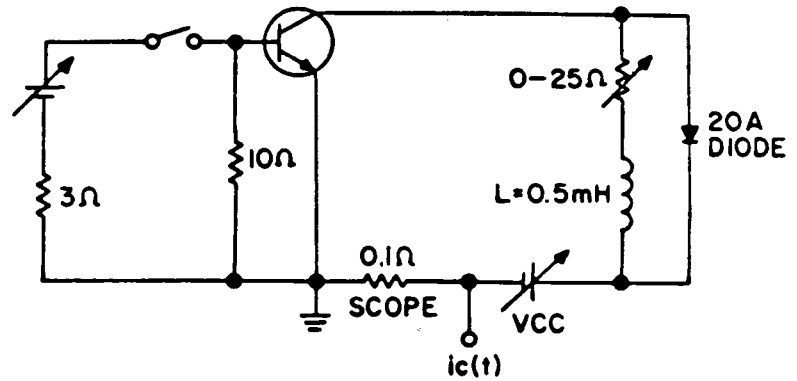
SUGGESTED TEST FREQUENCY $f = 25 \text{ Hz}$

RESISTIVE AND CLAMPED INDUCTIVE SWITCHING

(Switching from saturation to cutoff)

Conditions:

1. $T_J = T_C + \Theta_{J-C} P_{avg} \leq 200^\circ\text{C}$
2. $P_{avg} = \frac{1}{4\text{ms}} \int_0^{4\text{ms}} i_C v_{CE} dt \leq P_T \text{ max.}$
3. For the resistive loadline, $L = 0$ and $V_{CC} = V_2$ in the given circuit
4. $t_r \leq 2\mu\text{s}$, $t_f \leq 2\mu\text{s}$ in Area E



SATURATED SWITCHING TEST CIRCUIT

Maximum Switching Times: $t_d \leq 25 \text{ ns}$:

$t_r \leq 200 \text{ ns}$; $t_s \leq 300 \text{ ns}$; $t_f \leq 300 \text{ ns}$

Test Conditions: $V_{in} = 70 \text{ V}$ when generator with 50Ω internal impedance is terminated in a 50Ω load. $V_{BE} = -5 \text{ V}$; $V_{CE} = 55 \text{ V}$; $I_C \cong 10 \text{ A}$; $I_{B1} = 1 \text{ A}$, $I_{B2} \cong 1 \text{ A}$; $t_p = 400 \text{ ns}$; $f = 720 \text{ Hz}$.

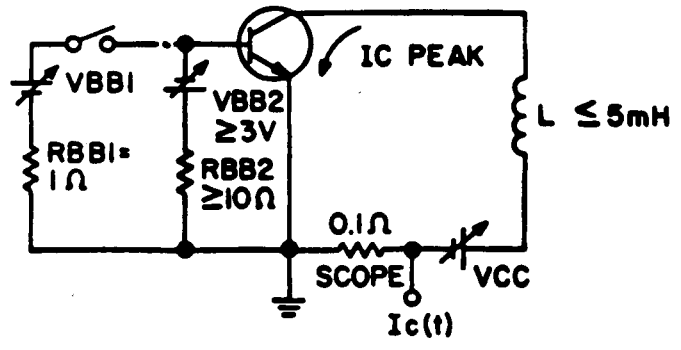
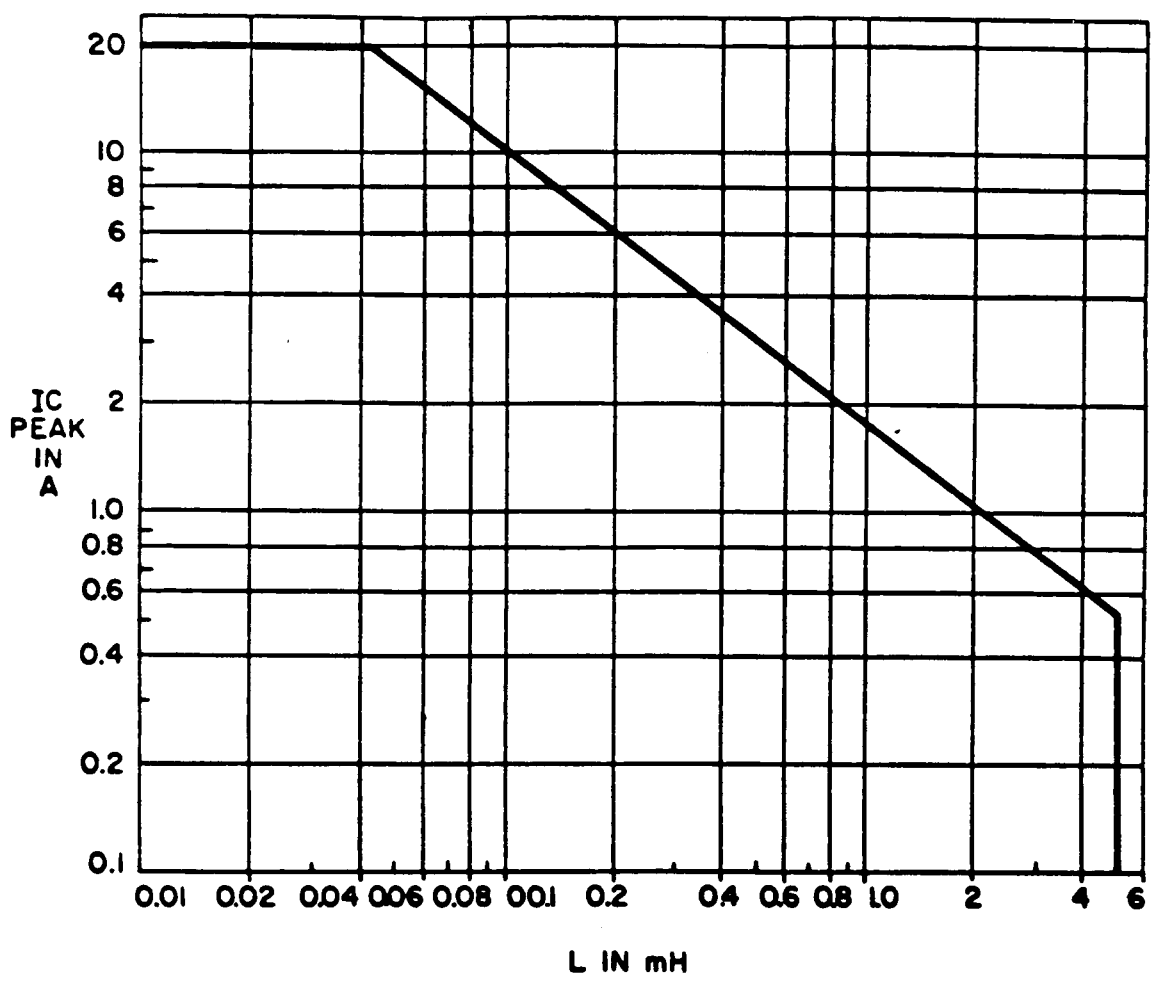
RADIATION RESISTANT NPN SILICON POWER TRANSISTORS

2N5535 2N5536 2N5537 2N5538

UNCLAMPED INDUCTIVE SWITCHING

(Switching from saturation to cutoff)

- Conditions:
1. $T_J = T_C + \Theta_{J-C} P_{avg} \leq 200^\circ\text{C}$
 2. $P_{avg} = \frac{1}{4\text{ms}} \int_0^{4\text{ms}} i_c v_{ce} dt \leq P_T \text{ of Area A at } 0.8 V_1$
 3. $\frac{1}{2} L I_C^2 \leq 8 \text{ mWs}$



Kennwerte bei 25°C (wenn nicht anders angegeben)

		min	max		Fig.
Statisch					
Gate-Source-Durchbruchspg.	$U_{(BR)GSS}$	-50		V	$I_G = -1\mu A, U_{DS} = 0V$
Gate-Sperrstrom	I_{GSS}		-0,25	nA	$U_{GS} = -30V, U_{DS} = 0V$
Gate-Sperrstrom (150°C)	I_{GSS}		-0,50	μA	$U_{GS} = -30V, U_{DS} = 0V$
Drainstrom (Gate 0V)	I_{DSS}	1	10	mA	$U_{DS} = 20V, U_{GS} = 0V$
Gate-Source-Restspg.	$U_{GS(off)}$	-1	-5	V	$U_{DS} = 20V, I_D = 1nA$
Dynamisch					
Kleinsignal-Vorwärtssteilheit Sourceschaltung (kurzgeschl.)	$ Y_{fs} $	2000	7000	μS	$U_{DS} = 20V, U_{GS} = 0V,$ $f = 1kHz$
Kleinsignal-Ausgangs- Scheinleitwert Sourceschaltung (kurzgeschl.)	$ Y_{os} $		10	μS	$U_{DS} = 20V, U_{GS} = 0V,$ $f = 1kHz$
Kleinsignal-Eingangskapazität Sourceschaltung (kurzgeschl.)	C_{iss}		20	pF	$U_{DS} = 20V, U_{GS} = 0V,$ $f = 1MHz$
Kleinsignal-Rückwirkkapazität Sourceschaltung (kurzgeschl.)	C_{rss}		5	pF	$U_{DS} = 20V, U_{GS} = 0V,$ $f = 1MHz$
Rauschverhalten					
Äquivalente Eingangsrauschspg. (kurzgeschl.)	e_N				
2N5592			10	nV/ \sqrt{Hz}	$U_{DS} = 5V, U_{GS} = 0V$ $f = 10Hz$
2N5593		15			
2N5594		20			
Rauschzahl (1), Sourceschaltung NF					
2N5592			2,5	dB	$U_{DS} = 5V, U_{GS} = 0V,$ $f = 10Hz, R_G = 10k\Omega$
2N5593		6			
2N5594		10			

(1) Quellwiderstand (R_G) entspricht nicht dem Wert für optimales Rauschen. Die Angabe des Rauschwertes (NF) bei nichtangepasstem Quellwiderstand ist beabsichtigt, um den Zusammenhang zwischen NF und e_N zu zeigen. Quellwiderstände für optimales Rauschen siehe Fig. 2, 3, 4.

Typische Kennlinien bei 25°C (wenn nicht anders angegeben)

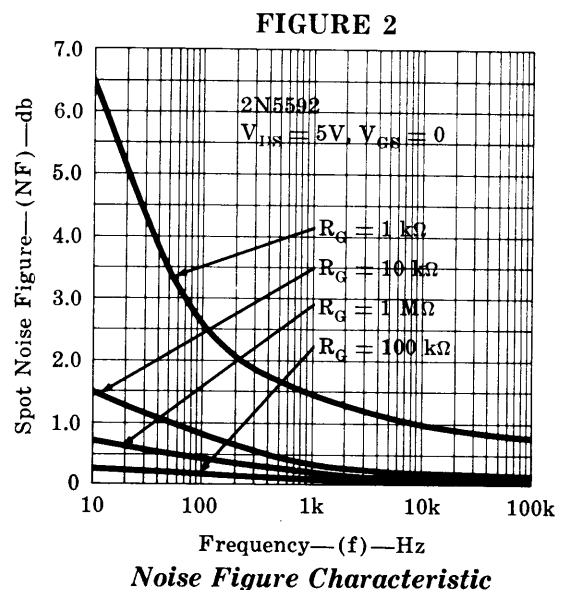
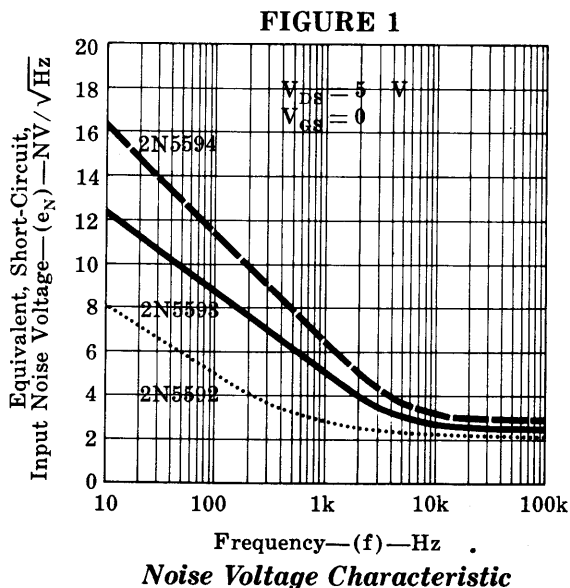


FIGURE 3

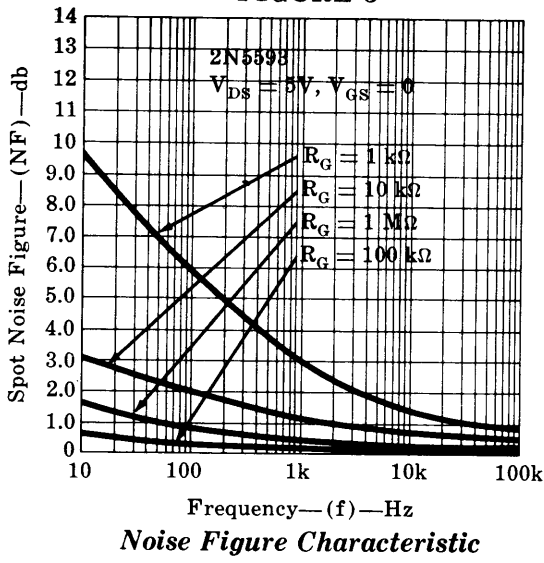


FIGURE 4

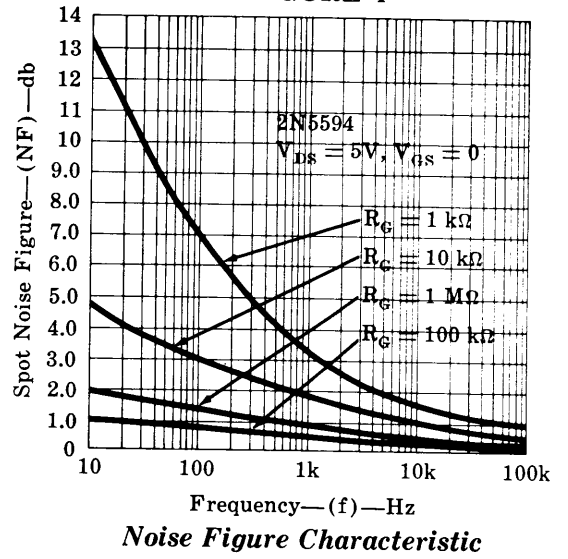


FIGURE 5

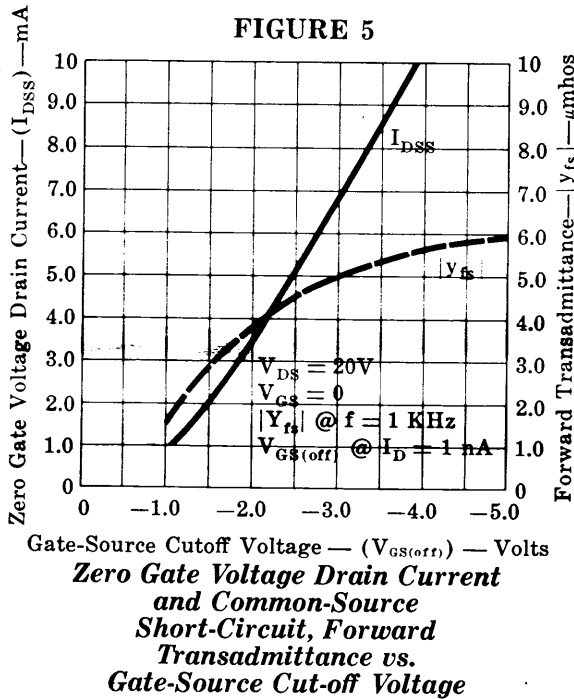


FIGURE 6

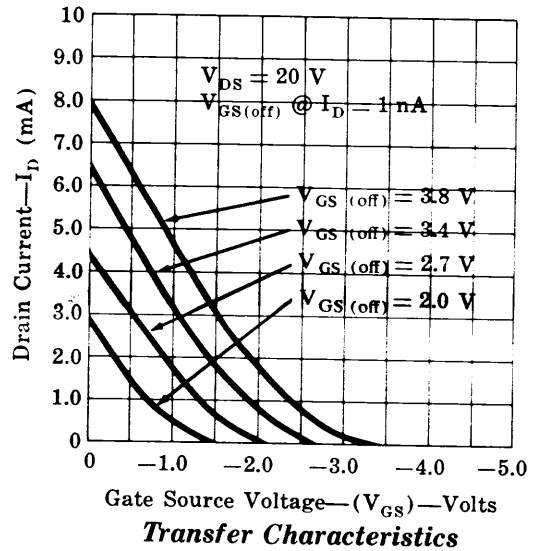


FIGURE 7

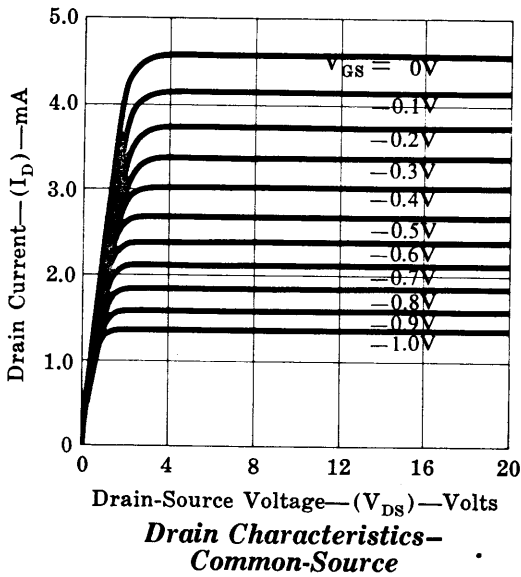


FIGURE 8

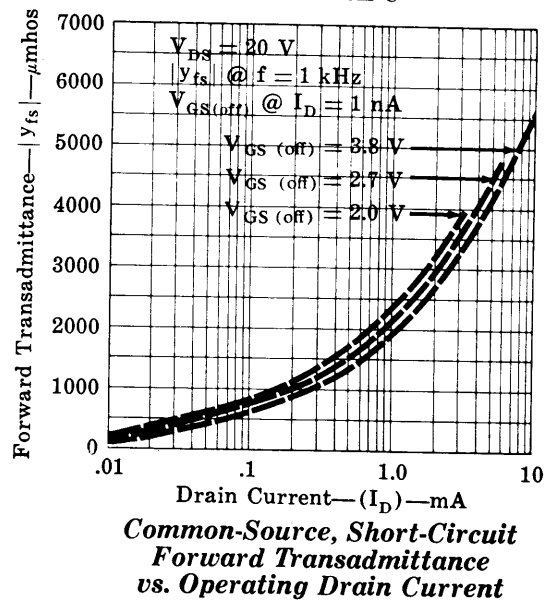
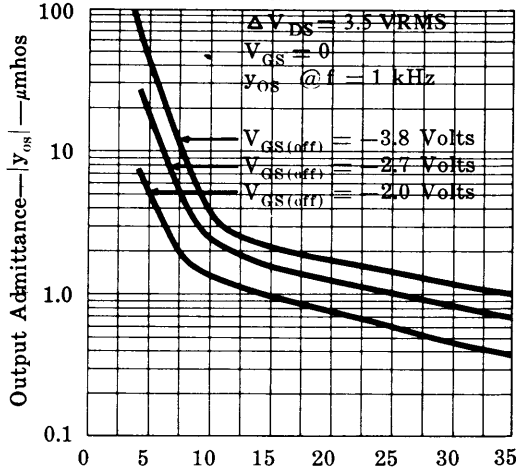
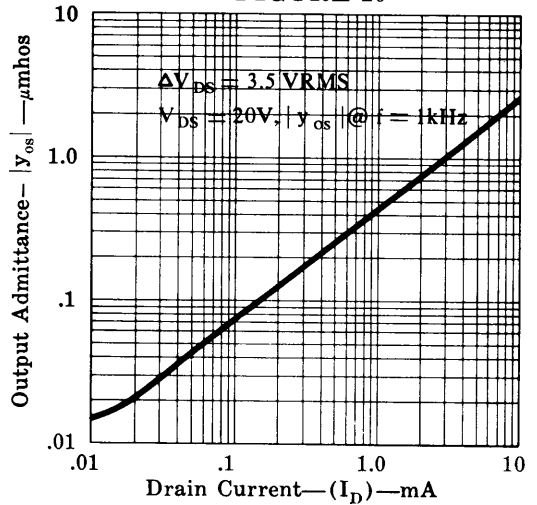


FIGURE 9



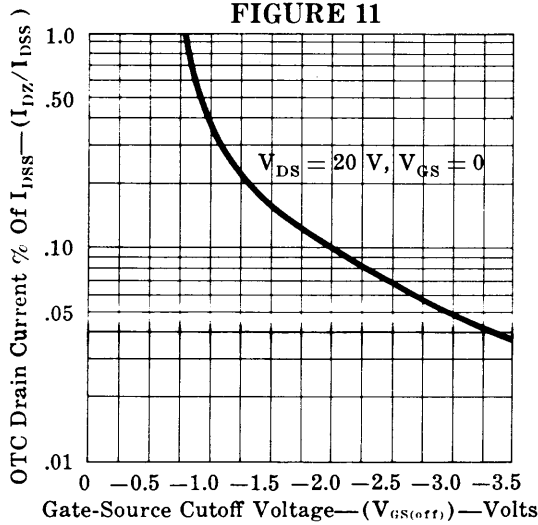
Common-Source, Short-Circuit, Output Admittance vs. Drain-Source Voltage

FIGURE 10



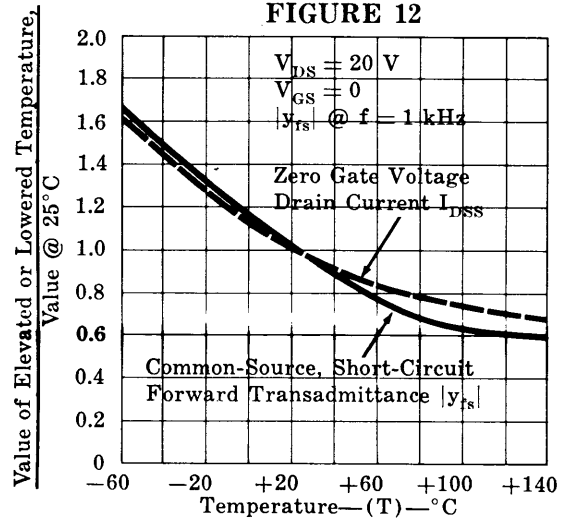
Common-Source, Short-Circuit Output Admittance vs. Drain Current

FIGURE 11



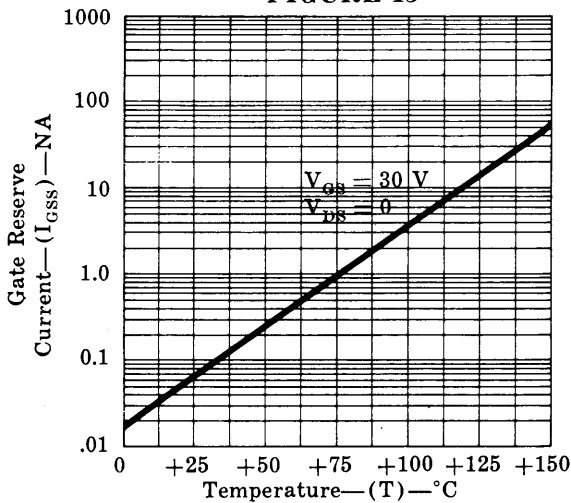
Drain Current "0" Temperature Coefficient Point

FIGURE 12



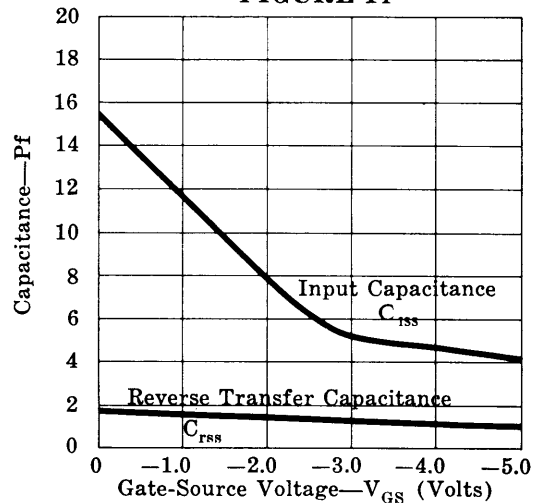
Normalized Zero Gate Voltage Drain Current and Common-Source, Short-Circuit Forward Transadmittance vs. Temperature

FIGURE 13



Gate Reserve Current vs. Temperature

FIGURE 14



Common-Source, Short-Circuit Junction Capacitances vs. Gate-Source Voltage

RADIATION RESISTANT NPN SILICON POWER TRANSISTORS

5.0 SUMMARY

SOLITRON RADIATION RESISTANT SILICON POWER TRANSISTORS

TYPE	CASE	MAXIMUM RATINGS				RADIATION PERFORMANCE								Θ_{JC} (°C/W)
		V _{CB0} (V)	V _{CE0} (V)	I _C (A)	P _T @ 25°C CASE (N)	Before				After 1x10 ¹⁴ n/cm**				
						hFE@ V _{CE} = 5		V _{CE} (SAT)@ I _C /I _E =5		hFE@ V _{CE} = 5V		V _{CE} (SAT)@ I _C /I _B 5		
						Min	I _C (A)	Max (V)	I _C (A)	Min	I _C (A)	Max (V)	I _C (A)	
2N5527	T0-5	60	40	5	5	40	3	1.0	3	15	3	2.0	3	35
2N5528	T0-111	60	40	10	35	40	3	1.0	3	15	3	2.0	3	5.0
2N5529	T0-61	60	40	10	35	40	3	1.0	3	15	3	2.0	3	5.0
2N5530	T0-61*	60	40	10	35	40	3	1.0	3	15	3	2.0	3	5.0
2N5531	T0-5	90	75	5	5	30	3	1.0	3	7	3	3.0	3	35
2N5532	T0-111	90	75	10	35	30	3	1.0	3	7	3	3.0	3	5.0
2N5533	T0-61	90	75	10	35	30	3	1.0	3	7	3	3.0	3	5.0
2N5534	T0-61*	90	75	10	35	30	3	1.0	3	7	3	3.0	3	5.0
2N5535	T0-61	60	50	20	50	50	5	1.0	5	15	5	2.0	5	3.5
2N5536	T0-61*	60	50	20	50	50	5	1.0	5	15	5	2.0	5	3.5
2N5537	T0-61	90	75	20	50	40	5	1.0	5	10	5	2.5	5	3.5
2N5538	T0-61*	90	75	20	50	40	5	1.0	5	10	5	2.5	5	3.5
BR100A	T0-5	75	60	5	5	75	2	0.3	2	15	2	2.0	2	35
BR100C	T0-111	75	60	10	35	75	2	0.3	2	15	2	2.0	2	5.0
BR100E	T0-61	75	60	10	35	75	2	0.3	2	15	2	2.0	2	5.0
BR100F	T0-61*	75	60	10	35	75	2	0.3	2	15	2	2.0	2	5.0
BR101A	T0-5	90	80	5	5	70	2	0.3	2	15	2	3.0	2	35
BR101C	T0-111	90	80	10	35	70	2	0.3	2	15	2	3.0	2	5.0
BR101E	T0-61	90	80	10	35	70	2	0.3	2	15	2	3.0	2	5.0
BR101F	T0-61*	90	80	10	35	70	2	0.3	2	15	2	3.0	2	5.0
BR200A	T0-61	70	60	20	50	50	5	0.3	4	15	5	1.8	4	35
BR200B	T0-61*	70	60	20	50	50	5	0.3	4	15	5	1.8	4	35
BR201A	T0-61	80	80	20	50	50	5	0.3	4	10	5	2.8	4	35
BR201B	T0-61*	80	80	20	50	50	5	0.3	4	10	5	2.8	4	35

* WITH ISOLATED COLLECTOR

** NEUTRON FLUENCE - MEV EQUIVALENT

† EXCEPTION TO JEDEC SPEC.

5.1. Detailed specifications for above devices follow except: for 2N5528, 2N5532 which, except for case, are similar to 2N5529, 2N5533 respectively.