RCA MOS FIELD-EFFECT TRANSISTOR

For Critical Chopper Applications & Multiplex Service

3N138

File No. 283

RCA-3N138‡ is a silicon, insulated-gate field-effect transistor of the N-channel depletion type, utilizing the MOS* construction. It is intended primarily for critical chopper and multiplex applications up to 60MHz.

This transistor features a New Terminal Arrangement in which the gate and source connections are interchanged to provide maximum isolation between the output (drain) and the input (gate) terminals. Although this new basing configuration does not appreciably change the measured device feedback capacitance, it permits the use of external inter-terminal shields to reduce the feedback due to external capacitances, particularly on printed circuit boards. This feature makes it possible to minimize feedthrough capacitance.

The insulated gate provides a very high value of input resistance (10^{14} ohms typ.), which is relatively insensitive to temperature and is independent of gate-bias conditions (positive, negative, or zero bias). The 3N138 also features extremely low feedthrough capacitance (0.18pF typ.) and zero inherent offset voltage.

The 3N138 is hermetically sealed in the JEDEC TO-72 package and features a gate metallization that covers the entire source-to-drain channel.

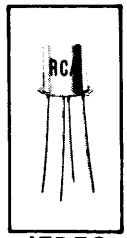
‡ Formerly Dev. No. TA7032.
* Metal-Oxide-Semiconductor.

Maximum Ratings, Absolute-Maximum Values:

(Substrate connected to source unless otherwise specified)

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+35 max.	V
DRAIN-TO-SUBSTRATE VOLTAGE, V_{DB}	+35, −0.3 max.	V
SOURCE-TO-SUBSTRATE VOLTAGE, V_{SB}	+35, −0.3 max.	V
DC GATE-TO-SOURCE VOLTAGE, V_{GS}	±10 max.	V
PEAK GATE-TO-SOURCE VOLTAGE, V_{GS}	±14 max.	V
PEAK VOLTAGE, GATE-TO-ALL OTHER TERMINALS: V_{GS}, V_{GD}, V_{GB}, non-repetitive	±45 max.	V
DRAIN CURRENT, I_D (Pulse duration 20 ms, duty factor ≤ 0.10)	50 max.	mA
TRANSISTOR DISSIPATION, P_T: At ambient temperatures from −65 to +125°C	150 max.	mW
AMBIENT TEMPERATURE RANGE:		
Storage	−65 to +150	°C
Operating	−65 to +125	°C
LEAD TEMPERATURE (During Soldering): At distances ≥ 1/32" to seating surface for 10 seconds max.	265 max.	°C

SILICON INSULATED-GATE FIELD-EFFECT TRANSISTOR N-Channel Depletion Type



JEDEC TO-72

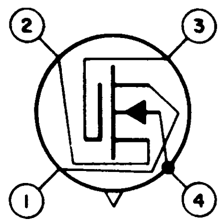
For Critical Chopper Applications and Multiplex Service up to 60 MHz: in Military Communications, Navigation, and Instrumentation Equipment in Industrial Instrumentation and Control Circuits

Applications

- **Servo Amplifiers**
- **Telemetry Amplifiers**
- **Computer Operational Amplifiers**
- **Sampling Circuits**
- **Electrometer Amplifiers**

Features

- **new terminal arrangement**



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

- **excellent thermal stability**
- **zero inherent offset voltage**
- **low leakage current: 10 pA max.**
- **low "on" resistance —** $r_{DS}(on) = 240\Omega$ **typ.** ($V_{GS} = 0V$)
- **high "off" resistance —** $R_{DS}(off) = 10^{10}\Omega$ **typ.**
- **low feedback capacitance —** $C_{rss} = 0.18pF$ **typ.**
- **low input capacitance —** $C_{iss} = 3pF$ **typ.**
- **symmetrical configuration — permits interchangeability of drain and source**

ELECTRICAL CHARACTERISTICS, at T_A = 25° C, Unless Otherwise Specified. Substrate Connected to Source.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS Type 3N138			UNITS
			Min.	Typ.	Max.	
Gate-Leakage Current	I_{GSS}	$V_{GS} = \pm 10$, $V_{DS} = 0$, $T_A = 25°C$ $V_{GS} = \pm 10$, $V_{DS} = 0$, $T_A = 125°C$	— —	0.1 20	10 200	pA pA
Drain-to-Source "ON" Resistance	$r_{DS}(on)$	$V_{GS} = 0$, $V_{DS} = 0$, f = 1 KHz, $T_A = 25°C$ $V_{GS} = +10$, $V_{DS} = 0$, f = 1 KHz, $T_A = 25°C$ $V_{GS} = 0$, $V_{DS} = 0$, f = 1 KHz, $T_A = 125°C$	— — —	240 135 350	300 — —	Ω Ω Ω
Drain-to-Source "OFF" Resistance	$R_{DS}(off)$	$V_{GS} = -10$, $V_{DS} = +1$	2×10^8	10^{10}	—	Ω
Drain-to-Source Cutoff Current	$I_D(off)$	$V_{GS} = -10$, $V_{DS} = +1$, $T_A = 25°C$ $V_{GS} = -10$, $V_{DS} = +1$, $T_A = 125°C$	— —	0.01 0.01	0.5 0.5	nA μA
Small-Signal, Short-Circuit, Reverse Transfer Capacitance	C_{rss}	$V_{GS} = -10$, $V_{DS} = 0$, f = 1 MHz	—	0.18	0.25	pF
Small-Signal, Short-Circuit, Input Capacitance	C_{iss}	$V_{GS} = -10$, $V_{DS} = 0$, f = 1 MHz	—	3	5	pF
Zero-Gate-Bias Forward Transconductance	g_{fs}	$V_{GS} = 0$, $V_{DS} = 12$	—	6000	—	μmho
Offset Voltage	V_0	$V_{GS} = \pm 10$, $V_{DS} = 0$	—	0*	—	V

* In measurements of Offset Voltage, thermocouple effects and contact potentials in the measurement setup may cause erroneous readings of 1 microvolt or more. These errors may be minimized by the use of solder having a low thermal e.m.f., such as Leeds & Northrup No. 107-1.0.1, or equivalent.

OPERATING CONSIDERATIONS

The flexible leads of the 3N138 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons should be grounded, and appropriate precautions should be taken to protect the device against high electric fields.

This device should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the device.

TYPICAL CHARACTERISTICS

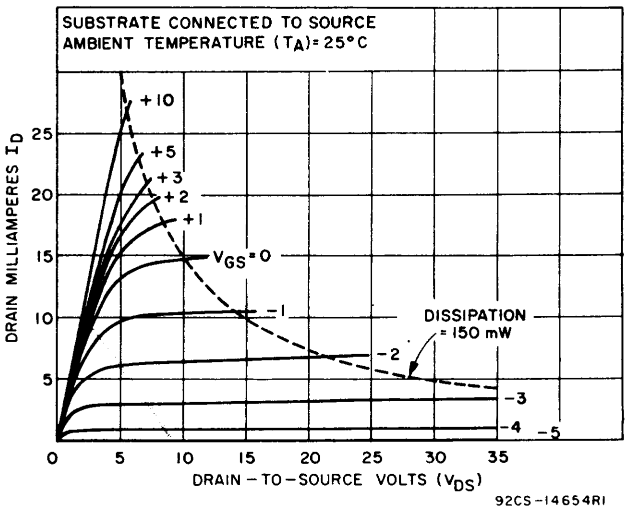


Fig. 1 — Drain Current vs Drain-to-Source Voltage

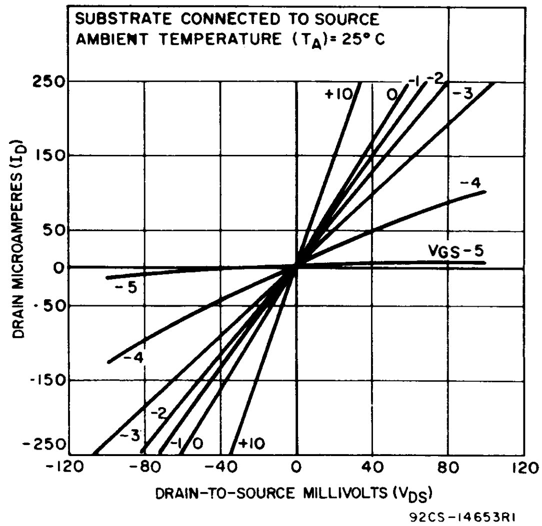


Fig. 2 — Low-Level Drain Current vs Drain-to-Source Voltage

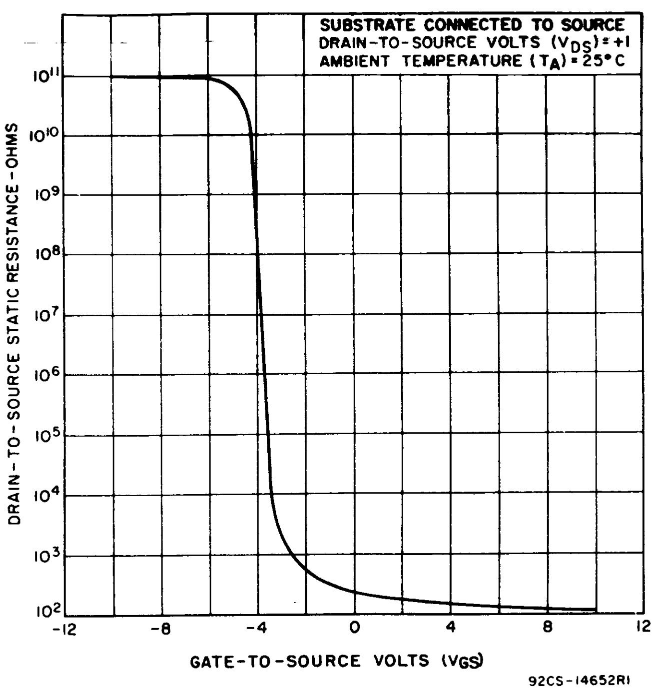
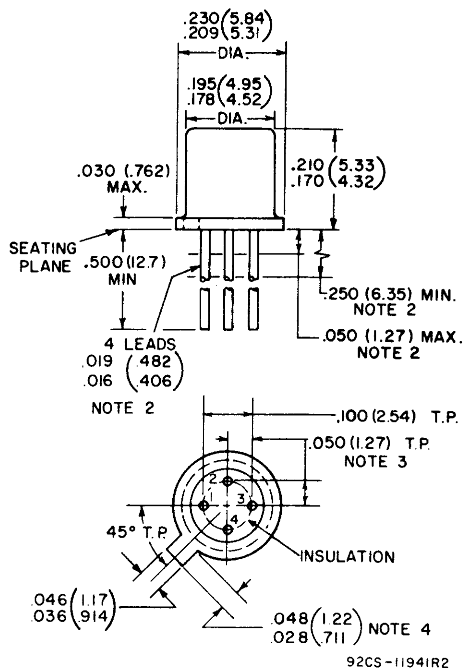


Fig. 3 — Drain-to-Source Static Resistance vs Gate-to-Source Voltage

DIMENSIONAL OUTLINE
JEDEC TO-72



Dimensions in inches and millimeters

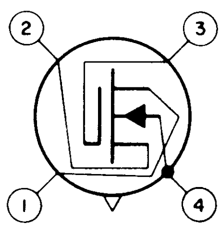
Note 1: *Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.*

Note 2: The specified lead diameter applies in the zone between 0.050" (1.27 mm) and 0.250" (6.35 mm) from the seating plane. From 0.250" (6.35 mm) to the end of the lead a maximum diameter of 0.021" (0.533 mm) is held. Outside of these zones, the lead diameter is not controlled.

Note 3: Leads having a maximum diameter of 0.019" (0.482 mm) at a gauging plane of 0.054" (1.372 mm) + 0.001" (0.025 mm) - 0.000" (0.000 mm) below seating plane shall be within 0.007" (0.177 mm) of their true position (location) relative to a maximum width of tab.

Note 4: Measured from actual maximum diameter.

TERMINAL DIAGRAM



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

RCA MOS FIELD-EFFECT TRANSISTOR

For Industrial and Military Applications to 175 MHz

3N142

File No 286

RCA-3N142† is a silicon, insulated-gate field-effect transistor of the N-channel depletion type utilizing the MOS* construction. It features

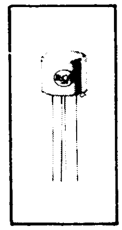
- high input resistance — 1000 megohms
- low feedback capacitance — 0.2pF max.
- low noise figure — 4dB typ.
- high useful power gain —
  neutralized — 17dB typ. } at 100MHz
  unneutralized — 14dB typ. }
- hermetically sealed TO-104 metal package

RCA-3N142 is intended primarily for use as the rf amplifier in FM receivers covering the 88 to 108MHz band, but can be used for general amplifier applications at frequencies up to 175 MHz.

The wide dynamic range of the 3N142 reduces cross-modulation effects in AM receivers and minimizes the generation of spurious responses in FM receivers.

† Formerly Dev. No. TA7306
* Metal-Oxide-Semiconductor

SILICON INSULATED-GATE FIELD-EFFECT TRANSISTOR N-Channel Depletion Type



JEDEC TO-104

For Frequencies up to 175 MHz

Applications

- **RF Amplifier, Mixer, and Oscillator in:**
  CB and Mobile Communication Receivers
  Aircraft and Marine Receivers
  CATV and MATV Equipment
- **Industrial Control Circuits**
- **Variable Attenuators**
- **Current Limiters**
- **Instrumentation Equipment**
- **High-Impedance Timing Circuits**

Performance Features

- **large dynamic range**
- **enhanced signal-handling capability for low cross-modulation**
- **dual-polarity gate permits positive and negative swing without degradation of input impedance**
- **reduced spurious responses in FM receivers**
- **permits use of vacuum-tube biasing techniques**
- **excellent thermal stability for critical oscillator designs**

Maximum Ratings, Absolute-Maximum Values:

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+20 max.	V
GATE-TO-SOURCE VOLTAGE, V_{GS}:		
Continuous	0 to −8 max.	V
Instantaneous	±15 max.	V
DRAIN-TO-GATE VOLTAGE, V_{DG}	+20 max.	V
DRAIN CURRENT, I_D**	50 max.	mA
TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 85°C	100 max.	mW
At ambient temperatures above 85°C	Derate at 6.67mW/°C	
AMBIENT TEMPERATURE RANGE:		
Storage	−65 to +100	°C
Operating	−65 to +100	°C
LEAD TEMPERATURE (During Soldering):		
At distances ≥ 1/32" from seating surface for 10 seconds max.	265 max.	°C

** Pulse Value. Pulse duration, 20ms max., Duty factor ≤0.1

ELECTRICAL CHARACTERISTICS, at T_A = 25° C Unless Otherwise Specified. Bulk (Substrate) Connected to Source

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS				LIMITS			UNITS
		FREQUENCY f	DC DRAIN-TO-SOURCE VOLTAGE V_{DS}	DC GATE-TO-SOURCE VOLTAGE V_{GS}	DC DRAIN CURRENT I_D	TYPE 3N142			
		MHz	V	V	mA	Min.	Typ.	Max.	
Drain-to-Source Cutoff Current	$I_D(off)$		20	−8		—	—	100	μA
Zero-Bias Drain Current*	I_{DSS}		15	0		5	20	50	mA
Gate Reverse Current	I_{GSS}	T_A = 25°C	0	−8		—	—	1	nA
		T_A = 100°C	0	−8		—	—	100	nA
Gate-to-Source Cutoff Voltage	$V_{GS}(off)$		20		0.05	−2	−5	−8	V
Small-Signal, Short-Circuit Reverse-Transfer Capacitance (Drain-to-Gate)	C_{rss}	1	15		5	—	0.12	0.2	pF
Input Resistance	r_{is}	100	15		5	2	4.5	—	KΩ
Input Capacitance	C_{iss}	1	15		5	—	5.5	10	pF
Output Resistance	r_{os}	100	15		5	2.25	4.2	—	KΩ
Output Capacitance	C_{oss}	100	15		5	—	1.4	—	pF
Forward Transconductance	g_{fs}	100	15		5	4	7.5	—	mmho
Maximum Available Power Gain	MAG	100	15		5	—	24	—	dB
Maximum Usable Power Gain (Unneutralized)	MUG	100	15		5	—	14	—	dB
Maximum Usable Power Gain (Neutralized)	MUG	100	15		5	15	17	—	dB
Noise Figure	NF	100	15		5	—	4	5	dB

* Pulse test: Pulse Duration 20 ms max. Duty Factor ≤0.15.

OPERATING CONSIDERATIONS

The flexible leads of the 3N142 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons should be grounded, and appropriate precautions should be taken to protect the device against high electric fields.

This device should not be connected into, or disconnected from, circuits with the power on because high transient voltages may cause permanent damage to the device.

TYPICAL CHARACTERISTICS

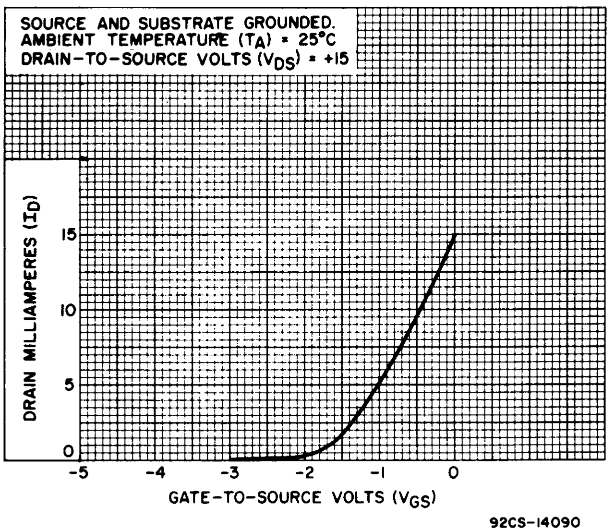


Fig. 1 – Typical Characteristic of Drain Current (I_D) vs Gate-to-Source Voltage (V_{GS})

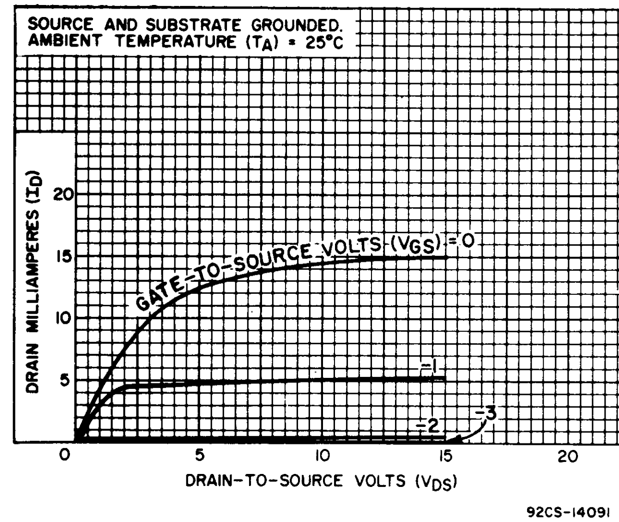


Fig. 2 – Drain Current (I_D) vs Drain-to-Source Voltage (V_{DS})

TYPICAL y PARAMETER CHARACTERISTICS

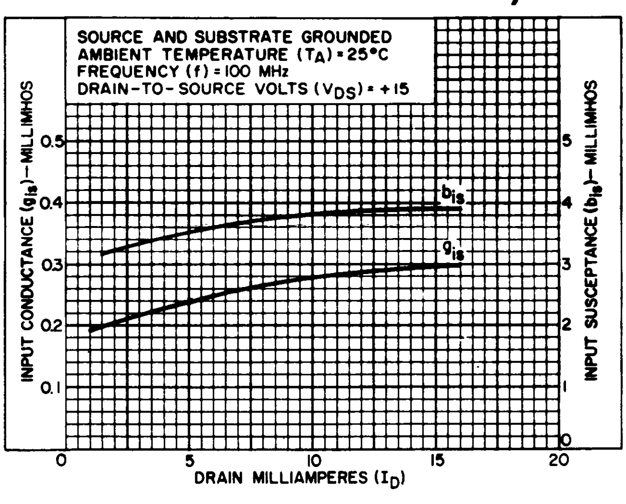


Fig. 3 – Input Admittance (y_{is}) vs Drain Current (I_D)

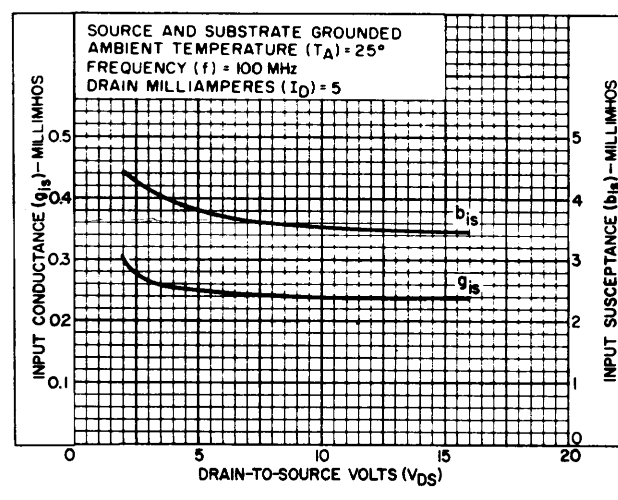


Fig. 4 – Input Admittance (y_{is}) vs Drain-to-Source Voltage (V_{DS})

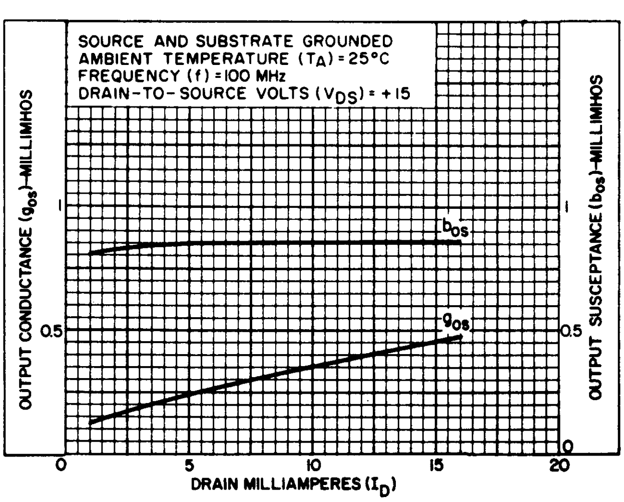


Fig. 5 – Output Admittance (y_{os}) vs Drain Current (I_D)

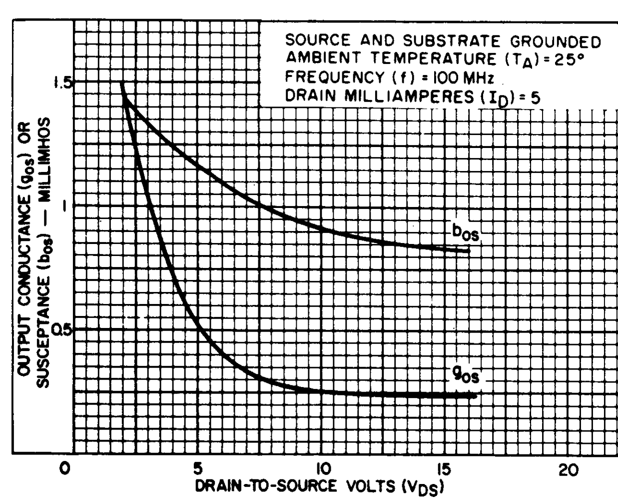


Fig. 6 – Output Admittance (y_{os}) vs Drain-to-Source Voltage (V_{DS})

TYPICAL y PARAMETER CHARACTERISTICS

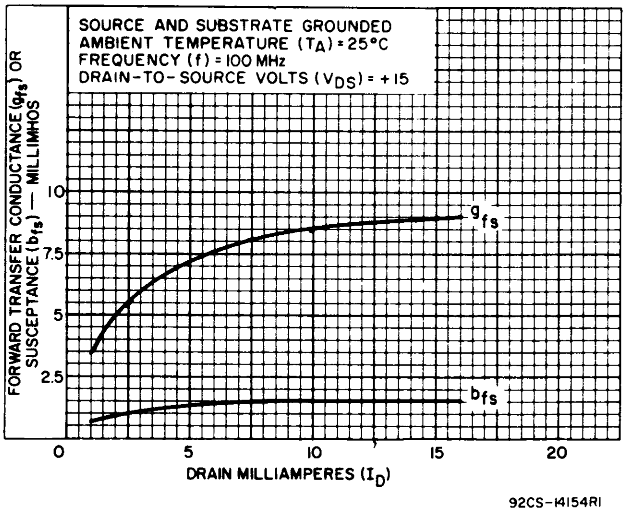


Fig. 7 – Forward Transadmittance (y_{fs}) vs Drain Current (I_D)

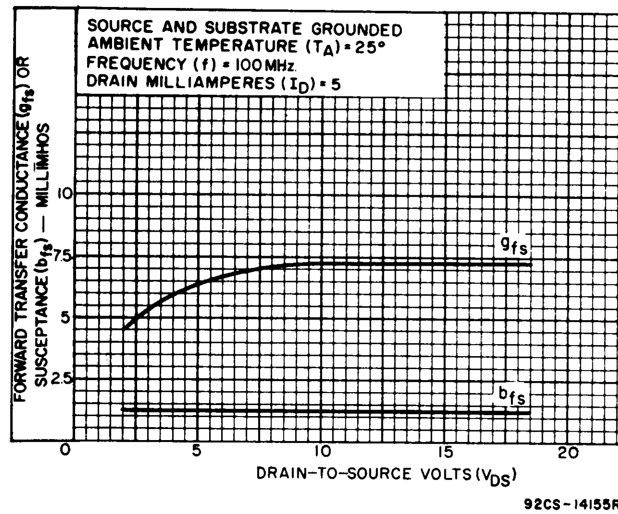


Fig. 8 – Forward Transadmittance (y_{fs}) vs Drain-to-Source Voltage (V_{DS})

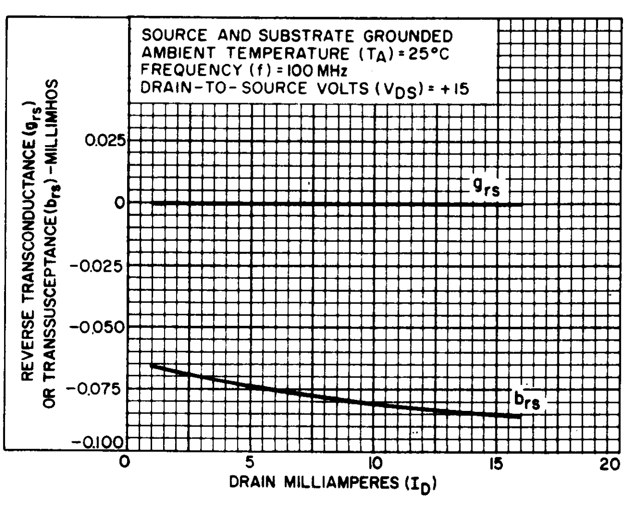


Fig. 9 – Reverse Transadmittance (y_{rs}) vs Drain Current (I_D)

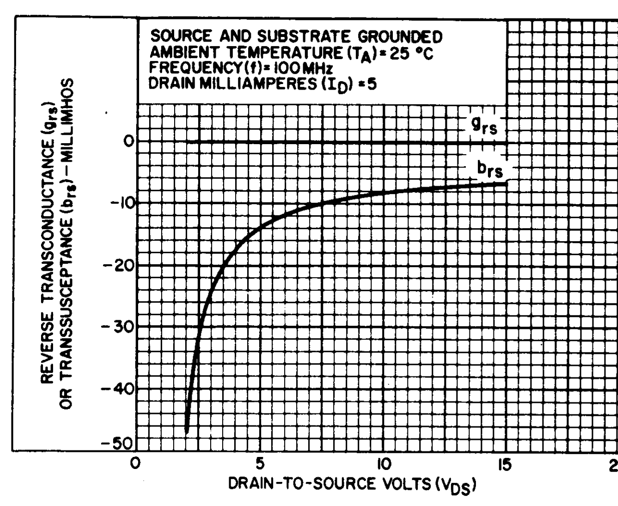


Fig. 10 – Reverse Transadmittance (y_{rs}) vs Drain-to-Source Voltage (V_{DS})

TYPICAL COMMON-SOURCE ADMITTANCE (Y) COMPONENTS vs FREQUENCY

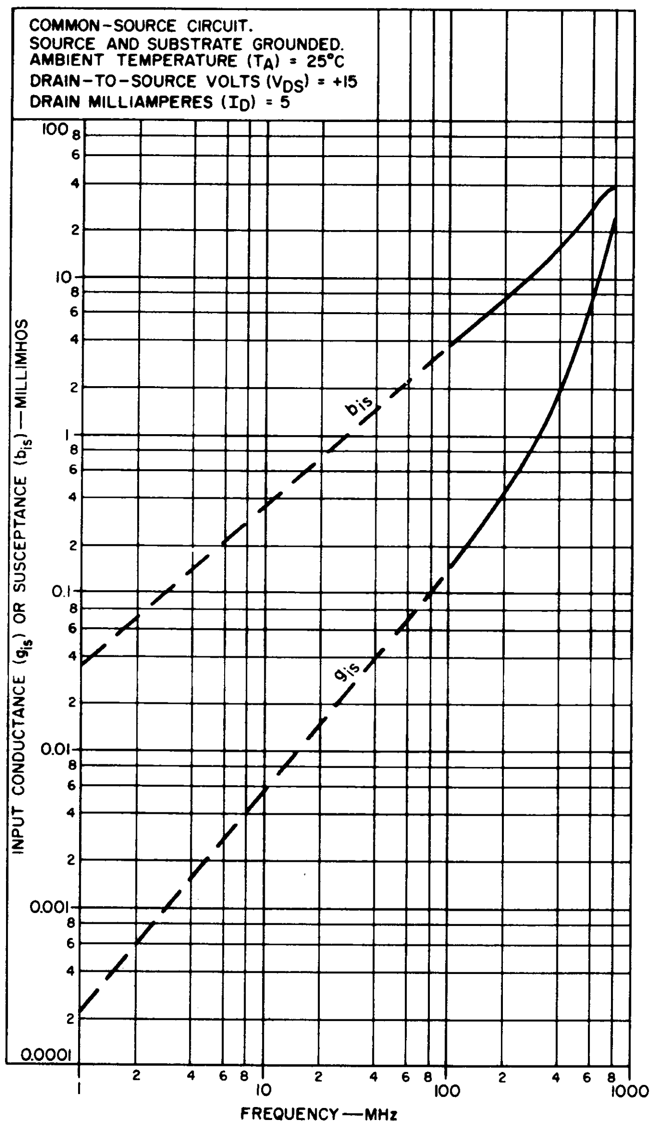


Fig. 11 – Input Admittance (Y_{is}) Components

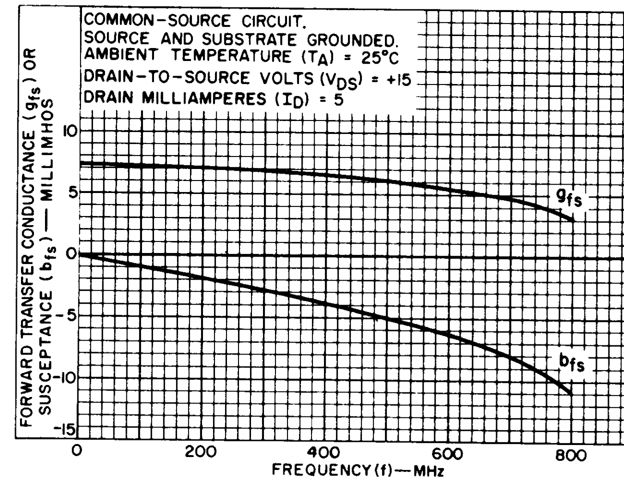


Fig. 12 – Forward Transadmittance (Y_{fs}) Components

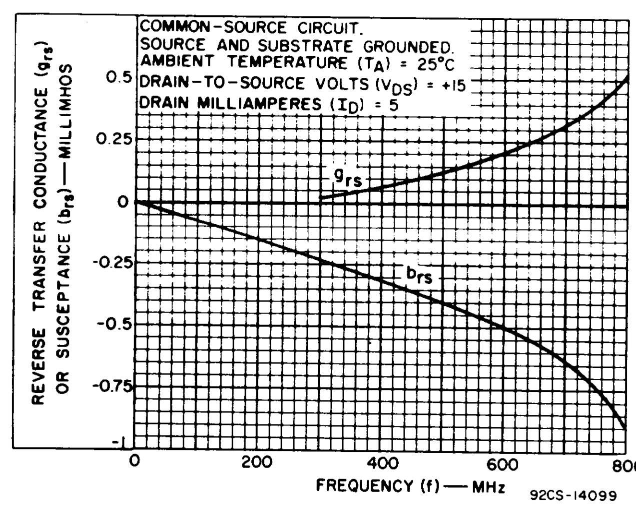


Fig. 13 – Reverse Transadmittance (Y_{rs}) Components

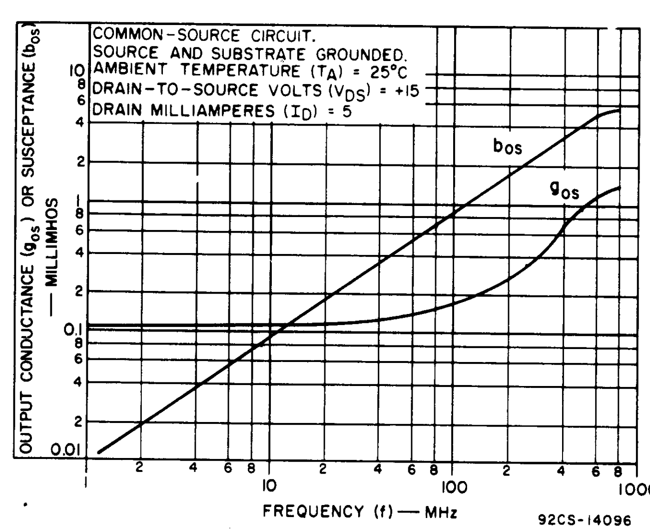
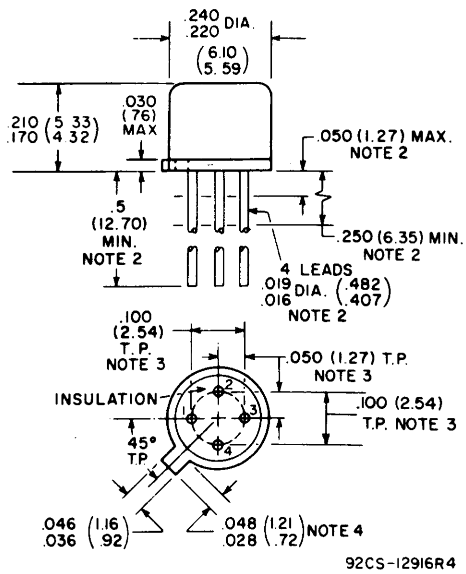


Fig. 14 – Output Admittance (Y_{os}) Components

DIMENSIONAL OUTLINE

TO-104



DIMENSIONS IN INCHES AND MILLIMETERS

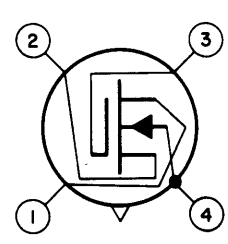
Note 1: *Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.*

Note 2: The specified lead diameter applies in the zone between 0.050" (1.27 mm) and 0.250"(6.35 mm) from the seating plane. From 0.250"(6.35 mm) to the end of the lead a maximum diameter of 0.021"(0.533 mm) is held. Outside of these zones, the lead diameter is not controlled.

Note 3: Leads having a maximum diameter of 0.019" (0.482 mm) at a gauging plane of 0.054"(1.372 mm) + 0.001" (0.025 mm) -0.000"(0.000 mm) below seating plane shall be within 0.007" (0.177 mm) of their true position (location) relative to a maxi-width of tab.

Note 4: Measured from actual maximum diameter.

TERMINAL DIAGRAM



LEAD 1 - DRAIN
LEAD 2 - SOURCE
LEAD 3 - INSULATED GATE
LEAD 4 - BULK (SUBSTRATE) AND CASE

Silicon Dual Insulated-Gate Field-Effect Transistor

With Integrated Gate-Protection Circuits

For Military and Industrial Applications up to 500 MHz

JEDEC TO-72 H-1299

Applications

- RF amplifier, mixer, and IF amplifier in military and industrial communications equipment
- Aircraft and marine vehicular receivers
- CATV and MATV equipment
- Telemetry and multiplex equipment

RCA-3N200♦ is an n-channel silicon, depletion type, dual insulated-gate field-effect transistor.

Special back-to-back diodes are diffused directly into the MOS▲ pellet and are electrically connected between each insulated gate and the FET's source. The diodes effectively bypass any voltage transients which exceed approximately ±10 volts. This protects the gates against damage in all normal handling and usage.

A feature of the back-to-back diode configuration is that it allows the 3N200 to retain the wide input signal dynamic range inherent in the MOSFET. In addition, the low junction capacitance of these diodes adds little to the total capacitance shunting the signal gate.

The excellent overall performance characteristics of the RCA-3N200 make it useful for a wide variety of rf-amplifier applications at frequencies up to 500 MHz. The two serially-connected channels with independent control gates make possible a greater dynamic range and lower cross-modulation than is normally achieved using devices having only a single control element.

The two-gate arrangement of the 3N200 also makes possible a desirable reduction in feedback capacitance by operating in the common-source configuration and ac-grounding Gate No. 2. The reduced capacitance allows operation at maximum gain *without neutralization;* and, of special importance in rf-amplifiers, it reduces local oscillator feedthrough to the antenna.

The 3N200 is hermetically sealed in the metal JEDEC TO-72 package.

▲ Metal-Oxide-Semiconductor.
♦ Formerly developmental type TA7684

Maximum Ratings, *Absolute-Maximum Values, at T_A = 25°C*

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	-0.2 to +20	V
GATE No.1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	-6 to +3	V
Peak ac	-6 to +6	V
GATE No.2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-6 to 30% of V_{DS}	V
Peak ac	-6 to +6	V
* DRAIN-TO-GATE VOLTAGE, V_{DG1} OR V_{DG2}	+20	V
* DRAIN CURRENT, I_D	50	mA
* TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	330	mW
At ambient temperatures above 25°C	derate linearly at 2.2 mW/°C	
* AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	°C
* LEAD TEMPERATURE (During soldering):		
At distances ≥1/32 inch from seating surface for 10 seconds max.	265	°C

*In accordance with JEDEC registration data format (JS-9 RDF-19A)

Performance Features

- Superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET s
- Wide dynamic range permits large-signal handling before overload
- Dual-gate permits simplified agc circuitry
- Virtually no agc power required
- Greatly reduces spurious responses in FM receivers

Device Features

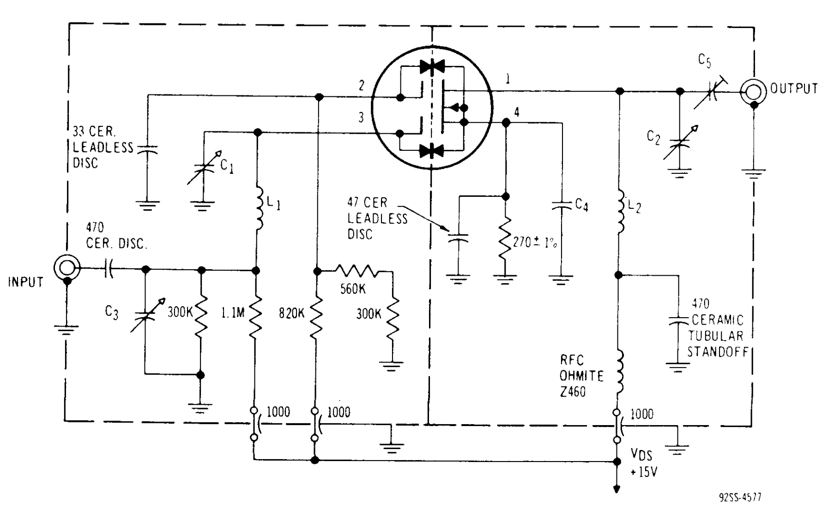
- Back-to-back diodes protect each gate against handling and in-circuit transients
- High forward transconductance – g_{fs} = 15,000 μmho (typ.)
- High unneutralized RF power gain – G_{ps} = 12.5 dB (typ.) at 400 MHz
  = 19 dB (typ.) at 200 MHz
- Low VHF noise figure – 4.5 dB (typ.) at 400 MHz
  3.0 dB (typ.) at 200 MHz

ELECTRICAL CHARACTERISTICS *at T_A = 25°C unless otherwise specified*		SYMBOLS	TEST CONDITIONS	LIMITS Min.	Typ.	Max.	UNITS
*	Gate No. 1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G2S} = +4 V	-0.1	-1	-3	V
*	Gate No. 2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G1S} = 0	-0.1	-1	-3	V
*	Gate No. 1-Terminal Forward Current	I_{G1SSF}	V_{G1S} = +1 V, V_{G2S} = V_{DS} = 0; T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
*	Gate No. 1-Terminal Reverse Current	I_{G1SSR}	V_{G1S} = −6 V, V_{G2S} = V_{DS} = 0; T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
*	Gate No. 2-Terminal Forward Current	I_{G2SSF}	V_{G2S} = +6 V, V_{G1S} = V_{DS} = 0; T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
*	Gate No. 2-Terminal Reverse Current	I_{G2SSR}	V_{G2S} = −6 V, V_{G1S} = V_{DS} = 0; T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
*	Zero-Bias Drain Current	I_{DS}	V_{DS} = +15 V, V_{G1S} = 0 V_{G2S} = +4 V	0.5	5.0	12	mA
*	Forward Transconductance (Gate No. 1-to-Drain)	g_{fs}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V; f = 1 kHz	10,000	15,000	20,000	μmho
	Small-Signal, Short-Circuit Input Capacitance†	C_{iss}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V; f = 1 MHz	4.0	6.0	8.5	pF
*	Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate-No. 1)♦	C_{rss}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V; f = 1 MHz	0.005	0.02	0.03	pF
	Small-Signal, Short-Circuit Output Capacitance	C_{oss}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V; f = 1 MHz	–	2.0	–	pF
*	Power Gain (see Fig. 1)	G_{PS}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V; f = 400 MHz	10	12.5	–	dB
	Noise Figure (see Fig. 1)	NF	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V; f = 400 MHz	–	4.5	6.0	dB
*	Bandwidth	BW	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V; f = 400 MHz	28	–	38	MHz
*	**Gate-to-Source Forward Breakdown Voltage** Gate No. 1	$V_{(BR)G1SSF}$	I_{G1SSF} = I_{G2SSF} = 100 μA; V_{G2S} = V_{DS} = 0	6.5	–	13	V
	Gate No. 2	$V_{(BR)G2SSF}$	I_{G1SSF} = I_{G2SSF} = 100 μA; V_{G1S} = V_{DS} = 0				
*	Gate-to-Source Reverse Breakdown Voltage Gate No. 1	$V_{(BR)G1SSR}$	I_{G1SSR} = I_{G2SSR} = 100 μA; V_{G2S} = V_{DS} = 0	-6.5	–	- 13	V
	Gate No. 2	$V_{(BR)G2SSR}$	I_{G1SSR} = I_{G2SSR} = 100 μA; V_{G1S} = V_{DS} = 0				

†Capacitance between Gate No. 1 and all other terminals.
♦Three-terminal measurement with Gate No. 2 and Source returned to guard terminal.
*In accordance with JEDEC registration data format (JS-9 RDF-19A)

OPERATING CONSIDERATIONS

The flexible leads of the 3N200 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons MUST be grounded.



All resistances in ohms
All capacitances in pF

C_1, C_2: 1.3-5.4 pF variable air capacitor: Hammerland Mac 5 type or equivalent

C_3: 1.9-13.8 pF variable air capacitor: Hammerland Mac 15 type or equivalent

C_4: Approx. 300 pF-capacitance formed between socket cover & chassis

C_5: 0.8-4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent

L_1, L_2: Inductance to tune circuit

Fig. 1 - 400 MHz power gain and noise figure test circuit

Typical Characteristics

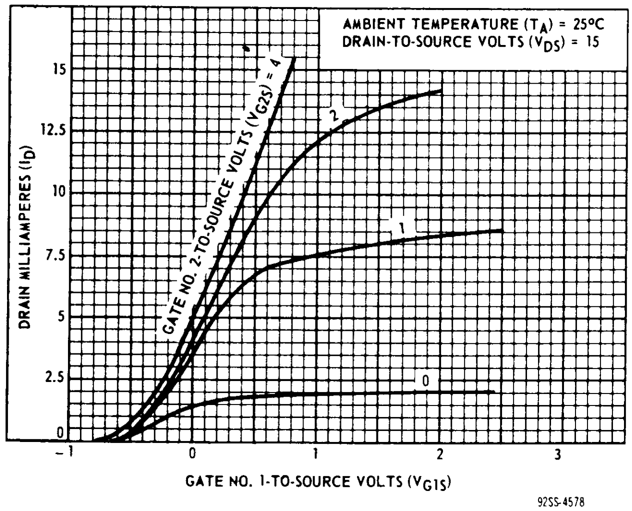


Fig. 2 - I_D vs. V_{G1S}

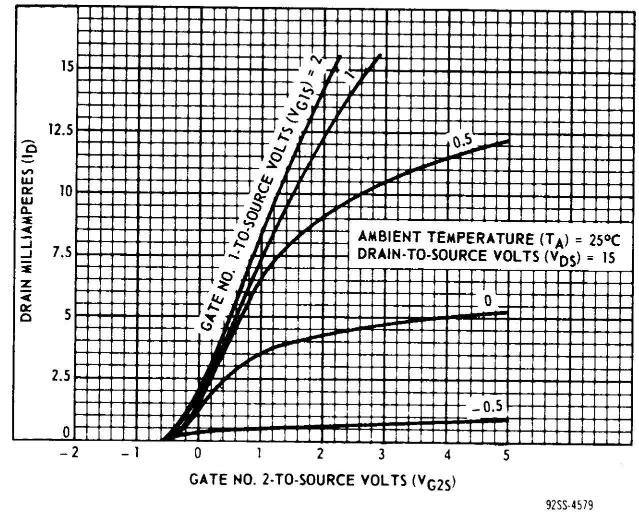


Fig. 3 - I_D vs. V_{G2S}

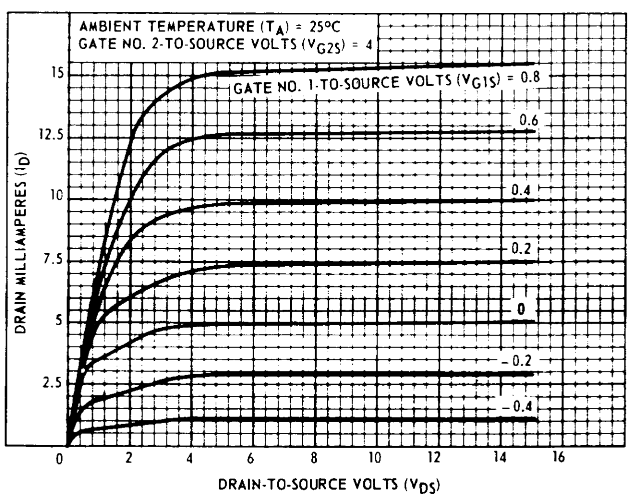


Fig. 4 - I_D vs. V_{DS}

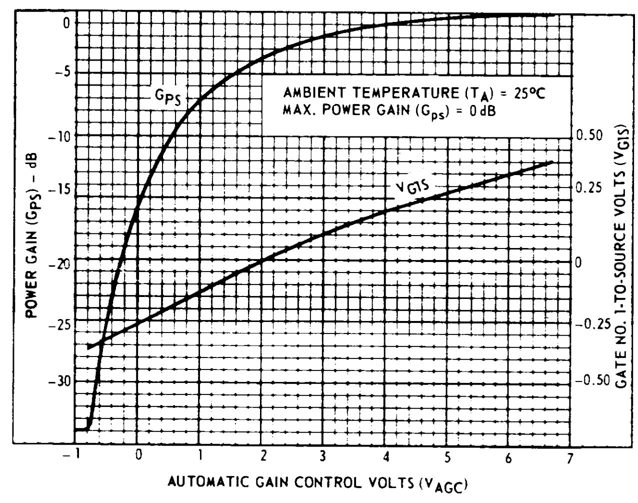


Fig. 5 - V_{AGC} vs. V_{G1S}

y and s Parameters vs. Frequency

TEST CONDITIONS: Drain-to-Source Volts (V_{DS}) = 15, Drain Milliamperes (I_D) = 10, Gate No. 2-to-Source Volts (V_{G2S}) = 4

CHARACTERISTICS	SYMBOL	FREQUENCY (MHz)					UNITS
		100	200	300	400	500	
Maximum Available Power Gain	MAG	32	24	17.5	13	10	dB
Maximum Usable Power Gain (Unneutralized)*	MUG	32	24	17.5	13	10	dB
Y Parameters							
Input Conductance	g_{is}	0.25	0.8	2.0	3.6	6.2	mmho
Input Susceptance	b_{is}	3.4	5.8	8.5	11.2	15.5	mmho
Magnitude of Forward Transadmittance	$\|y_{fs}\|$	15.3	15.3	15.4	15.5	16.3	mmho
Angle of Forward Transadmittance	$\angle y_{fs}$	-15	-25	-35	-47	-60	degrees
Output Conductance	g_{os}	0.15	0.3	0.5	0.8	1.1	mmho
Output Susceptance	b_{os}	1.5	2.7	3.6	4.25	5.0	mmho
Magnitude of Reverse Transadmittance	$\|y_{rs}\|$	0.012	0.025	0.06	0.14	0.26	mmho
Angle of Reverse Transadmittance	$\angle y_{rs}$	-60	-25	0	14	20	degrees
S Parameters							
Magnitude of Input Reflection Coeff.	$\|s_{is}\|$	0.97	0.90	0.84	0.78	0.70	
Angle of Input Reflection Coeff.	$\angle s_{is}$	-20	-32	-55	-68	-82	degrees
Magnitude of Forward Transmission Coeff.	$\|s_{fs}\|$	1.50	1.40	1.25	1.1	0.9	
Angle of Forward Transmission Coeff.	$\angle s_{fs}$	153	133	112	90	70	degrees
Mangitude of Output Reflection Coeff.	$\|s_{os}\|$	0.985	0.95	0.93	0.92	0.91	
Angle of Output Reflection Coeff.	$\angle s_{os}$	-7.5	-16	-22	-28	-34	degrees
Magnitude of Reverse Transmission Coeff.	$\|s_{rs}\|$	0.001	0.0025	0.005	0.010	0.0165	
Angle of Reverse Transmission Coeff.	$\angle s_{rs}$	100	125	141	150	142	degrees

*Limited only by practical design considerations

Typical y Parameters vs. V_{DS}

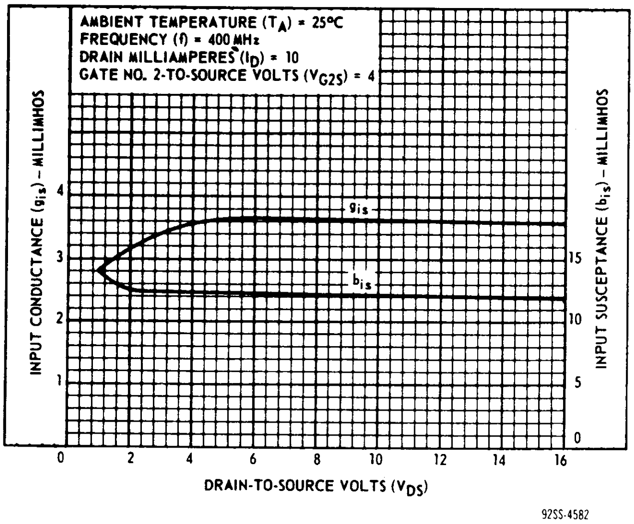


Fig. 6 - y_{is} vs. V_{DS}

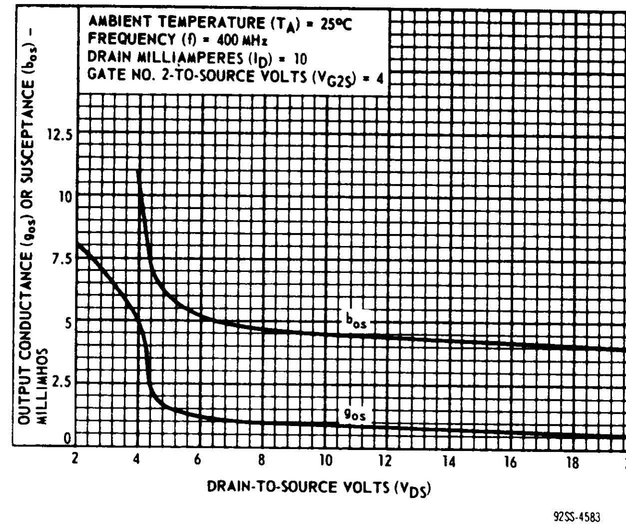


Fig. 7 - y_{os} vs. V_{DS}

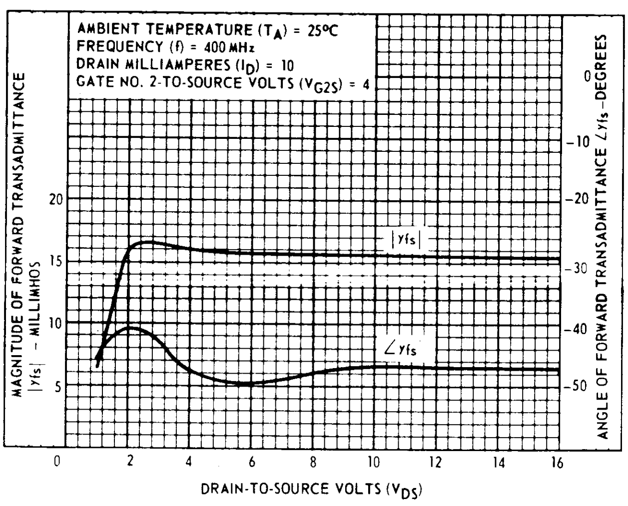


Fig. 8 - y_{fs} vs. V_{DS}

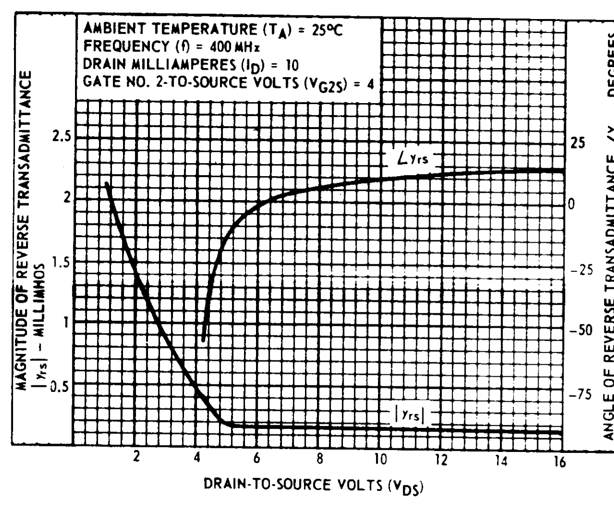


Fig. 9 - y_{rs} vs. V_{DS}

Typical y Parameters vs I_D

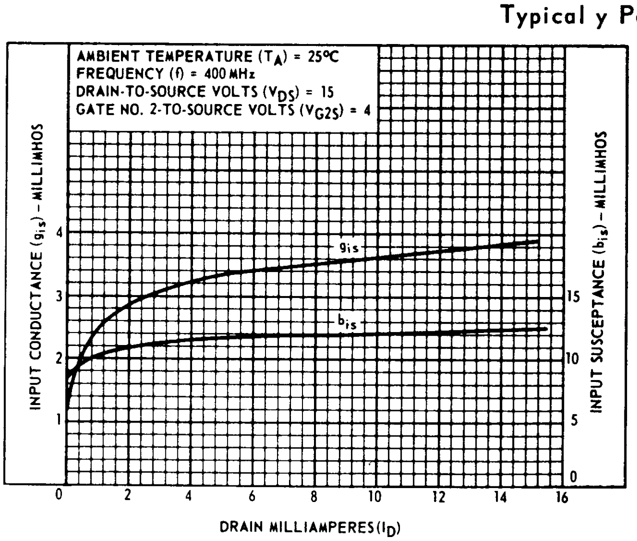


Fig. 10 - y_{is} vs. I_D

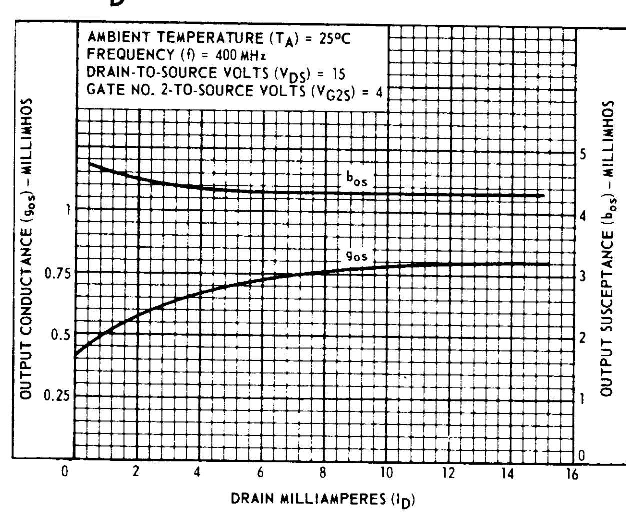
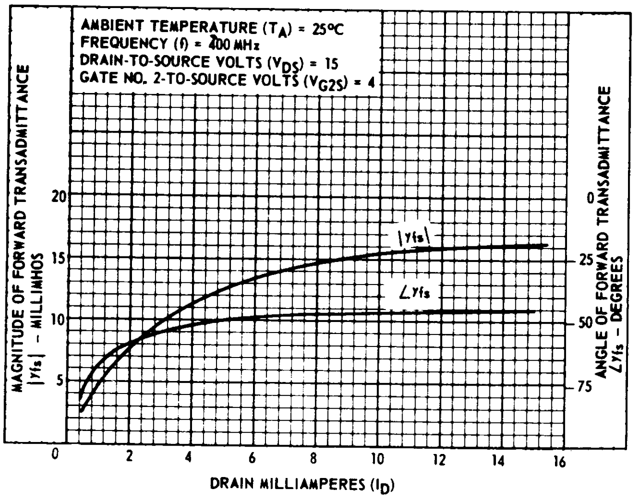


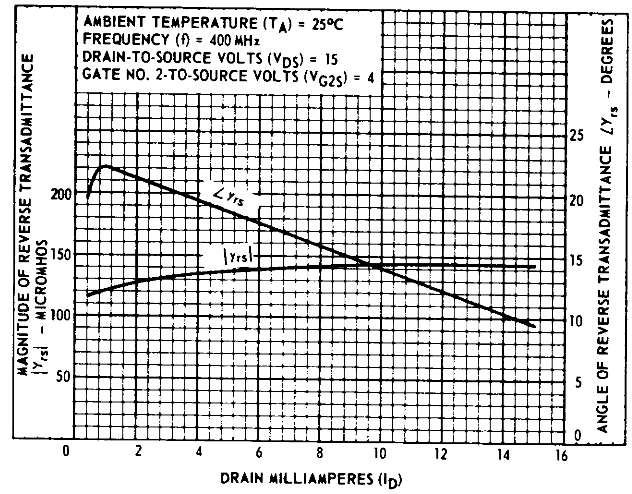
Fig. 11 - y_{os} vs. I_D

Typical y Parameters vs. I_D (cont'd)



92SS-4588

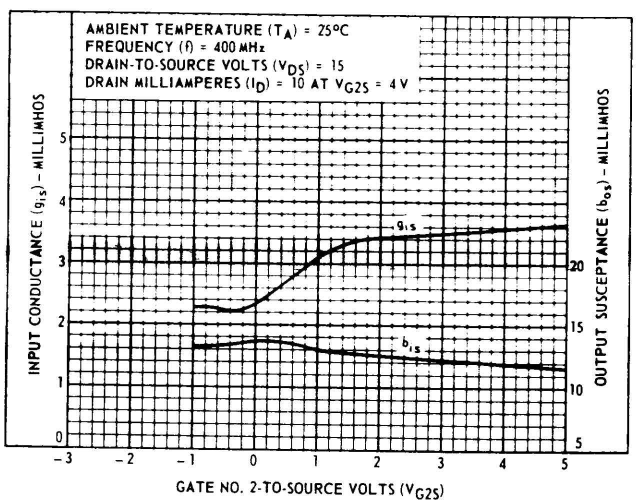
Fig. 12 - y_{fs} vs. I_D



92SS-4589

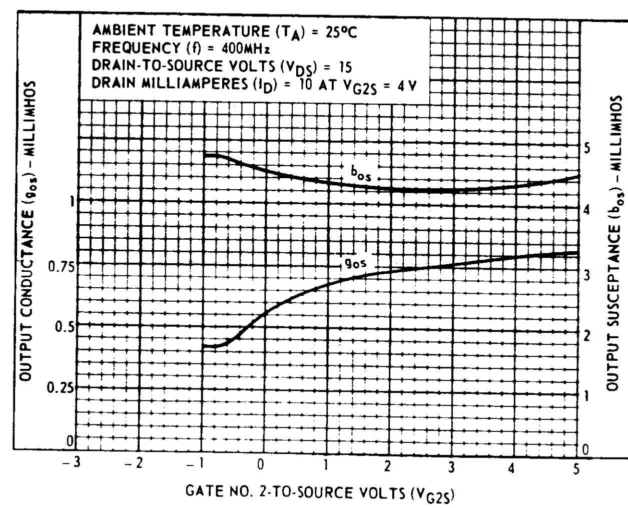
Fig. 13 - y_{rs} vs. I_D

Typical y Parameters vs. V_{G2S}



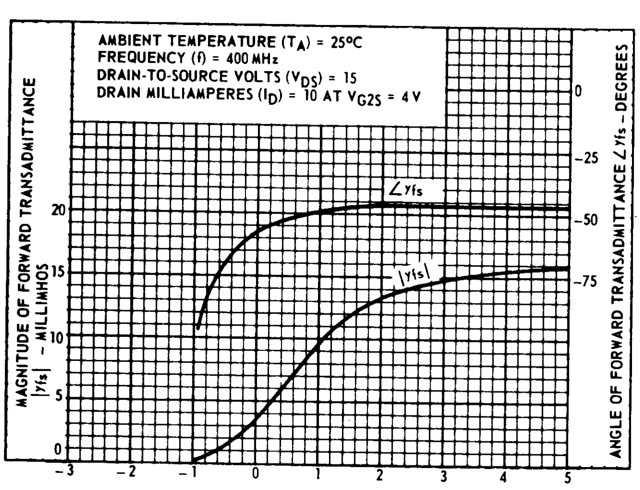
92SS-4590

Fig. 14 - y_{is} vs. V_{G2S}



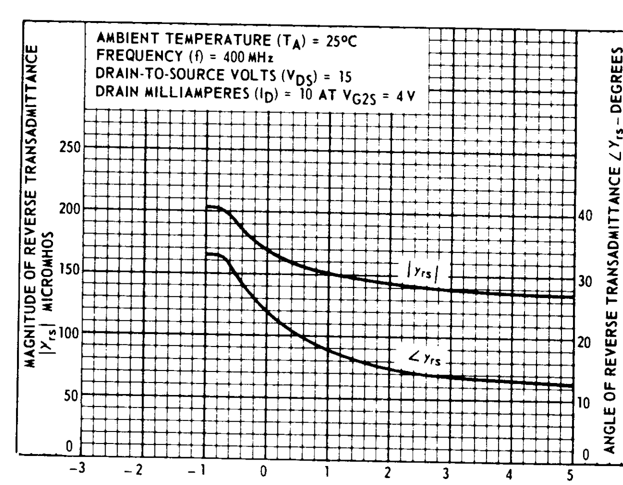
92SS-4591

Fig. 15 - y_{os} vs. V_{G2S}



92SS-4592

Fig. 16 - y_{fs} vs. V_{G2S}



92SS-4593

Fig. 17 - y_{rs} vs. V_{G2S}

Typical Characteristics

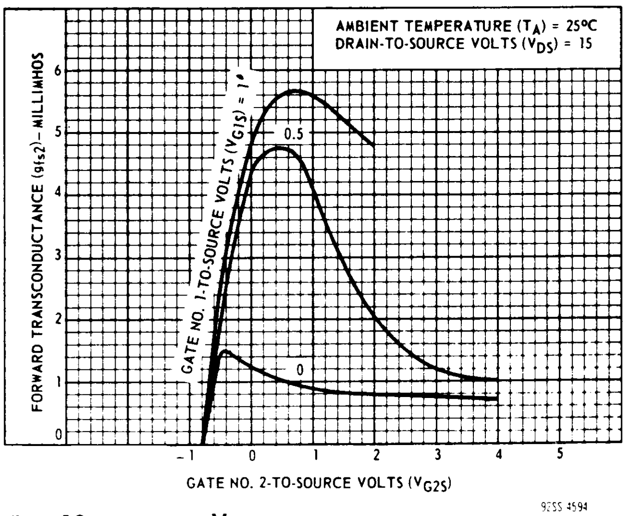


Fig. 18 - g_{fs2} vs. V_{G2S}

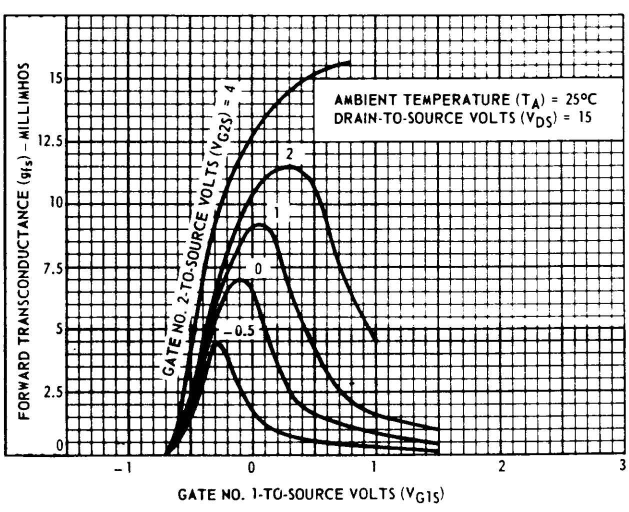


Fig. 19 - g_{fs} vs. V_{G1S}

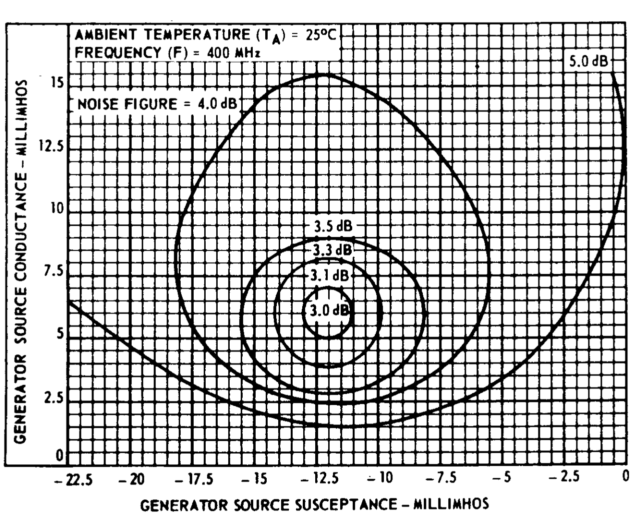
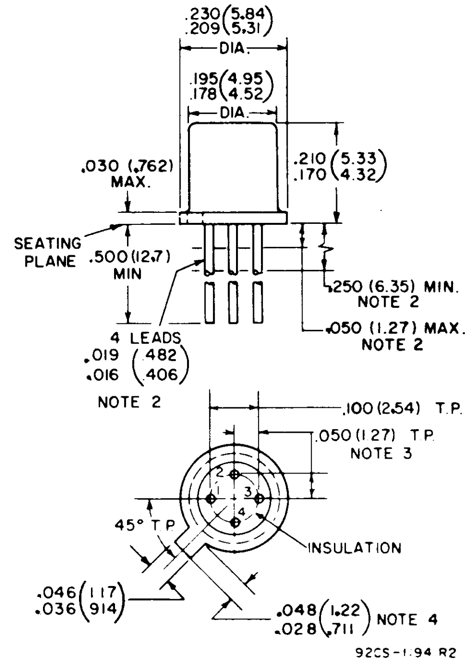


Fig. 20 - Noise figure vs. generator source admittance

DIMENSIONAL OUTLINE JEDEC TO-72



Dimensions in Inches and Millimeters

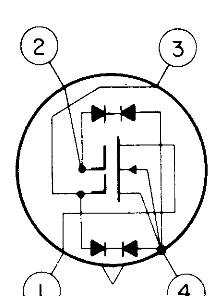
Note 1: *Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.*

Note 2: The specified lead diameter applies in the zone between 0.050" (1.27 mm) and 0.250" (6.35 mm) from the seating plane. From 0.250" (6.35 mm) to the end of the lead a maximum diameter of 0.021" (0.533 mm) is held. Outside of these zones, the lead diameter is not controlled.

Note 3: Leads having a maximum diameter of 0.019" (0.482 mm) at a guaging plane of 0.054" (1.372 mm) + 0.001" (0.025 mm) −0.000" (0.000 mm) below seating plane shall be within 0.007" (0.177 mm) at their true position (location) relative to a maximum width of tab.

Note 4: Measured from actual maximum diameter.

TERMINAL DIAGRAM



LEAD 1 - DRAIN
LEAD 2 - GATE No. 2
LEAD 3 - GATE No. 1
LEAD 4 - SOURCE, SUBSTRATE AND CASE