GENERAL DESCRIPTION

These devices are a dual P-channel, silicon, tetrode, insulated gate, enhancement-type, field-effect transistors designed primarily for low power chopper and switching applications. These devices include a shunting resistor diode network connected between the gate and body.

DUAL MATCHED P-CHANNEL ENHANCEMENT MODE MOS FETS (DIODE PROTECTED)

3N147 3N148

ABSOLUTE MAXIMUM RATINGS (Note 2)

Maximum Temperatures

Operating Junction Temperature	−65°C to +175°C
Storage Temperature	−65°C to +200°C
Lead Temperature (Soldering, 10 sec time limit)	+300°C

Maximum Power Dissipation (Note 3)

Total Dissipation at 25°C Case Temperature	1.7W
at 25°C Ambient Temperature	0.6 W

Maximum Voltages and Currents

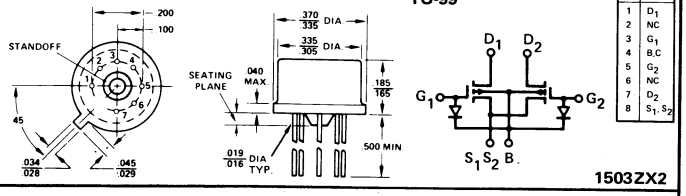
$V_{GS(f)}$	Forward Gate to Bulk Voltage	−50 V
V_{DB}	Drain to Bulk Voltage	−30 V
V_{SB}	Source to Bulk Voltage	−30 V
I_G	Gate Current	10 mA
I_D	Drain Current	200 mA
I_S	Source Current	200 mA
I_B	Bulk Current	200 mA

FEATURES

- Integrated Gate Protection Circuit (Note 1)
- Low On-Resistance $r_{ds(on)}$ = 500 Ω (Max)
- Low Leakage $I_{D(off)}$ = 0.5 nA (Max)

PACKAGE DIMENSIONS

TO-99



PIN	OUT
1	D_1
2	NC
3	G_1
4	B,C
5	G_2
6	NC
7	D_2
8	S_1, S_2

1503ZX2

ELECTRICAL CHARACTERISTICS (Each Side, 25°C Free Air Temperature unless otherwise noted)

	PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS
$V_{GB(f)}$	Forward Gate Voltage (Note 4)		−50			V	I_G = 10 mA $V_{DB} = V_{SB} = 0$
$V_{(BR)DB}$	Drain to Bulk Breakdown Voltage		−30			V	I_D = 10 μA $V_{GB} = V_{SB} = 0$
$V_{(BR)SB}$	Source to Bulk Breakdown Voltage		−30			V	I_S = 10 μA $V_{GB} = V_{DB} = 0$
$I_{D(off)}$	Drain Off Current	3N147		1.0	5.0	nA	V_{DB} = −20 V $V_{GB} = V_{SB} = 0$
		3N148		0.1	0.5	nA	V_{DB} = −20 V $V_{GB} = V_{SB} = 0$
$I_{S(off)}$	Source Off Current	3N147		2.0	10	nA	V_{SB} = −20 V $V_{GB} = V_{DB} = 0$
		3N148		0.2	1.0	nA	V_{SB} = −20 V $V_{GB} = V_{DB} = 0$
$I_{G(f)}$	Gate Forward Current			0.03	1.0	nA	V_{GB} = −40 V $V_{DB} = V_{SB} = 0$
$V_{GS(th)}$	Gate to Source Threshold Voltage		−2.0	−3.6	−6.0	V	I_D = 10 μA V_{DS} = −20 V $V_{BS} = 0$
$V_{GS(th)}$	Gate to Source Threshold Voltage		−3.0	−6.8	−12	V	I_D = 10 μA V_{DS} = −20 V V_{BS} = 5.0 V
$V_{GS(th)}$	Gate to Source Threshold Voltage		−4.0	−8.0	−15	V	I_D = 10 μA V_{DS} = −20 V V_{BS} = 10 V
$I_{D(on)}$	On-state Drain Current		8.0	22		mA	V_{DS} = −20 V V_{GS} = −15 V $V_{BS} = 0$
$V_{DS(on)}$	Drain to Source On-state Voltage			−1.2	−2.5	V	I_D = 5.0 mA V_{GS} = −15 V $V_{BS} = 0$
$r_{ds(on)}$	Drain to Source On-state Resistance (f = 1.0 kHz)			205	500	Ω	V_G = −15 V $V_D = 0$ $V_S = 0$ $V_B = 0$
$r_{ds(on)}$	Drain to Source On-state Resistance (f = 1.0 kHz)			220	650	Ω	V_G = −25 V V_D = −5.0 V V_S = −5.0 V V_B = 5.0 V
$r_{ds(on)}$	Drain to Source On-state Resistance (f = 1.0 kHz)			270	800	Ω	V_G = −30 V V_D = −10 V V_S = −10 V V_B = 10 V

ELECTRICAL CHARACTERISTICS (Each Side, 25°C Free Air Temperature unless otherwise noted)

	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS	
C_d	Drain Capacitance (f = 1.0 MHz)		8.0	12	pF	$V_{DB} = 0$	$V_{SB} = V_{GB} = 0$
C_s	Source Capacitance (f = 1.0 MHz)		14	20	pF	$V_{SB} = 0$	$V_{DB} = V_{GB} = 0$
C_g	Gate Capacitance (f = 1.0 MHz)		4.2	6.0	pF	V_{GB} = −40 V	$V_{DB} = V_{SB} = 0$
C_{dg}	Drain to Gate Capacitance (f = 1.0 MHz)		0.8	2.0	pF	$V_{DG} = 0$	$V_{BS} = 0$
C_{sg}	Source to Gate Capacitance (f = 1.0 MHz)		0.8	2.0	pF	$V_{SG} = 0$	$V_{BS} = 0$
$t_{d(on)}$	Turn On Delay Time		4.0	20	ns	V_{DD} = −17.5 V	$I_{D(on)}$ = 5.0 mA
t_r	Rise Time		30	100	ns	$V_{GS(on)}$ = −15 V	$V_{GS(off)} = 0$
$t_{d(off)}$	Turn Off Delay Time		6.0	30	ns	R_G = 50 Ω	
t_f	Fall Time		100	150	ns		
$I_{D(off)(125°C)}$	Drain Off Current	3N147	1.0	5.0	μA	V_{DB} = −20 V	$V_{GB} = V_{SB} = 0$
		3N148	0.1	0.5	μA	V_{DB} = −20 V	$V_{GB} = V_{SB} = 0$
$I_{S(off)(125°C)}$	Source Off Current	3N147	2.0	10	μA	V_{SB} = −20 V	$V_{GB} = V_{DB} = 0$
		3N148	0.2	1.0	μA	V_{SB} = −20 V	$V_{GB} = V_{DB} = 0$
$I_{G(f)(125°C)}$	Gate Forward Leakage Current		0.03	1.0	μA	V_{GB} = −40 V	$V_{DB} = V_{SB} = 0$
$r_{ds(on)(125°C)}$	Drain to Source On Resistance (f = 1.0 kHz)		345	850	Ω	V_G = −15 V	$V_D = 0$ $V_S = 0$ $V_B = 0$
$r_{ds(on)(125°C)}$	Drain to Source On Resistance (f = 1.0 kHz)		0.36	1.1	kΩ	V_G = −25 V	V_D = −5.0 V V_S = −5.0 V V_B = 5.0 V
$r_{ds(on)(125°C)}$	Drain to Source On Resistance (f = 1.0 kHz)		0.32	1.35	kΩ	V_G = −30 V	V_D = −10 V V_S = −10 V V_B = 10 V

NOTES:

1. The Integrated Gate Protection Circuit consists of a diffused resistor-diode network which protects the gate of the MOS-FET from accidental damage due to voltage transients.
2. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
3. These ratings give a maximum junction temperature of 175°C and junction to case thermal resistance of 88.2°C/Watt (derating factor of 11.3 mW/°C); junction to ambient thermal resistance of 250°C/Watt (derating factor of 4.0 mW/°C).
4. Pulse Condition: Pulse width ≤ 1.0 ms; Duty Cycle = 1%.