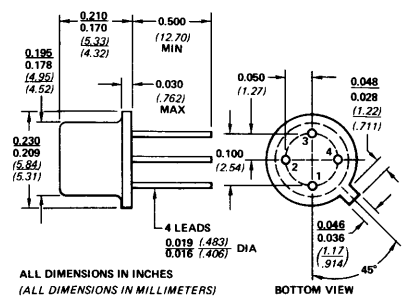
Performance Curves MABD
See Page 4-2

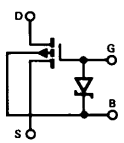
P-CHANNEL ENHANCEMENT-TYPE SILICON MOS FIELD-EFFECT TRANSISTOR

NORMALLY-OFF MOS FETS FOR ANALOG AND DIGITAL SWITCHING APPLICATIONS

- **Zener Clamp Protects the Gate**
- **$r_{DS(on)} < 20\ \Omega$ (3N167)**
- **$I_{D(off)} < 500$ pA**



TO-72
Body & Case Connected Internally



PIN	OUT
1	D
2	G
3	B C
4	S

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source or Gate-Source Voltage 3N167 ..... -30 V
Drain-Source or Gate-Source Voltage 3N168 ..... -25 V
Gate Current (Forward Direction for Zener Clamp). +0.1 mA
Storage Temperature ..... -65 to +150°C
Operating Junction Temperature ..... -55 to +125°C
Total Device Dissipation
(Derate 2.25 mW/°C to 125°C) ..... 225 mW

*ELECTRICAL CHARACTERISTICS (25°C and V_{BS} = 0 unless otherwise noted)

		Characteristics		3N167 Min	3N167 Max	3N168 Min	3N168 Max	Unit	Test Conditions	
1		BV_{DSS}	Drain-Source Breakdown Voltage	-30		-25		V	I_D = -1 μA, V_{GS} = 0	
2		BV_{SDS}	Source-Drain Breakdown Voltage	-30		-25		V	I_S = -1 μA, V_{GD} = V_{BD} = 0	
3		BV_{GBS}	Gate-Body Breakdown Voltage	-30	-85	-25	-85	V	I_G = -10 μA, V_{SB} = V_{DB} = 0	
4	STATIC	I_{GSS}	Gate-Body Leakage Current		-0.1		-0.5	nA	V_{GS} = -20 V, V_{DS} = 0	
5	STATIC	I_{GSS}	Gate-Body Leakage Current		-20		-200	nA	V_{GS} = -20 V, V_{DS} = 0	100°C
6	STATIC	$I_{D(off)}$	Drain Cutoff Current		-0.5		-1	nA	V_{DS} = -20 V, V_{GS} = 0	
7	STATIC	$I_{D(off)}$	Drain Cutoff Current		-200		-400	nA	V_{DS} = -20 V, V_{GS} = 0	100°C
8	STATIC	$I_{S(off)}$	Source Cutoff Current		-0.5		-1	nA	V_{SD} = -20 V, V_{GD} = 0, V_{BD} = 0	
9	STATIC	$I_{S(off)}$	Source Cutoff Current		-200		-400	nA	V_{SD} = -20 V, V_{GD} = 0, V_{BD} = 0	100°C
10	STATIC	$V_{GS(th)}$	Gate-Source Threshold Voltage	-2	-6	-2	-6	V	V_{DS} = -10 V, I_D = -10 μA	
11	STATIC	$I_{D(on)}$	On Drain Current (Note 1)	-200		-100		mA	V_{DS} = -20 V, V_{GS} = -20 V	
12	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance		20		40	Ω	I_D = -1 mA, V_{GS} = -20 V	
13	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance		25		50	Ω	I_D = -1 mA, V_{GS} = -20 V, V_{BS} = 10 V	
14	STATIC	$V_{DS(on)}$	Drain-Source ON Voltage		-20		-40	mV	I_D = -1 mA, V_{GS} = -20 V	
15	DYNAMIC	$r_{DS(on)}$	Drain-Source ON Resistance		20		40	Ω	V_{GS} = -20 V, I_D = 0	f = 1 kHz
16	DYNAMIC	C_{iss}	Common Source Input Capacitance		35		35	pF	V_{DS} = 0, V_{GS} = 0	f = 1 MHz
17	DYNAMIC	C_{rss}	Common Source Reverse Transfer Capacitance		12		12	pF	V_{DS} = 0, V_{GS} = 0	f = 1 MHz
18	DYNAMIC	C_{ds}	Drain-Source Capacitance		0.3		0.3	pF	V_{DS} = 0, V_{GS} = 0	f = 1 MHz
19	SW	t_d	Turn-ON Delay Time		8		8	ns	V_{DD} = -1.5 V,	
20	SW	t_r	Rise Time		6		6	ns	$I_{D(on)}$ = -10 mA (Note 3),	
21	SW	$t_{d(off)}$	Turn-OFF Delay Time		12		12	ns	$V_{GS(on)}$ = -20 V,	
22	SW	t_f	Fall Time		9		9	ns	$V_{GS(off)}$ = 0	

*JEDEC Registered Data

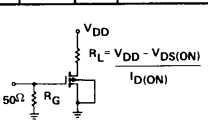
MABD

Notes:

1 Pulse test required, pulsewidth 200 μs duty cycle ≤ 3%

2 Due to symmetrical geometry, these units may be operated with source and drain leads interchanged

3 JEDEC registration in error.



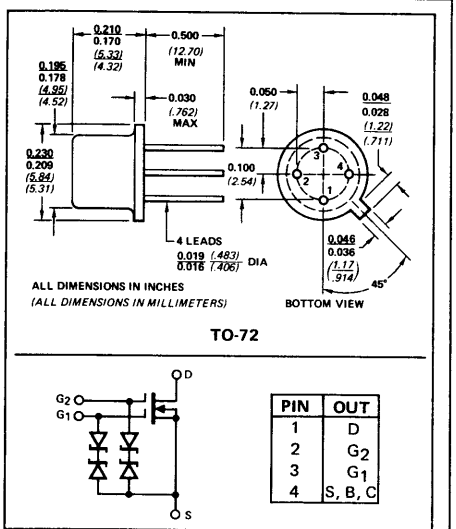
INPUT PULSE	SAMPLING SCOPE
RISE TIME 2 ns	RISE TIME 0.4 ns
FALL TIME 2.8 ns	INPUT RESISTANCE 10 MΩ
PULSE WIDTH 20 ns	INPUT CAPACITANCE 1.5 pF
PULSE RATE 550 pps	

Performance Curves MCB
See Page 4-11

N-CHANNEL DUAL GATE DEPLETION TYPE SILICON MOS FIELD-EFFECT TRANSISTOR

VHF AMPLIFIER-MIXER-IF AMPLIFIER

- High g_{fs} - Typically 12 mmhos
- Low C_{rss} — .03 pF max
- Monolithic Gate Protection Diodes



TO-72

PIN	OUT
1	D
2	G_2
3	G_1
4	S, B, C

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Gate Voltage	20 V
Gate Current, Forward & Reverse	1 mA
Drain-to-Source Voltage	20 V
Drain Current, Continuous	50 mA
Device Dissipation Case Temperature - 25°C	1.2 W
Free Air Temperature up to 25°C	360 mW
Free Air Temperature above 25°C derate linearly	2.2 mW/°C
Storage Temperature Range	-65 to +200°C
Lead Temperature 1/16" From Case for 10 Seconds	300°C

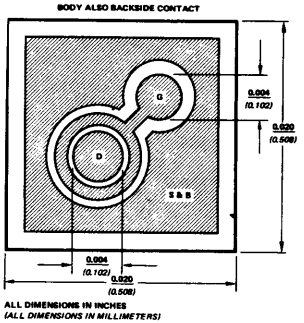
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{G1SS}	Gate One to Source Leakage Current			±50	nA	V_{G1S} = ±6 V, V_{G2S} = V_{DS} = 0	
2		I_{G2SS}	Gate Two to Source Leakage Current			±50		V_{G2S} = ±6 V, V_{G1S} = V_{DS} = 0	
3		I_{G1SS}	Gate One to Source Leakage Current			±5	µA	V_{G1S} = ±6 V, V_{G2S} = V_{DS} = 0	T_A = 100°C
4		I_{G2SS}	Gate Two to Source Leakage Current			±5		V_{G2S} = ±6 V, V_{G1S} = V_{DS} = 0	
5		BV_{G1SS}	Gate One to Source Breakdown Voltage	±6.5		±13	V	I_{G1} = ±100 µA, V_{G2S} = V_{DS} = 0	
6		BV_{G2SS}	Gate Two to Source Breakdown Voltage	±6.5		±13		I_{G2} = ±100 µA, V_{G1S} = V_{DS} = 0	
7		$V_{G1S(off)}$	Gate One to Source Cut-off Voltage	-.5		-4		V_{DS} = 15 V, V_{G2S} = 4 V, I_D = 50 µA	
8		$V_{G2S(off)}$	Gate Two to Source Cut-off Voltage	-.5		-4		V_{DS} = 15 V, V_{G1S} = 0, I_D = 50 µA	
9		I_{DS}	Zero Gate One Voltage Drain Current	5	15	30	mA	V_{DS} = 15 V, V_{G2S} = 4 V, V_{G1S} = 0	
10		g_{fs} (Note 2)	Common Source Forward Transconductance	7		18	mmho	V_{DS} = 15 V, V_{G2S} = 4 V, I_D = 10 mA	f = 1 kHz
11	DYN	C_{iss} (Note 1)	Common Source Input Capacitance		6		pF	V_{DS} = 15 V, V_{G2S} = 4 V, I_D = 10 mA	f = 1 MHz
12		C_{rss}	Common Source Reverse Transfer Capacitance		.02	.03			
13		C_{oss} (Note 1)	Common Source Output Capacitance		2.5				
14	HF	G_{ps} (Note 3)	Common Source Power Gain	16		22	dB	V_{DD} = 15 V, V_{G2S} = 4 V, I_D = 10 mA	f = 200 MHz
15		NF (Note 3)	Noise Figure			4.5			

MCB

* JEDEC Registered Data

Notes:
1 Non-JEDEC Registered Data 2 Pulse test 3 See figure 1



N-CHANNEL DEPLETION TYPE SILICON MOS FIELD-EFFECT TRANSISTOR

APPLICATIONS

- High and Low Frequency Amplifiers
- Ultra-High Input Impedance Amplifiers for such Circuits as:
  - Proximity Detectors
  - Smoke Detectors
  - Transducer Amplifiers
  - pH Detectors

PRINCIPAL DEVICES

2N3631 M100 M101

PACKAGE TYPE

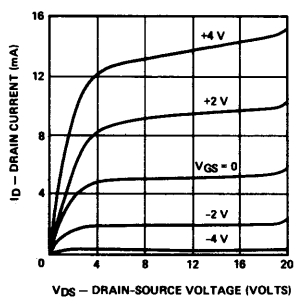
TO-18

FEATURES

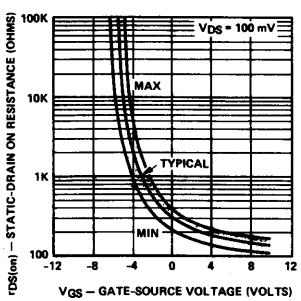
- No Gate Protective Diode Which Results In Ultra-High Input Impedance
- Ultra-Low Gate Leakage
- Normally ON

PERFORMANCE CURVES (25°C and V_{BS} = 0 unless otherwise noted)

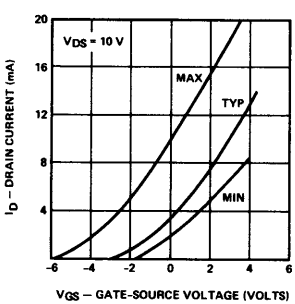
Output Characteristics



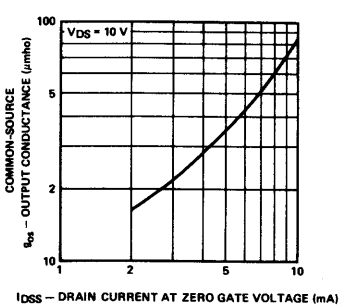
Drain-Source Static Resistance vs Gate-Source Bias



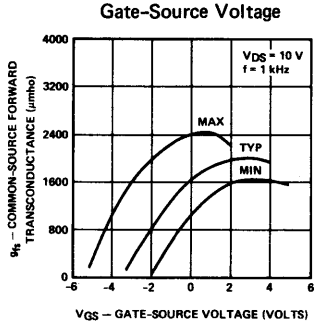
Transfer Characteristics

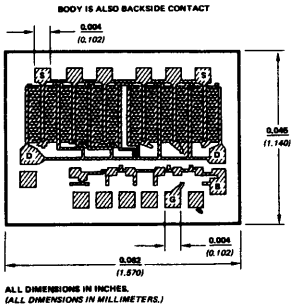


Output Conductance



Forward Transconductance vs Gate-Source Voltage





P-CHANNEL ENHANCEMENT-TYPE SILICON MOS FIELD-EFFECT TRANSISTOR

APPLICATIONS

- Analog and Digital Switching Circuits

PRINCIPAL DEVICES

3N167 3N168

FEATURES

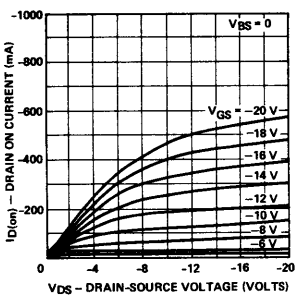
- Normally OFF
- Zener Clamp Protects the Gate
- $r_{DS(on)} < 20\ \Omega$ (3N167)
- $I_{D(off)} < 500$ pA

PACKAGE TYPE

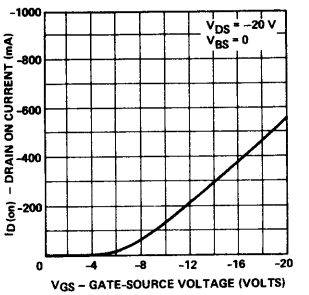
TO-72

PERFORMANCE CURVES (25°C unless otherwise noted)

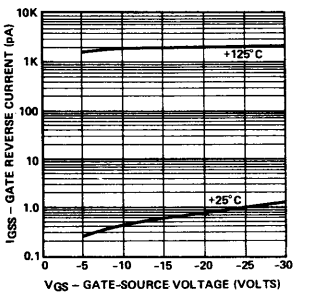
Output Characteristics



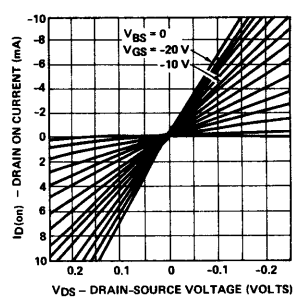
Transfer Characteristic



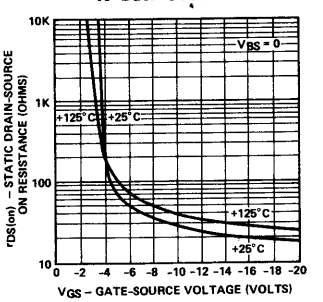
Gate Leakage Current vs Gate-Source Bias



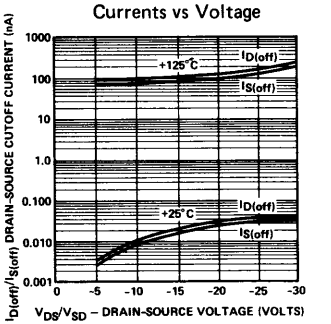
Low-Level Output Characteristics



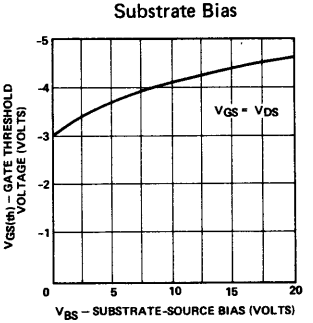
Drain-Source ON-State Resistance vs Gate-Source Bias



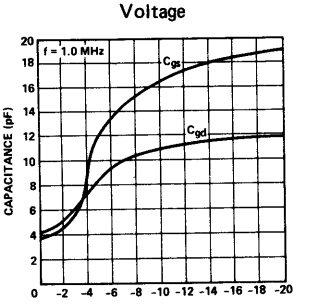
Source-Drain Leakage Currents vs Voltage



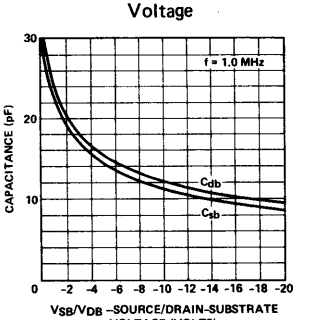
Gate Threshold Voltage vs Substrate Bias

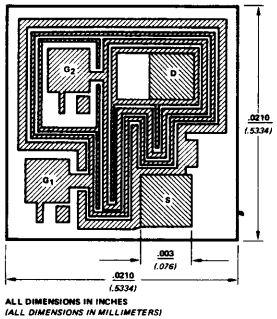


Gate Capacitance vs Voltage



Substrate Capacitance vs Voltage





N-CHANNEL DUAL GATE DEPLETION MODE SILICON MOS FIELD-EFFECT TRANSISTOR

APPLICATIONS

- VHF Amplifiers, Mixer & IF Amplifiers

PRINCIPAL DEVICES

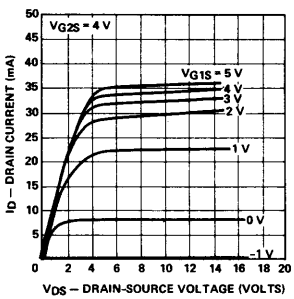
3N187 3N201-3

PACKAGE TYPE

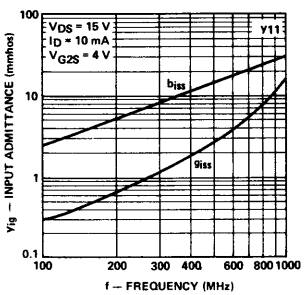
TO-72

PERFORMANCE CURVES (25°C unless otherwise noted)

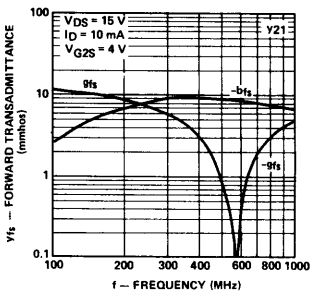
Output Characteristics



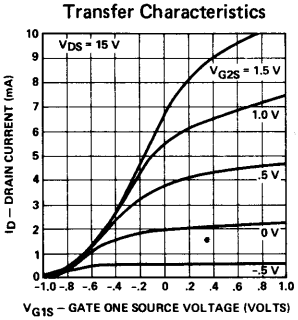
Common-Source Input Admittance vs Frequency



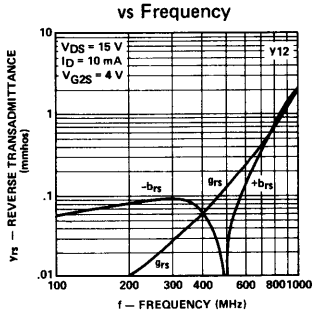
Common-Source Forward Transadmittance vs Frequency



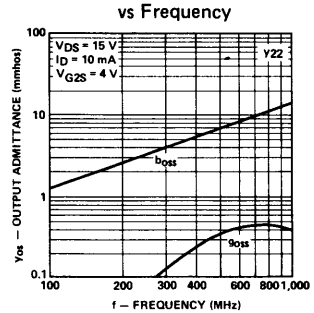
Transfer Characteristics



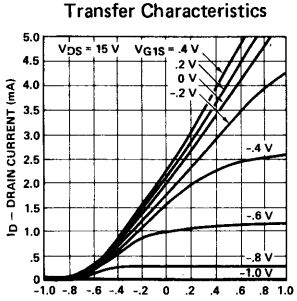
Common-Source Reverse Transadmittance vs Frequency



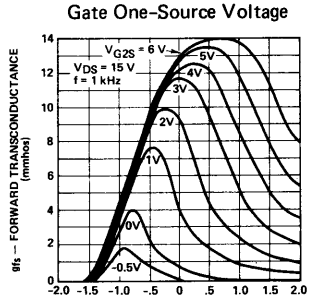
Common-Source Output Admittance vs Frequency



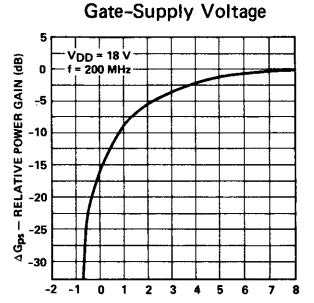
Transfer Characteristics



Forward Transconductance vs Gate One-Source Voltage



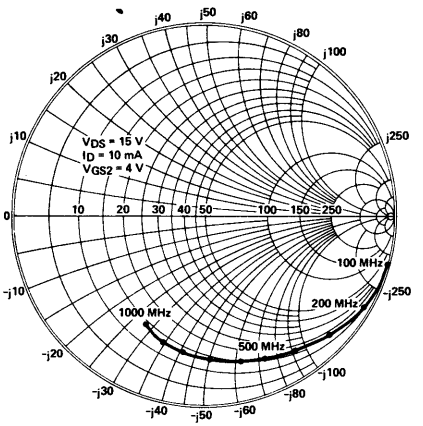
Relative Power Gain vs Gain Control Gate-Supply Voltage



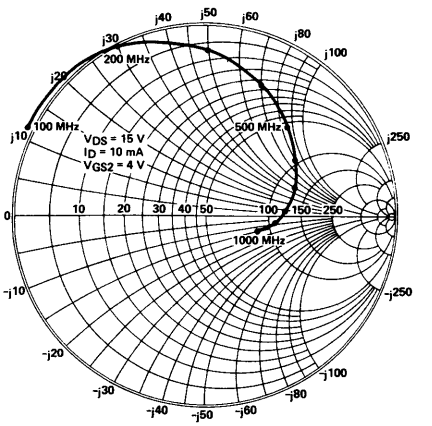
PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

S Parameters (Plotted on 50 ohm Smith Chart)

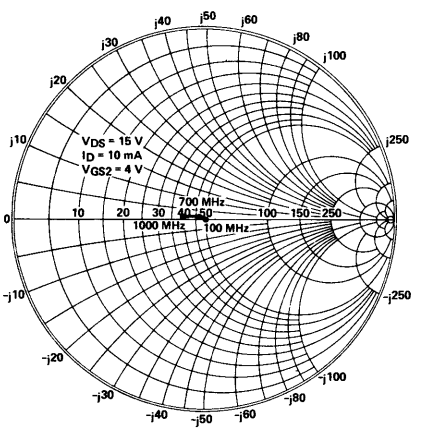
s11



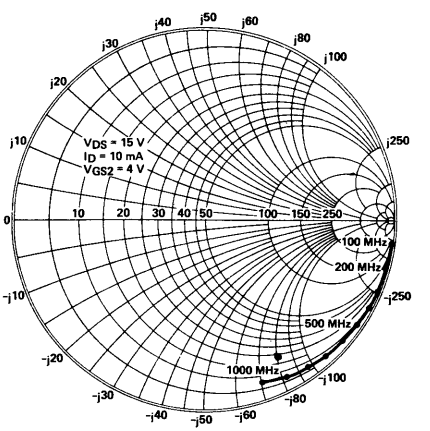
s21

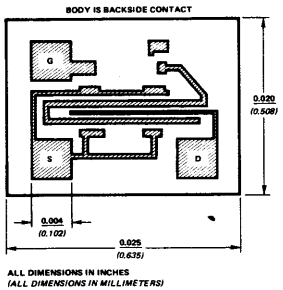


s12



s22





P-CHANNEL ENHANCEMENT-TYPE SILICON MOS FIELD-EFFECT TRANSISTOR

APPLICATIONS

- Audio and RF Amplifiers
- Analog Switches
- Logic Circuits
- Multiplexers

PRINCIPAL DEVICE

MEM511

PACKAGE TYPE

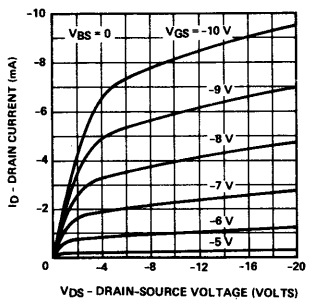
TO-72

FEATURES

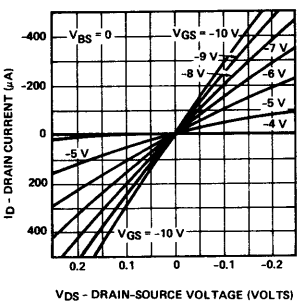
- $10^{10}\ \Omega$ Input Resistance
- Integrated Zener Clamp Protects the Gate
- Square Low Transfer Characteristics
- Normally OFF

PERFORMANCE CURVES (25°C unless otherwise noted)

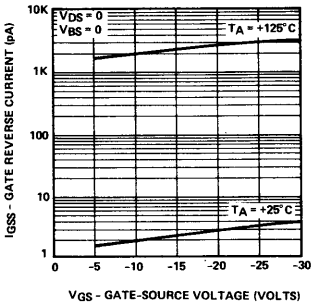
Output Characteristics



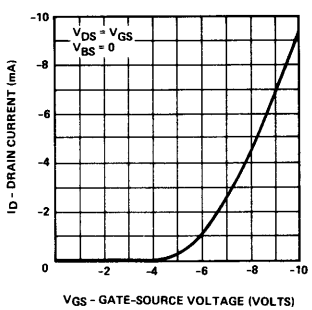
Low Voltage Output Characteristics



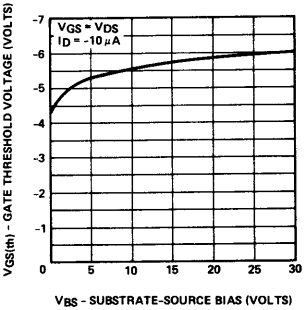
Gate Leakage Current vs Gate-Source Bias



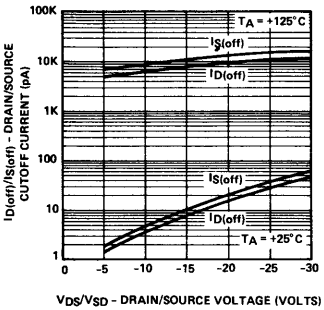
Transfer Characteristic



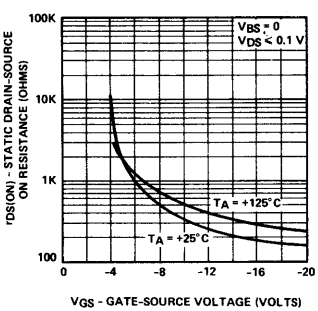
Gate Threshold Voltage vs Substrate Bias



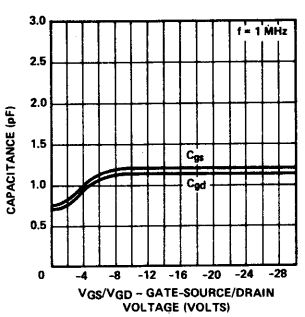
Source-Drain Leakage Currents vs Voltage



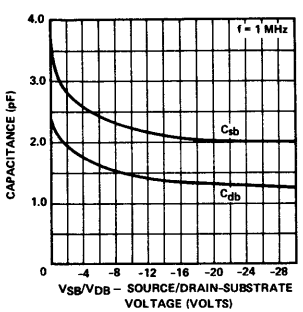
Drain-Source ON State Resistance vs Gate-Source Bias

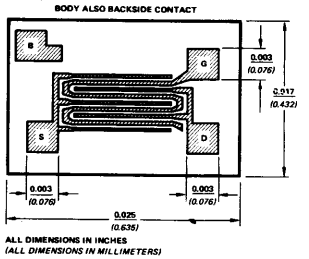


Gate Capacitance vs Voltage



Substrate Capacitance vs Voltage





P-CHANNEL ENHANCEMENT-TYPE SILICON MOS FIELD EFFECT TRANSISTOR

APPLICATIONS

- Analog and Digital Switching
- General Purpose Amplifiers

PRINCIPAL DEVICES

3N163 3N164

FEATURES

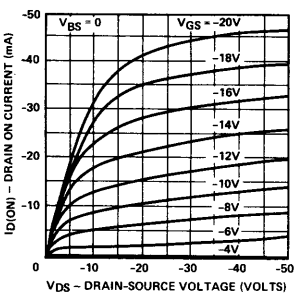
- High Gate Transient Voltage Breakdown Eliminates Need For Gate Protective Diode
- Ultra-High Input Impedance
- Low Leakage
- Normally OFF

PACKAGE TYPE

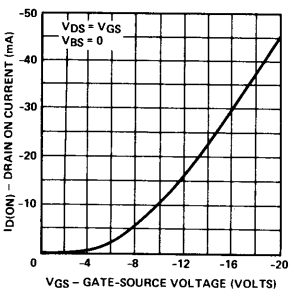
TO-72

PERFORMANCE CURVES (25°C unless otherwise noted)

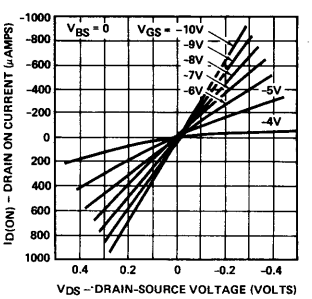
Output Characteristics



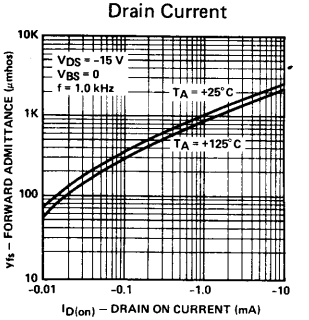
Transfer Characteristic



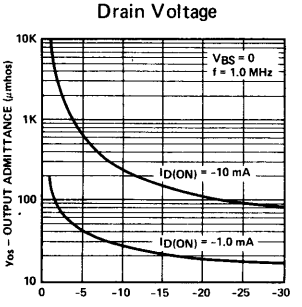
Low-Level Output Characteristics



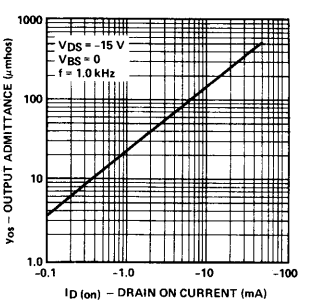
Common-Source, Short-Circuit, Forward Transadmittance vs Drain Current



Common-Source, Short-Circuit, Output Admittance vs Drain Voltage

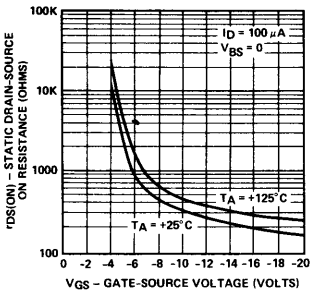


Common-Source, Short-Circuit, Output Admittance vs Drain Current

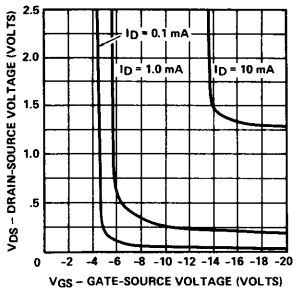


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

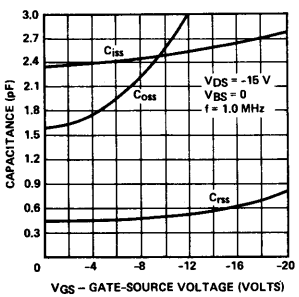
Drain-Source ON Resistance vs Gate-Source Voltage



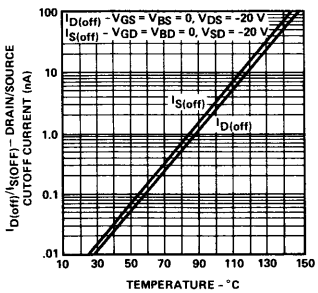
Low-Level "ON" Drain-Source Voltage vs Gate-Source Voltage

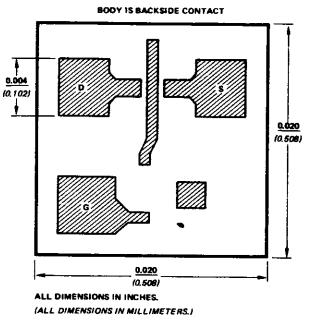


Capacitance vs Gate-Source Voltage



Drain-Source Leakage Current vs Temperature





P-CHANNEL ENHANCEMENT-TYPE SILICON MOS FIELD-EFFECT TRANSISTOR

APPLICATIONS

- Analog and Switching Circuits

PRINCIPAL DEVICE

M104

FEATURES

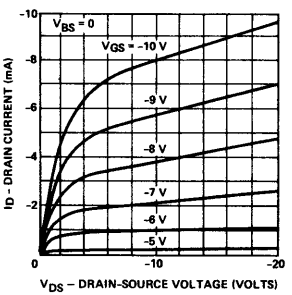
- Integrated Zener Clamp Protects the Gate
- C_{gs} Less Than 0.5 pF
- Very Low $I_{D(off)}$ and $I_{S(off)}$
- Normally OFF

PACKAGE TYPE

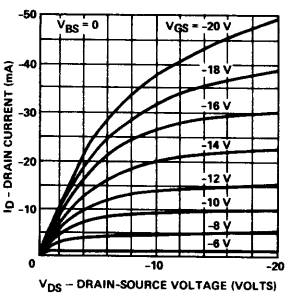
TO-72

PERFORMANCE CURVES (25°C unless otherwise noted)

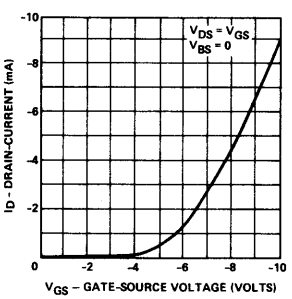
Output Characteristic



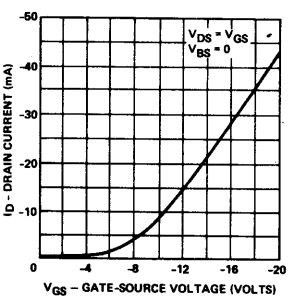
Output Characteristic



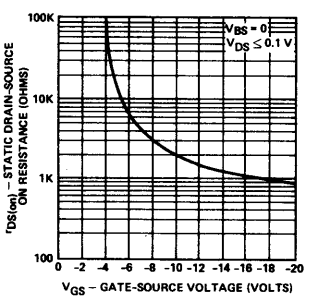
Transfer Characteristic



Transfer Characteristic



Drain-Source ON Resistance vs Gate-Source Bias



Gate Threshold Voltage vs Substrate Bias