BDW10, 10A
BDW12, 12A
BDW14, 14A
BDW16, 16A

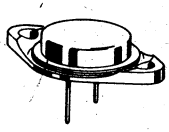
NPN SILICON POWER TRANSISTORS

The BDW10/10A, BDW12/12A, BDW14/14A, BDW16/16A are POWERBASE▲ transistors intended for general purpose use in professional and consumer applications.

The POWERBASE▲ process offers the following features:

- High Voltage Capabitily — V_{CEO} up to 160 V, V_{CBO} up to 200 V
- Large SOA — 180 W at V_{CE} = 60 Vdc
- High Gain — 25 min. at I_C = 5 Adc (A Version)
- High Stability and Reliability
  — Motorola patented photoglass passivation
- Excellent Thermal Efficiency for enhanced reliability
  $R_{\theta JC}$ = 0.97 °C/W Max.

15 AMPERES
NPN SILICON
POWER TRANSISTORS
100, 120, 140, 160 VOLTS
180 WATTS



MAXIMUM RATINGS

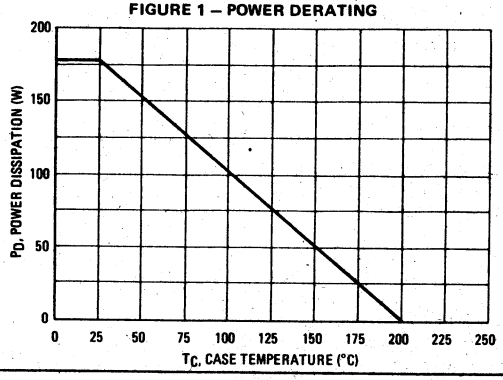
Rating	Symbol	BDW10 BDW10A	BDW12 BDW12A	BDW14 BDW14A	BDW16 BDW16A	Unit
Collector Emitter Voltage	V_{CEO}	100	120	140	160	Vdc
Collector Emitter Voltage	$V_{CER(sus)}$	120	140	160	180	Vdc
Collector Emitter Voltage	V_{CBO}	140	160	180	200	Vdc
Emitter Base Voltage	V_{EB}	8				Vdc
Collector Current — Continuous Peak[1]	I_C I_{CM}	15 20				Adc
Base Current — Continuous Peak[1]	I_B I_{BM}	5 10				Adc
Emitter Current — Continuous Peak[1]	I_E I_{EM}	20 30				Adc
Total Power Dissipation Derate above 25 °C	P_D	180 1.03				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200				°C

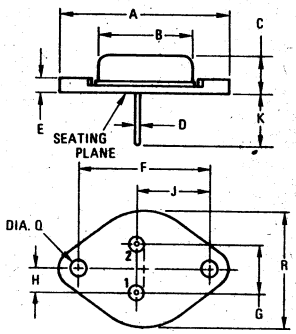
THERMAL CHARACTERISTICS

Characteristics	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.97	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	°C

[1] Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

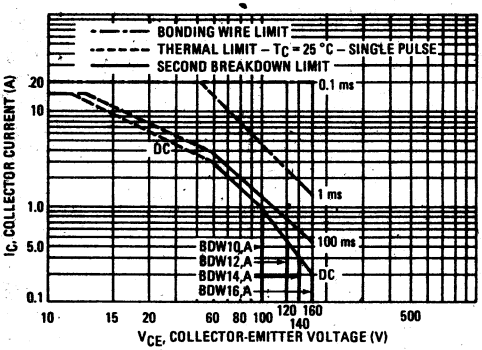
CASE 11-01
TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristics	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector Emitter Breakdown Voltage (I_C = 0.2 Adc, I_B = 0) BDW10,A	$V_{CEO(sus)}$	100		Vdc
BDW12,A		120		
BDW14,A		140		
BDW16,A		160		
Collector Emitter Sustaining Voltage (I_C = 0.2 Adc, R_{BE} = 100 Ω, L = 25 mH) BDW10,A	$V_{CER(sus)}$	120		Vdc
BDW12,A		140		
BDW14,A		160		
BDW16,A		180		
Collector Cutoff Current (V_{CB} = rated V_{CBO}, I_E = 0) T_C = 25 °C	I_{CBO}		0.1	mAdc
T_C = 125 °C			1	
Collector Cutoff Current (I_B = 0, V_{CE} = 50 V — BDW10,A; 60 V — BDW12,A; 70 V — BDW14,A; 80 V — BDW16,A)	I_{CEO}		0.1	mAdc
Collector Cutoff Current (V_{CE} = rated V_{CER}, R_{BE} = 100Ω	I_{CER}		10	mAdc
Emitter Cutoff Current (V_{BE}= 8 Vdc, I_C = 0)	I_{EBO}		1	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 60 Vdc, t = 0.5 sec.)	$I_{S/b}$	3		Adc
(V_{CE} = 100 Vdc, t = 0.5 sec.)		1		
ON CHARACTERISTICS[1]				
DC Current Gain I_C = 1 Adc BDW10, 12, 14, 16	h_{FE}	50		
BDW10A, 12A, 14A, 16A		100		
V_{CE} = 4 Vdc, I_C = 5 Adc BDW10, 12, 14, 16		20	100	
BDW10A, 12A, 14A, 16A		25	100	
I_C = 8 Adc BDW10, 12, 14, 16		10	50	
BDW10A, 12A, 14A, 16A		12	50	
I_C = 12 Adc All types		5		
Collector Emitter Saturation Voltage I_C = 5 Adc, I_B = 0.5 Adc BDW10, 12, 14, 16	$V_{CE(sat)}$		1.0	Vdc
BDW10A, 12A, 14A, 16A			0.8	
I_C = 8 Adc, I_B = 1.6 Adc BDW10, 12, 14, 16			1.5	
BDW10A, 12A, 14A, 16A			1.2	
Base Emitter On Voltage (I_C = 5 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$		1.5	Vdc
Base Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.5 Adc)	$V_{BE(sat)}$		1.6	Vdc
(I_C = 8 Adc, I_B = 1.6 Adc)			2.0	
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 100 kHz	f_T	1.0		MHz

[1] Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%

FIGURE 2 – FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistors: average junction temperature and second breakdown. Safe Operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation, i.e. the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on T_C = 25 °C; $T_{J(pk)}$ is variable depending on power level.

Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures thermal limitations will reduce the power that can be handled to value less than the limitations imposed by second breakdown. (See Motorola Application Note AN-415.)

FIGURE 3 – DC CURRENT GAIN

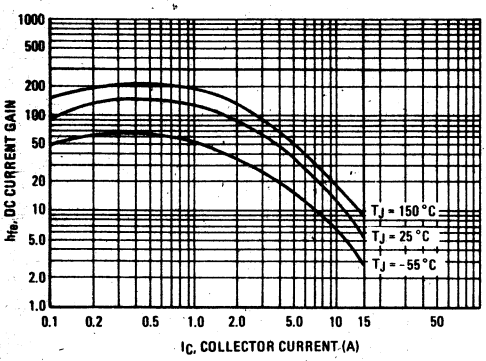


FIGURE 4 – COLLECTOR SATURATION REGION

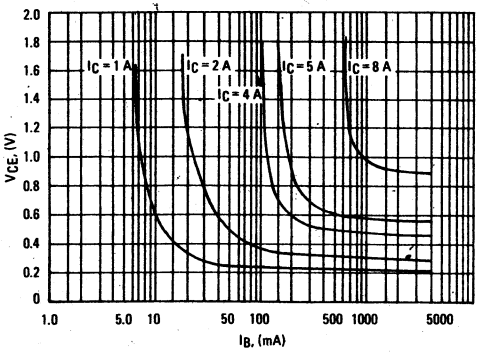


FIGURE 5 – "ON" VOLTAGES

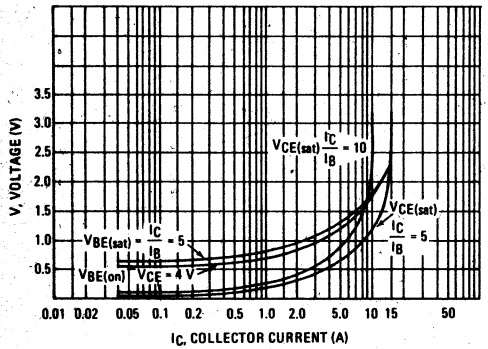


FIGURE 6 – CURRENT GAIN–BANDWIDTH PRODUCT

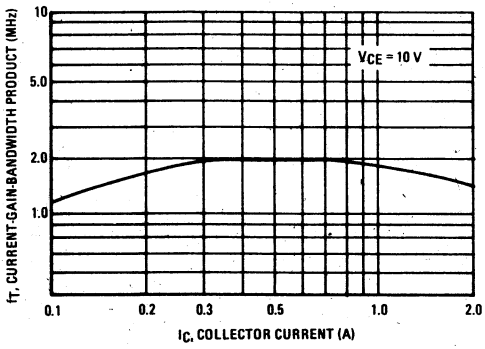


FIGURE 7 – SWITCHING TIMES TEST CIRCUIT

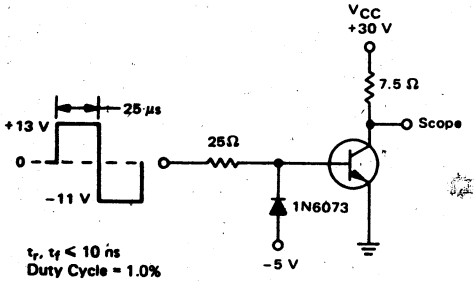


FIGURE 8 – TURN-ON TIME

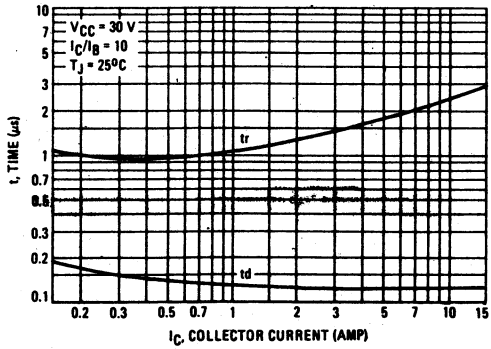


FIGURE 9 – TURN-OFF TIMES

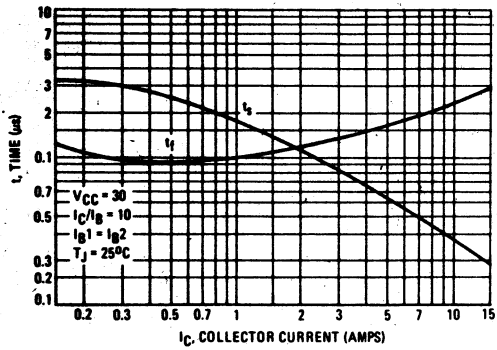


FIGURE 10 – CAPACITANCES

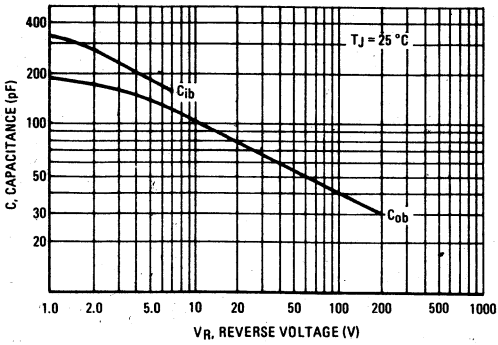
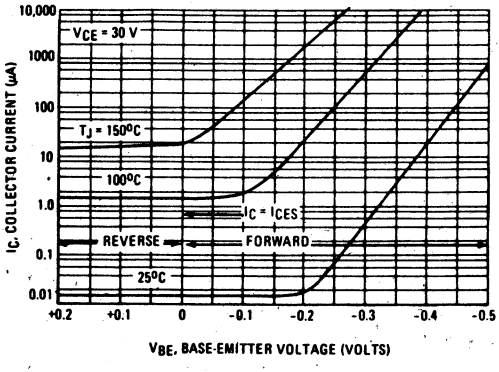


FIGURE 11 – COLLECTOR CUT-OFF REGION



BDW30
BDW32
BDW34
BDW36

NPN SILICON POWER TRANSISTORS

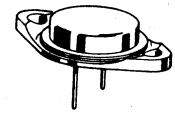
The BDW30, 32, 34, 36 are POWERBASE▲ transistors intended for use in high current/high power professional and consumer applications.

The devices feature:

- High Voltage Capability V_{CEO} up to 160 V, V_{CBO} up to 190 V
- Large SOA 250 W at 60 V
- Excellent thermal efficiency $R_{\theta JC}$ = 0.7 °C/W
- High stability and reliability Motorola patented photoglass passivation

NPN SILICON POWER TRANSISTORS

30 AMPERE
100, 120, 140, 160 VOLTS
250 WATTS



MAXIMUM RATINGS

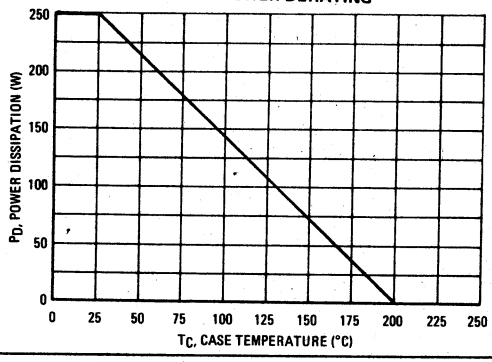
Rating	Symbol	BDW30	BDW32	BDW34	BDW36	Unit
Collector Emitter Voltage	$V_{CEO(sus)}$	100	120	140	160	Vdc
Collector Emitter Voltage	$V_{CER(sus)}$	120	140	160	180	Vdc
Collector Emitter Voltage	V_{CBO}	140	160	180	200	Vdc
Emitter Base Voltage	V_{EB}	8				Vdc
Collector Current — Continuous Peak[1]	I_C I_{CM}	30 40				Adc
Base Current — Continuous Peak[1]	I_B I_{BM}	10 20				Adc
Emitter Current — Continuous Peak[1]	I_E I_{EM}	40 60				Adc
Total Power Dissipation Derate above 25 °C	P_D	250 1.43				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200				°C

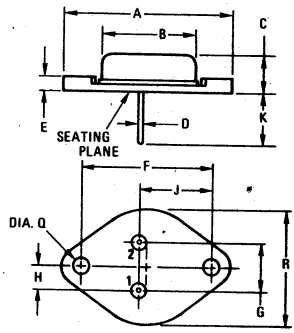
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	°C

[1] Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050

CASE 11-01
TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector Emitter Breakdown Voltage (I_C = 0.3 Adc, I_R = 0, L = 25 mH) BDW30	$V_{CEO(sus)}$	100		Vdc
BDW32		120		
BDW34		140		
BDW36		160		
Collector Emitter Sustaining Voltage (I_C = 0.3 Adc, R_{BE} = 100Ω, L = 25 mH) BDW30	$V_{CER(sus)}$	120		Vdc
BDW32		140		
BDW34		160		
BDW36		180		
Collector Cutoff Current (V_{CB} = rated V_{CBO}, I_E = 0) T_C = 25 °C	I_{CBO}		0.2	mAdc
T_C = 125 °C			2	
Collector Cutoff Current (I_B = 0, V_{CE} = 50 V) BDW30	I_{CEO}		0.2	mAdc
V_{CE} = 60 V) BDW32				
V_{CE} = 70 V) BDW34				
V_{CE} = 80 V) BDW36				
Collector Cutoff Current (V_{CE} = rated V_{CER}, R_{BE} = 100Ω	I_{CER}		20	mAdc
Emitter Cutoff Current (V_{BE} = 8 Vdc, I_C = 0)	I_{EBO}		2	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 60 Vdc, t = 0.5 sec.)	$I_{s/b}$	4.17		Adc
ON CHARACTERISTICS[1]				
DC Current Gain (V_{CE} = 4 Vdc, I_C = 2A)	h_{FE}	50		
I_C = 8A)		20	100	
I_C = 16A)		8		
Collector Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc)	$V_{CE(sat)}$		1.2	Vdc
(I_C = 16 Adc, I_B = 3.2 Adc)			1.7	
Base Emitter On Voltage (I_C = 10 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$		1.6	Vdc
Base Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc)	$V_{BE(sat)}$		1.6	Vdc
(I_C = 16 Adc, I_B = 3.2 Adc)			2.1	
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 2 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz.	f_T	1.0		MHz

[1] Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

FIGURE 2 – "ON" VOLTAGES

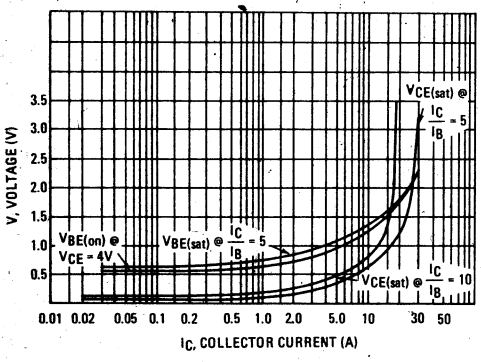


FIGURE 3 – COLLECTOR SATURATION REGION

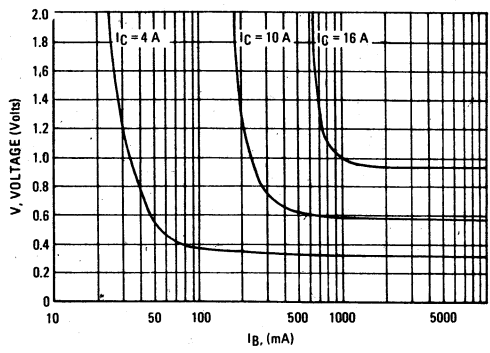
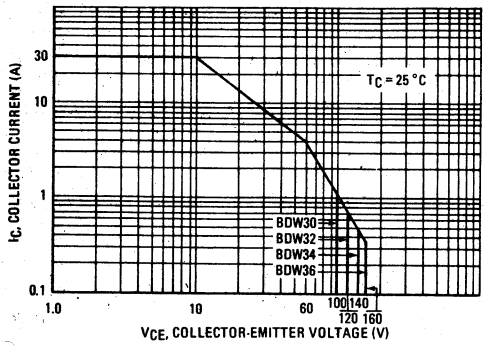


FIGURE 4 – ACTIVE REGION SAFE OPERATING AREA

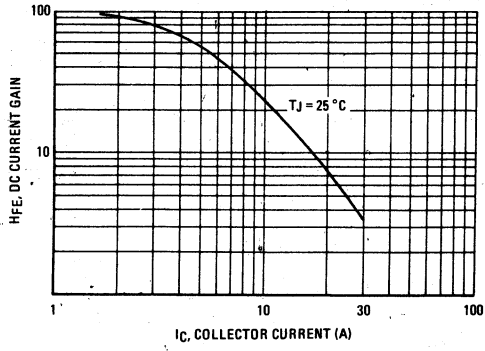


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 4 is based on $T_C = 25\,°C$; $T_{J(pk)}$ is variable depending on power level.

Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breadkown. (See Motorola Application Note AN-415.)

FIGURE 5 – DC CURRENT GAIN



BDW39 BDW44
BDW40 BDW45
BDW41 BDW46
BDW42 BDW47

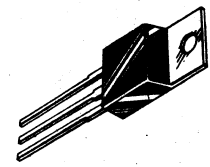
DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general purpose and low speed switching applications.

- High DC Current Gain — h_{FE} = 2500 (typ.) @ I_C = 5.0 Adc.
- Collector Emitter Sustaining Voltage @ 30 mAdc:
  $V_{CEO(sus)}$ = 45 Vdc (min.) — BDW39/BDW44
  60 Vdc (min.) — BDW40/BDW45
  80 Vdc (min.) — BDW41/BDW46
  100 Vdc (min.) — BDW42/BDW47
- Low Collector Emitter Saturation Voltage:
  $V_{CE(sat)}$ = 2.0 Vdc (max.) @ I_C = 5.0 Adc
  3.0 Vdc (max.) @ I_C = 10.0 Adc
- Monolithic Construction with Built-In Base Emitter Shunt resistors
- TO-220AB Compact Package
- TO-66 Lead form also available ordered with "-66" suffix.

DARLINGTON 15 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS 45-60-80-100 VOLTS 85 WATTS



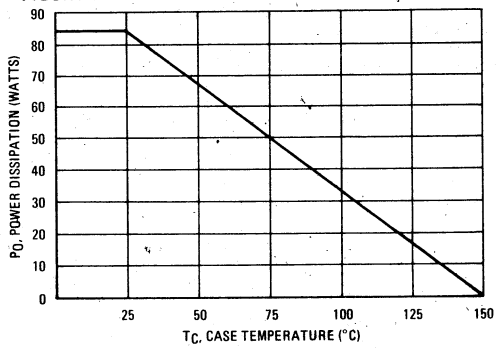
MAXIMUM RATINGS

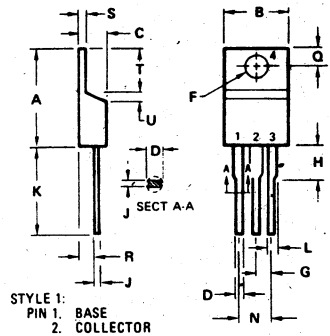
Rating	Symbol	BDW39 BDW44	BDW40 BDW45	BDW41 BDW46	BDW42 BDW47	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current - Continuous	I_C	15				Adc
Base Current	I_B	0.5				Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	85 0.68				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.47	°C/W

FIGURE 1 — POWER TEMPERATURE DERATING CURVE





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic		Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage[1]		$V_{CEO(sus)}$			Vdc
(I_C = 30 mAdc, I_B 0)	BDW39/BDW44		45		
	BDW40/BDW45		60		
	BDW41/BDW46		80		
	BDW42/BDW47		100		
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 22.5 Vdc, I_B = 0)	BDW39/BDW44			2	
(V_{CE} = 30 Vdc, I_B = 0)	BDW40/BDW45			2	
(V_{CE} = 40 Vdc, I_B = 0)	BDW41/BDW46			2	
(V_{CE} = 50 Vdc, I_B = 0)	BDW42/BDW47			2	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 45 Vdc, I_E = 0)	BDW39/BDW44			1	
(V_{CB} = 60 Vdc, I_E = 0)	BDW40/BDW45			1	
(V_{CB} = 80 Vdc, I_E = 0)	BDW41/BDW46			1	
(V_{CB} = 100 Vdc, I_E = 0)	BDW42/BDW47			1	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)				2	
ON CHARACTERISTICS[1]					
DC Current Gain		h_{FE}			–
(I_C = 5 Adc, V_{CE} = 4.0 Vdc)			1000		
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)			250		
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 5 Adc, I_B = 10 mAdc)				2	
(I_C = 10 Adc, I_B = 50 mAdc)				3	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 10 Adc, V_{CE} = 4 Vdc)				3	
SECOND BREAKDOWN[2]					
Second Breakdown Collector-Current With Base Forward Biased		$I_{S/b}$			Adc
BDW39/BDW40/BDW41/BDW42	V_{CE} = 28.4 Vdc		3		
	V_{CE} = 40 Vdc		1.2		
BDW44/BDW45/BDW46/BDW47	V_{CE} = 22.5 Vdc		3.8		
	V_{CE} = 36 Vdc		1.2		
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product[3]		f_T			MHz
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)			4.0		
Output Capacitance		C_{ob}			pF
V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	BDW39/40/41/42			200	
	BDW44/45/46/47			300	
Small Signal Current Gain		h_{fe}			–
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 KHz)			300		

[1] Pulse test: Pulse width = 300 μs, Duty cycle = 2.0%.
[2] Pulse test non repetitive pulse width: 250 ms.
[3] $f_T = |h_{fe}| \cdot f$ test.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

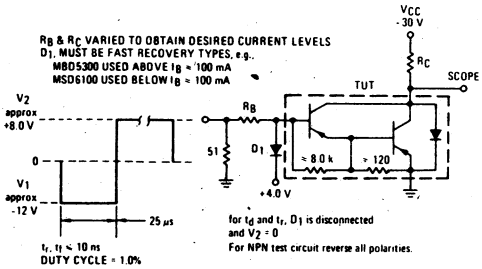


FIGURE 3 – SWITCHING TIMES

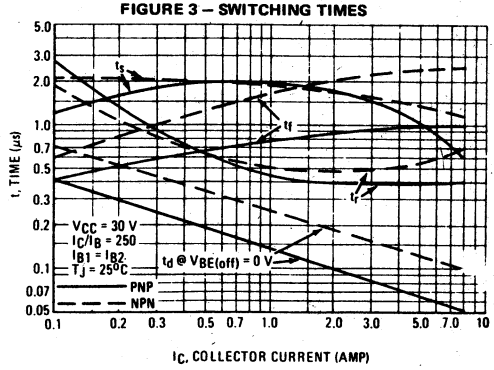
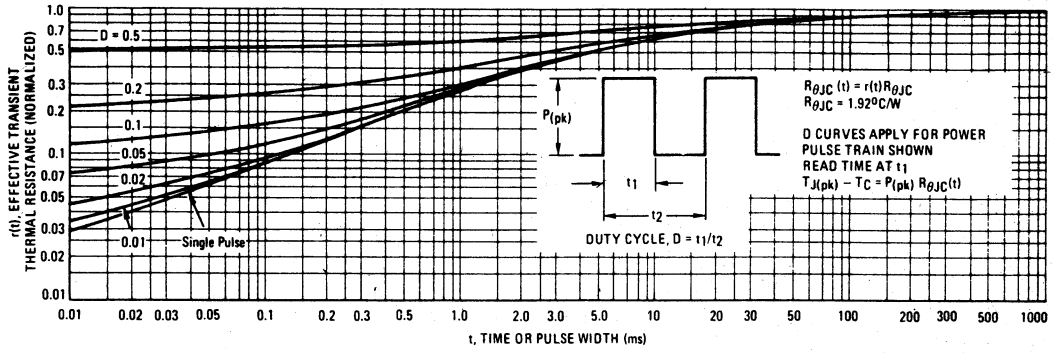


FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 – BDW39 THRU BDW42

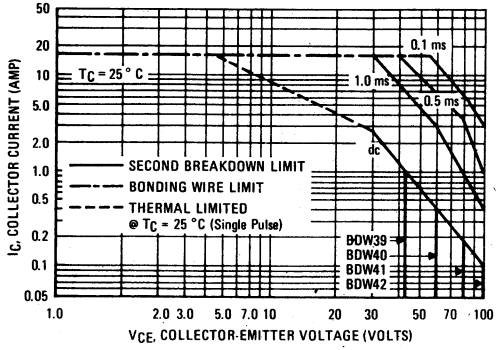
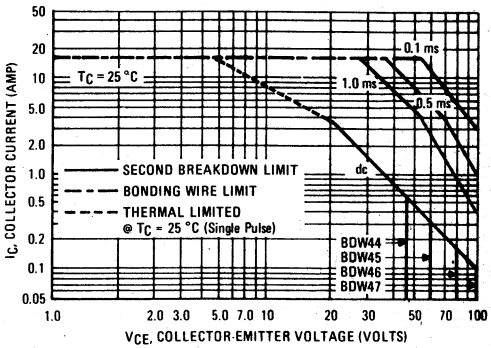


FIGURE 6 – BDW44 THRU GDW47



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Fig. 5 and 6 is based on $T_{J(pk)}$ = 200 °C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200$ °C. $T_{J(pk)}$ may be calculated from the data in Fig. 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See an-415).

FIGURE 7 – SMALL-SIGNAL CURRENT GAIN

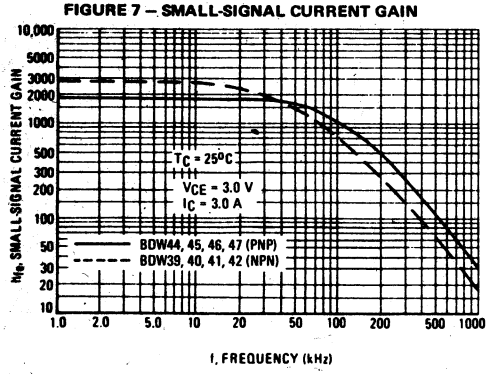
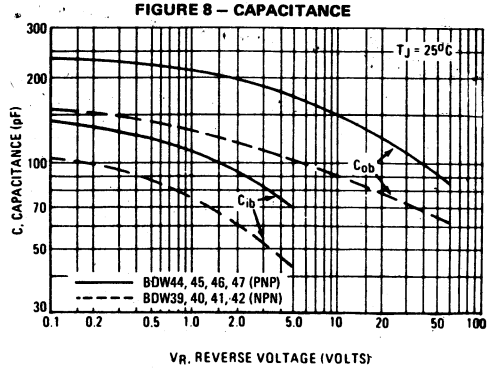


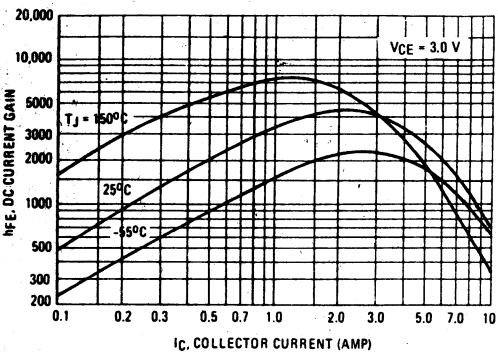
FIGURE 8 – CAPACITANCE



BDW39, 40, 41, 42 (NPN)

BDW44, 45, 46, 47 (PNP)

FIGURE 9 – DC CURRENT GAIN



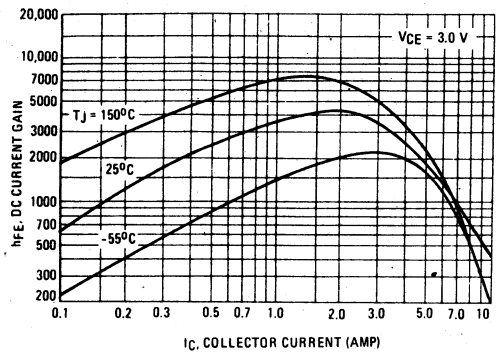
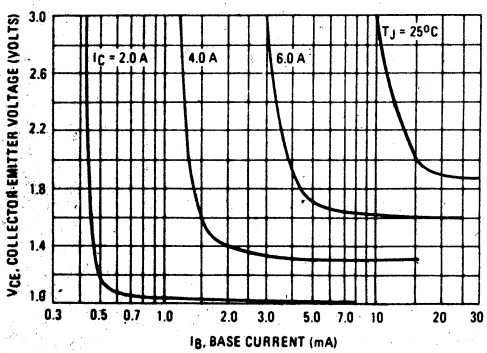
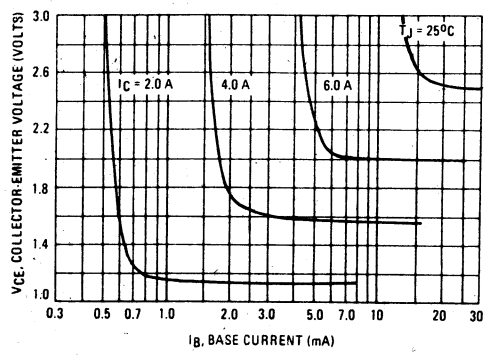


FIGURE 10 – COLLECTOR SATURATION REGION

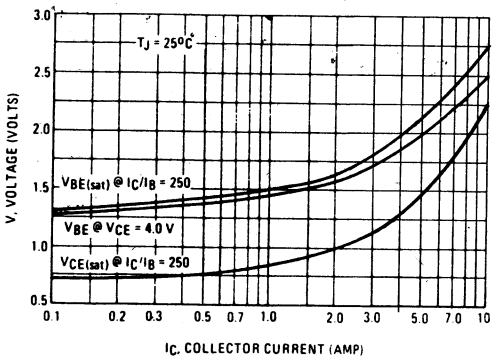




BDW39, 40, 41, 42 (NPN)

BDW44, 45, 46, 47 (PNP)

FIGURE 11 – "ON" VOLTAGES



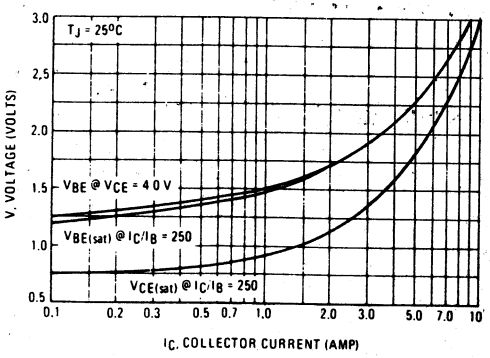
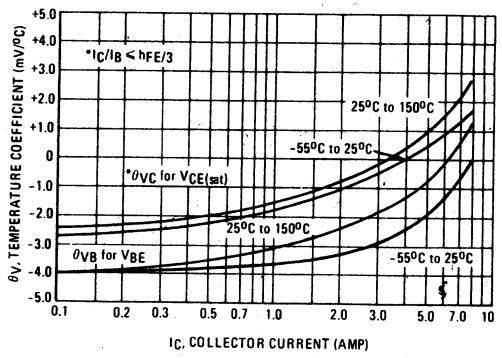


FIGURE 12 – TEMPERATURE COEFFICIENTS



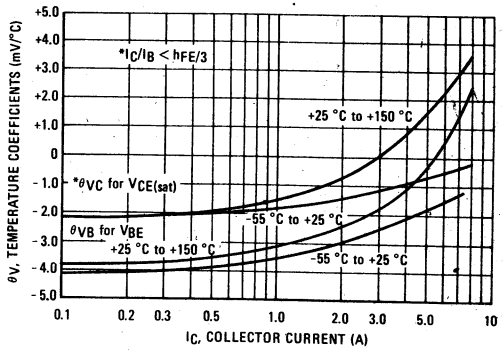
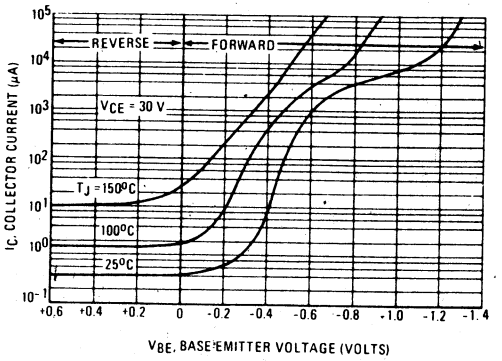


FIGURE 13 – COLLECTOR CUT-OFF REGION



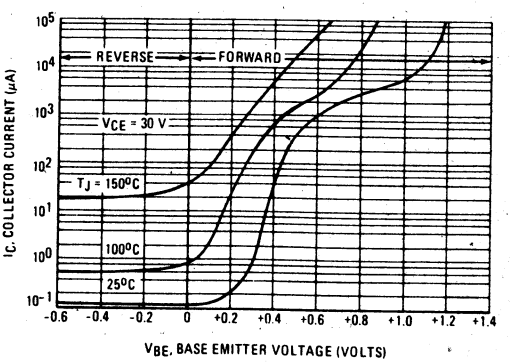


FIGURE 14 – DARLINGTON SCHEMATIC