V.H.F. POWER TRANSISTOR

N-P-N silicon planar epitaxial transistor primarily intended for use in mobile radio transmitters in the 175 MHz communications band.

Features

- multi-base structure and emitter-ballasting resistors for an optimum temperature profile
- gold metallization ensures excellent reliability
- internal matching to achieve an optimum wideband capability and high power gain

The transistor has a 6-lead flange envelope with a ceramic cap (SOT-119). All leads are isolated from the flange.

QUICK REFERENCE DATA

R.F. performance up to T_h = 25 °C in a common-emitter class-B circuit

mode of operation	V_{CE} V	f MHz	P_L W	G_p dB	η_C %
narrow band; c.w.	12,5	175	45	> 6,5	> 55

MECHANICAL DATA

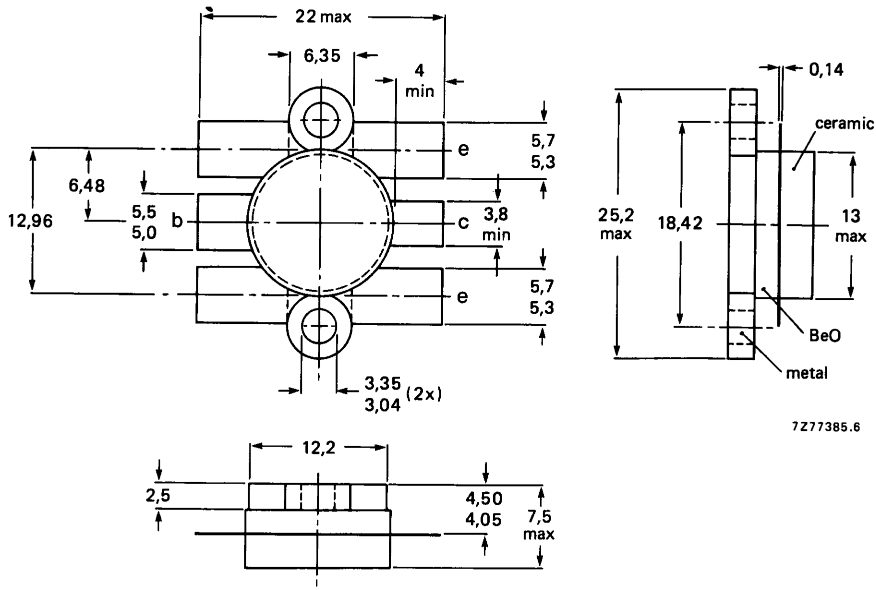
SOT-119 (see Fig. 1)

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-119.



7Z77385.6

Torque on screw: min. 0,6 Nm
max. 0,75 Nm

Recommended screw: cheese-head 4-40 UNC/2A

Heatsink compound must be applied sparingly and evenly distributed.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-base voltage (open emitter)			
peak value	V_{CBOM}	max.	36 V
Collector-emitter voltage (open base)	V_{CEO}	max.	16,5 V
Emitter-base voltage (open collector)	V_{EBO}	max.	4 V
Collector current			
d.c. or average	I_C	max.	9 A
peak value; f > 1 MHz	I_{CM}	max.	27 A
Total power dissipation			
at T_{mb} = 25 °C; f > 1 MHz	P_{tot}	max.	90 W
Storage temperature	T_{stg}		−65 to +150 °C
Operating junction temperature	T_j	max.	200 °C

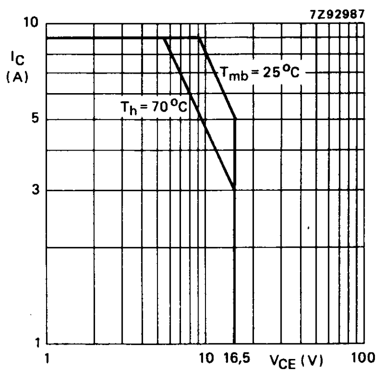


Fig. 2 D.C. soar.
$R_{th\ mb\text{-}h}$ = 0,2 K/W.

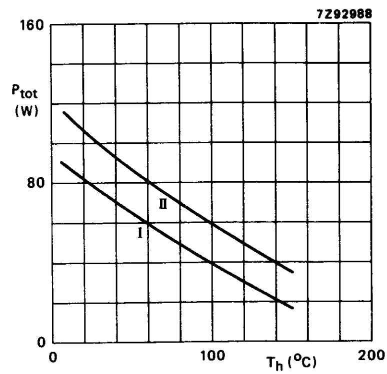


Fig. 3 Power/temperature derating curves; $R_{th\ mb\text{-}h}$ = 0,2 K/W.
I Continuous operation (f > 1 MHz)
II Short-time operation during mismatch; (f > 1 MHz)

THERMAL RESISTANCE

Dissipation = 68 W; T_{mb} = 25 °C

From junction to mounting base (r.f. operation)	$R_{th\ j\text{-}mb}$	=	1,58 K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	=	0,2 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-base breakdown voltage open emitter; I_C = 50 mA	$V_{(BR)CBO}$	>	36 V
Collector-emitter breakdown voltage open base; I_C = 100 mA	$V_{(BR)CEO}$	>	16,5 V
Emitter-base breakdown voltage open collector; I_E = 10 mA	$V_{(BR)EBO}$	>	4 V
Collector cut-off current V_{BE} = 0; V_{CE} = 16 V	I_{CES}	<	22 mA
Second breakdown energy L = 25 mH; f = 50 Hz; R_{BE} = 10 Ω	E_{SBR}	>	12,5 mJ
D.C. current gain V_{CE} = 10 V; I_C = 6 A	h_{FE}	> typ.	15 55
Collector capacitance at f = 1 MHz $I_E = i_e$ = 0; V_{CB} = 12,5 V	C_c	typ.	130 pF
Collector-flange capacitance	C_{cf}	typ.	3 pF
Feedback capacitance at f = 1 MHz I_C = 0; V_{CE} = 12,5 V	C_{re}	typ.	80 pF

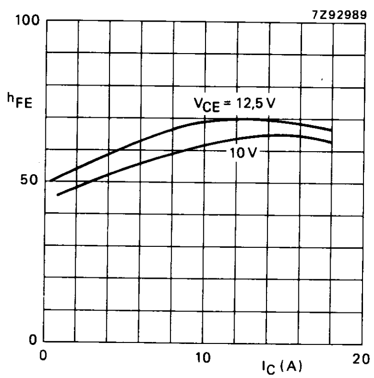


Fig. 4 D.C. current gain versus collector current; T_j = 25 °C.

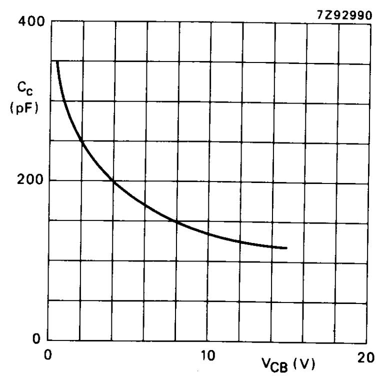


Fig. 5 Output capacitance versus V_{CB}; $I_E = i_e$ = 0; f = 1MHz; T_j = 25 °C

APPLICATION INFORMATION

R.F. performance in c.w. operation (common-emitter circuit; class-B)
f = 175 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0,2 K/W

mode of operation	V_{CE} V	P_L W	G_P dB	η_C %
narrow band; c.w.	12,5	45	> 6,5 typ. 8,0	> 55 typ. 67

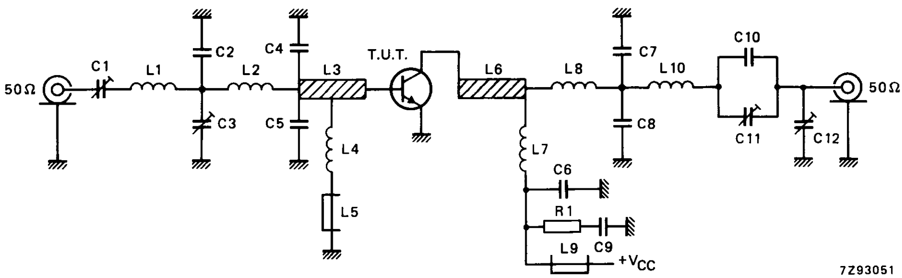


Fig. 6 Class-B test circuit at f = 175 MHz.

List of components:

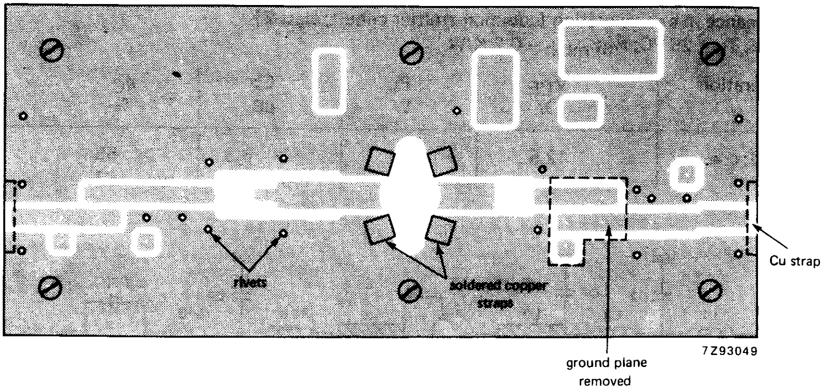
C1 = C11 = C12 = 4 to 40 film dielectric trimmer (cat.no. 2222 809 07008)
C2 = C10 = 10 pF multilayer ceramic chip capacitor *
C3 = 2,5 to 20 pF film dielectric trimmer (cat.no. 2222 809 07004)
C4 = C5 = 91 pF multilayer ceramic chip capacitor *
C6 = 820 pF multilayer ceramic chip capacitor *
C7 = C8 = 2 x 4,7 pF multilayer ceramic chip capacitors* in parallel
C9 = 100 nF polyester capacitor

L1 = strip, 28 mm x 4 mm
L2 = 4 turns Cu wire (1,0 mm); int.dia. 4,0 mm; length 7,5 mm; leads 2 x 3,5 mm
L3 = strip, 22 mm x 6 mm
L4 = 1 turn Cu wire (0,8 mm); int.dia. 3,0 mm; leads 2 x 9 mm
L5 = L9 = Ferroxcube wideband h.f. choke, grade 3B (cat.no. 4312 020 36640)
L6 = strip, 12 mm x 6 mm
L7 = 2 turns enamelled Cu wire (1,6 mm); int.dia. 5,0 mm; length 7,0 mm; leads 2 x 5 mm
L8 = 2 turns enamelled Cu wire (1,6 mm); int.dia. 5,0 mm; length 7,0 mm; leads 2 x 3 mm
L10 = strip, 18 mm x 4 mm

L1, L3, L6 and L10 are strips on a double Cu-clad printed-circuit board with epoxy fibre-glass dielectric, thickness 1/16 inch.

R1 = 4,7 Ω ± 10%, carbon resistor

* American Technical Ceramics capacitor type 100B or capacitor of same quality.



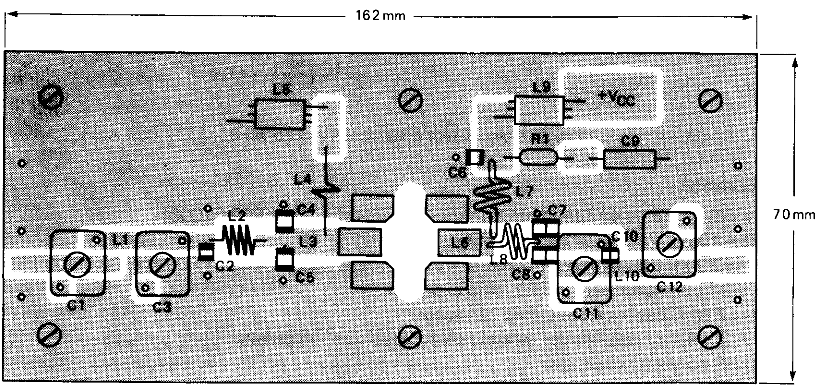


Fig. 7 Printed circuit board and component lay-out for 175 MHz class-B test circuit.

The circuit and components are on one side of the epoxy fibre-glass board. The other side, except for the area indicated by the dotted line, is unetched copper serving as a ground plane.
If the p.c.b. is in direct contact with the heatsink, the heatsink area within the dotted line has to be raised al least 0,5 mm to minimize the dielectric losses.
Earth connections are made by hollow rivets and additionally by fixing screws and copper straps under the emitters to provide a direct contact between the copper of the component side and the ground plane.

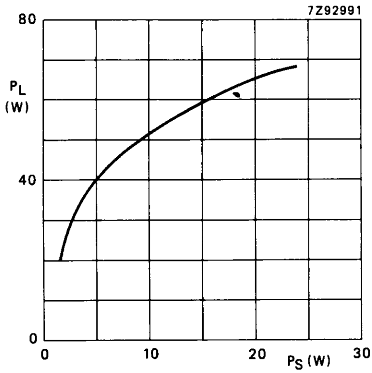


Fig. 8 Load power versus source power.

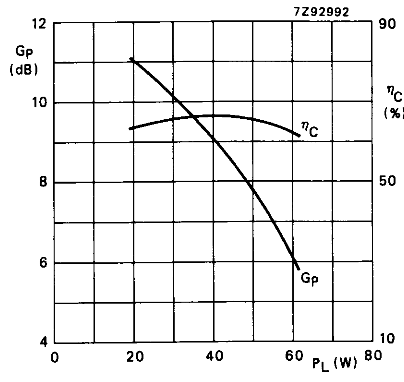


Fig. 9 Power gain and efficiency versus load power.

Condition for Figs 8 and 9:

Typical values; V_{CE} = 12,5 V; f = 175 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0,2 K/W.

Ruggedness in class-B operation

The BLV45/12 is capable of withstanding a load mismatch (VSWR = 20 through all phases) at rated load power up to a supply voltage of 15,5 V; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0,2 K/W.

Power slump

If T_h is increased from 25 °C to 70 °C the output power slump for constant P_S amounts to typ. 7 % (V_{CE} = 12,5; f = 175 MHz; $R_{th\ mb\text{-}h}$ = 0,2 K/W).

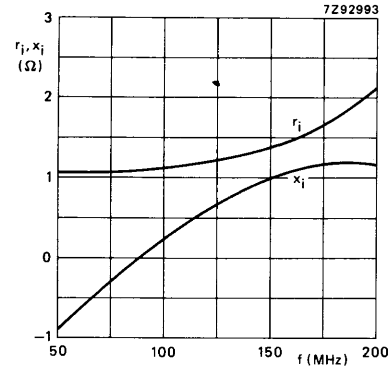


Fig. 10 Input impedance (series components).

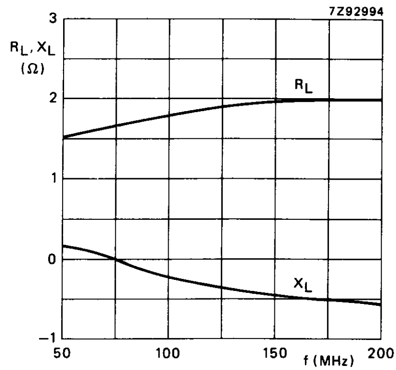


Fig. 11 Load impedance (series components).

Conditions for Figs 10, 11 and 12:

Typical values; V_{CE} = 12,5 V; P_L = 45 W; f = 50 to 200 MHz; $R_{th\ mb\text{-}h}$ = 0,2 K/W.

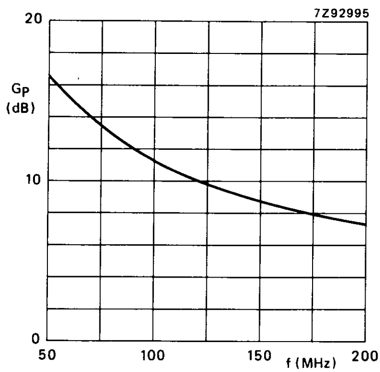


Fig. 12 Power gain versus frequency.

U.H.F. LINEAR PUSH-PULL POWER TRANSISTOR

Two n-p-n silicon planar epitaxial transistor sections in one envelope to be used as push-pull amplifier, primarily intended for use in linear u.h.f. television transmitters and transposers.

Features:

- internally matched input for wideband operation and high power gain;
- internal midpoint (r.f. ground) reduces negative feedback and improves power gain;
- increased input and output impedances (compared with single-ended transistors) simplify wideband matching;
- length of the external emitter leads is not critical;
- diffused emitter ballasting resistors for an optimum temperature profile;
- gold metallization ensures excellent reliability.

The envelope is an 8-lead flange type with a ceramic cap. All leads are isolated from the flange.

QUICK REFERENCE DATA

R.F. performance in linear amplifier

mode of operation	f_{vision} MHz	V_{CE} V	$I_{C1} = I_{C2}$ A	$I_{C(ZS)}$ A	T_h °C	d_{im}* dB	$P_{o\ sync}$* W	P_L W	G_p dB
class-A	860	25	0,85	–	70 25	−60 −55	> 6 typ. 12	–	> 8,0 typ. 9,0
class-AB	860	25	1,25	2 x 0,1	25	–	–	typ. 38**	typ. 6,5**

* Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.

** Power gain compression is 1 dB.

MECHANICAL DATA

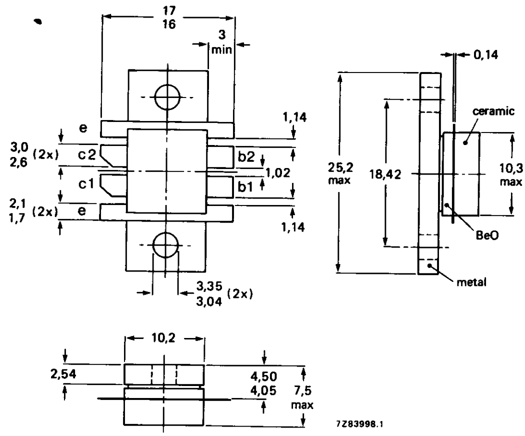
SOT-161 (see Fig. 1).

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-161.



Torque on screw: min. 0,6 Nm (6 kg cm)
max. 0,75 Nm (7,5 kg cm)

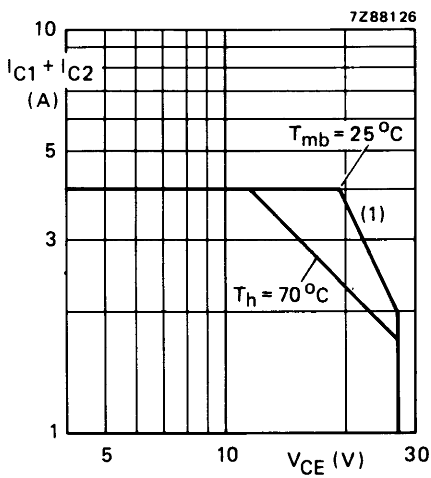
Recommended screw: cheese-head 4-40 UNC/2A

Heatsink compound must be applied sparingly and evenly distributed.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage			
(peak value); $V_{BE} = 0$	V_{CESM}	max.	50 V
open base	V_{CEO}	max.	27 V
Emitter-base voltage (open collector)	V_{EBO}	max.	3,5 V
Collector current per transistor section			
d.c. or average	I_C; $I_{C(AV)}$	max.	2 A
(peak value); f > 1 MHz	I_{CM}	max.	4 A
Total power dissipation at T_{mb} = 25 °C*	P_{tot}	max.	77 W*
R.F. power dissipation (f > 1 MHz); T_{mb} = 25 °C*	P_{rf}	max.	93 W*
Storage temperature	T_{stg}		−65 to + 150 °C
Operating junction temperature	T_j	max.	200 °C



(1) Second breakdown limit (independent of temperature).

Fig. 2 D.C. SOAR.*

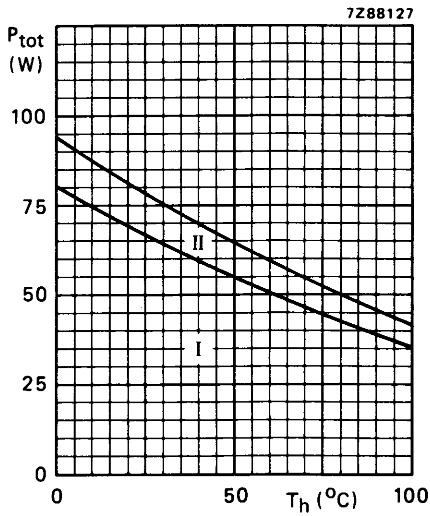


Fig. 3 Power derating curves vs. temperature.*

I Continuous d.c. (including r.f. class-A) operation

II Continuous r.f. operation

THERMAL RESISTANCE (dissipation = 42 W; T_{mb} = 80,5 °C, i.e. T_h = 70 °C)

From junction to mounting base (d.c. dissipation)	$R_{th\ j\text{-}mb(dc)}$	=	2,43 K/W
From junction to mounting base (r.f. dissipation)	$R_{th\ j\text{-}mb(rf)}$	=	1,91 K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	=	0,25 K/W

* Dissipation of either transistor section should not exceed half rated dissipation.

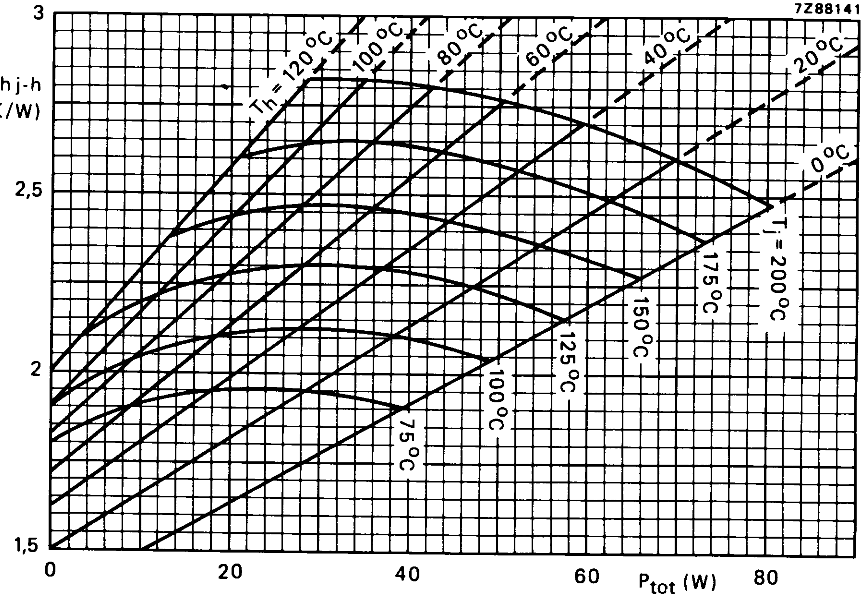


Fig. 4 Maximum thermal resistance from junction to heatsink as a function of power dissipation, with heatsink and junction temperature as parameters. ($R_{th\ mb-h}$ = 0,25 K/W.)

Example

Nominal class-A push-pull operation (without r.f. signal): V_{CE} = 25 V; I_{C1} = I_{C2} = 0,85 A; T_h = 70 °C.

Fig. 4 shows:	$R_{th\ j-h}$	max.	2,68 K/W
	T_j	max.	184 °C
Typical device:	$R_{th\ j-h}$	typ.	2,28 K/W
	T_j	typ.	167 °C

CHARACTERISTICS apply to either transistor section unless otherwise specified

T_j = 25 °C

Collector-emitter breakdown voltage				
V_{BE} = 0; I_C = 10 mA	$V_{(BR)CES}$	>	50	V
open base; I_C = 25 mA	$V_{(BR)CEO}$	>	27	V
Emitter-base breakdown voltage				
open collector; I_E = 5 mA	$V_{(BR)EBO}$	>	3,5	V
Collector cut-off current				
V_{BE} = 0; V_{CE} = 27 V	I_{CES}	<	10	mA
Second breakdown energy; L = 25 mH; f = 50 Hz				
open base	E_{SBO}	>	2	mJ
R_{BE} = 10 Ω	E_{SBR}	>	2	mJ
D.C. current gain*				
I_C = 0,85 A; V_{CE} = 25 V	h_{FE}	>	15	
		typ.	40	
D.C. current gain ratio of transistor sections				
I_C = 0,85 A; V_{CE} = 25 V		0,67 to 1,5		
Collector-emitter saturation voltage*				
I_C = 1,7 A; I_B = 0,17 A	V_{CEsat}	typ.	0,75	V
Transition frequency at f = 100 MHz**				
$-I_E$ = 0,85 A; V_{CB} = 25 V	f_T	typ.	2,5	GHz
$-I_E$ = 1,7 A; V_{CB} = 25 V	f_T	typ.	2,5	GHz
Collector capacitance at f = 1 MHz				
$I_E = I_e$ = 0; V_{CB} = 25 V	C_c	typ.	24	pF
		<	30	pF
Feedback capacitance at f = 1 MHz				
I_C = 50 mA; V_{CE} = 25 V	C_{re}	typ.	15	pF
Collector-flange capacitance	C_{cf}	typ.	2	pF

* Measured under pulse conditions: $t_p \leqslant 300\ \mu s$; $\delta \leqslant 0,02$.

** Measured under pulse conditions: $t_p \leqslant 50\ \mu s$; $\delta \leqslant 0,01$.

The graphs apply to either transistor section.

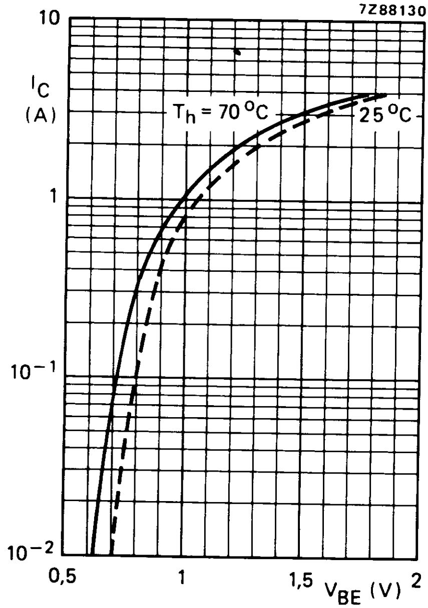


Fig. 5 Typical values; V_{CE} = 25 V.

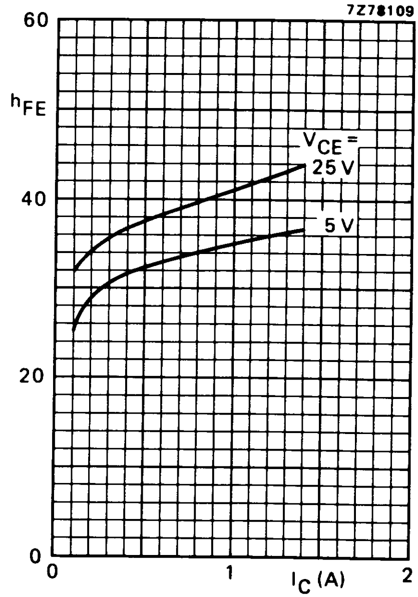


Fig. 6 Typical values; T_j = 25 °C.

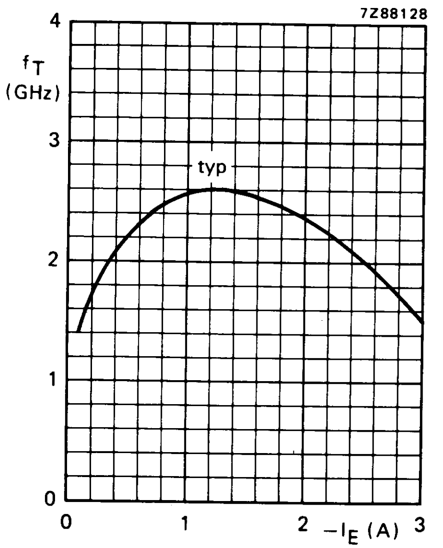


Fig. 7 V_{CB} = 25 V; f = 500 MHz; T_j = 25 °C.

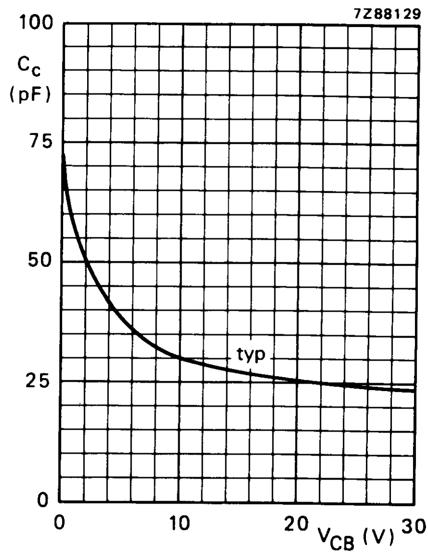


Fig. 8 $I_E = I_e = 0$; f = 1 MHz; T_j = 25 °C.

APPLICATION INFORMATION

R.F. performance in u.h.f. class-A operation (linear push-pull power amplifier)

f_{vision} (MHz)	V_{CE} (V)	$I_{C1} = I_{C2}$ (A)	T_h (°C)	d_{im}* (dB)	$P_{o\ sync}$* (W)	G_p (dB)
860	25	0,85	70	−60	> 6	> 8,0
			70	−60	typ. 7,5	typ. 8,5
			70	−55	typ. 10	typ. 8,5
			25	−55	typ. 12	typ. 9,0

* Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.

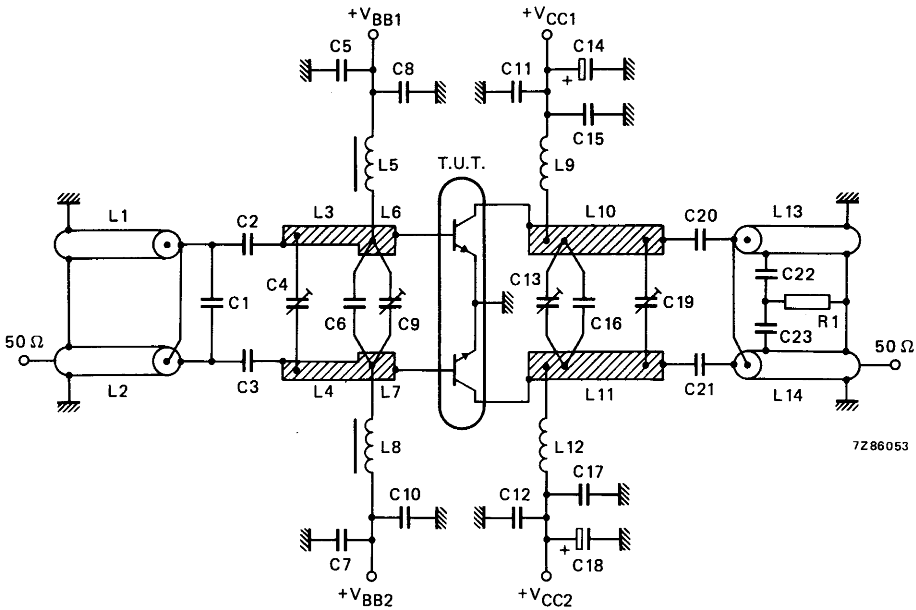


Fig. 9 Class-A test circuit at f_{vision} = 860 MHz.

List of components:

C1 = C6 = C16 = 4,7 pF (500 V) multilayer ceramic chip capacitor (ATC▲)
C2 = C3 = C20 = C21 = 33 pF multilayer ceramic chip capacitor (cat. no. 2222 851 13339)
C4 = C9 = C13 = C19 = 1,2 to 3,5 pF film dielectric trimmer (cat. no. 2222 809 05001)
C5 = C7 = C15 = C17 = 100 nF multilayer ceramic chip capacitor (cat. no. 2222 852 59104)
C8 = C10 = C11 = C12 = 220 pF multilayer ceramic chip capacitor (cat. no. 2222 852 13221)
C14 = C18 = 6,8 μF/40 V solid aluminium electrolytic capacitor
C22 = C23 = 1 pF (500 V) multilayer ceramic chip capacitor (ATC▲)

C9 and C13 are placed 8,0 and 14,0 mm from transistor edge, respectively.

▲ ATC means American Technical Ceramics.

L1 = L2 = L13 = L14 = 50 Ω semi-rigid cable; outer diameter 2,2 mm; length 29,0 mm. These cables are soldered on 75 Ω striplines (1,1 mm x 28,0 mm). The centre conductors of the cables L1 and L13 are not connected.
L3 = L4 = 52 Ω stripline (2,0 mm x 16,5 mm)
L5 = L8 = 470 nH microchoke
L6 = L7 = 39 Ω stripline (3,1 mm x 8,0 mm)
L9 = L12 = 1 turn Cu wire (1,0 mm); int. dia. 5,5 mm; leads 2 x 3,5 mm
L10 = L11 = 39 Ω stripline (3,1 mm x 34,0 mm)

L3, L4, L6, L7, L10 and L11 are striplines on a double Cu-clad printed-circuit board with PTFE fibre-glass dielectric (ϵ_r = 2,74); thickness 1/32".

R1 = 10 Ω carbon resistor

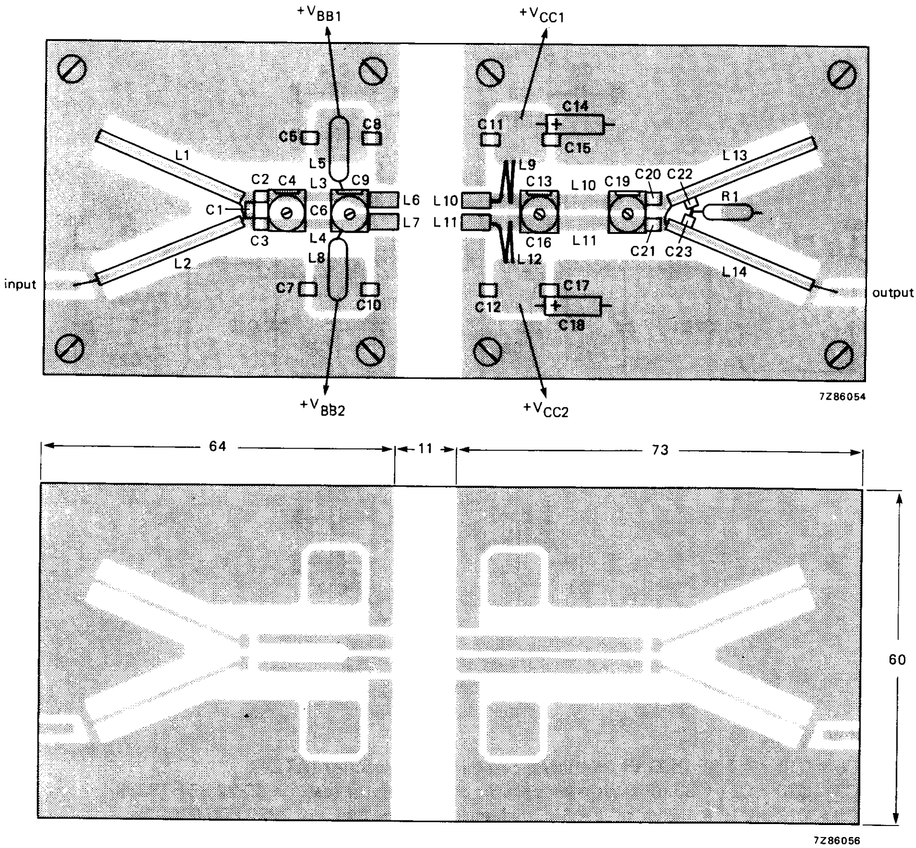


Fig. 10 Component layout and printed-circuit board for 860 MHz class-A test circuit.

The circuit and the components are on one side of the PTFE fibre-glass board, the other side is unetched copper to serve as a ground-plane. Earth connections are made by means of bolts. Additionally copper straps are used under the emitters and at the input and output to provide direct contact between the copper on the component side and the ground-plane.

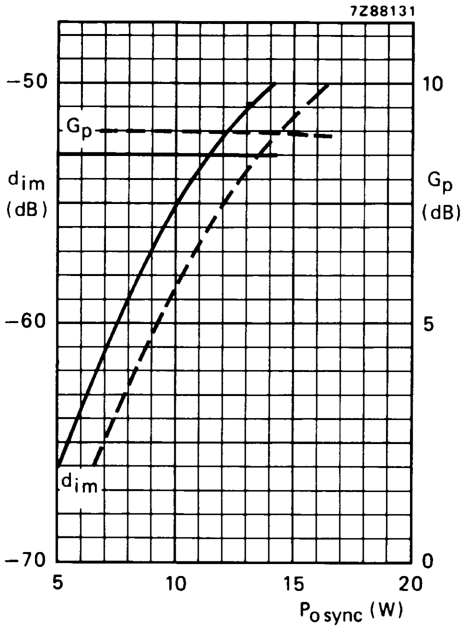


Fig. 11 Intermodulation distortion (d_{im})* and power gain as a function of output power.

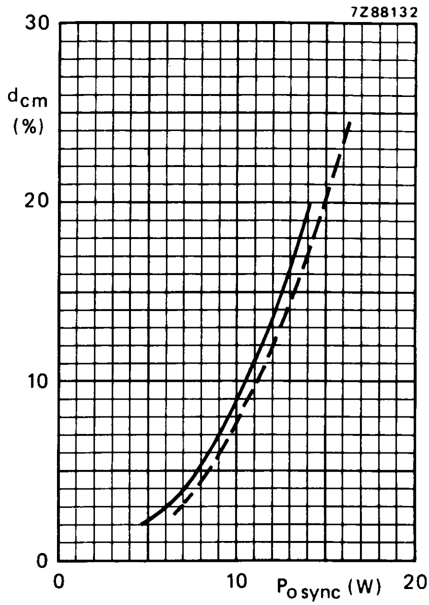


Fig. 12 Cross-modulation distortion (d_{cm})** as a function of output power.

Conditions for Figs 11 and 12:

Typical values; V_{CE} = 25 V; I_C = 2 x 0,85 A; — — — T_h = 25 °C; ——— T_h = 70 °C; f_{vision} = 860 MHz.

Ruggedness in push-pull class-A operation

The BLV57 is capable of withstanding full load mismatch (VSWR = 50 through all phases) under the following conditions:
V_{CE} = 25 V; I_C = 2 x 0,85 A; T_h = 70 °C; $P_{o\,sync}$* ⩽ 12,5 W; f = 860 MHz; $R_{th\,mb\text{-}h}$ = 0,25 K/W.
At any other composition of the output signal: P_L (r.m.s. value) ⩽ 5 W.

* Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.
Intermodulation distortion of input signal ⩽ −70 dB.

** Two-tone test method (vision carrier 0 dB, sound carrier −7 dB), zero dB corresponds to peak sync level.
Cross-modulation distortion (d_{cm}) is the voltage variation (%) of sound carrier when vision carrier is switched from 0 dB to −20 dB.

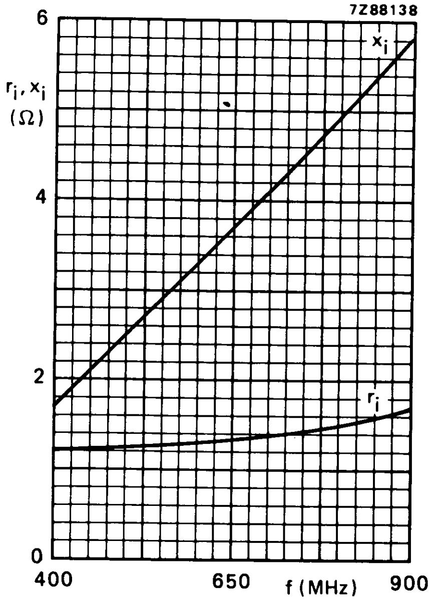


Fig. 20 Input impedance (series components).

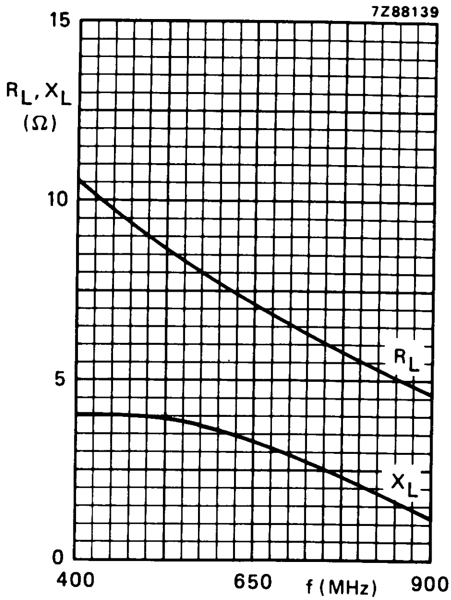


Fig. 21 Load impedance (series components).

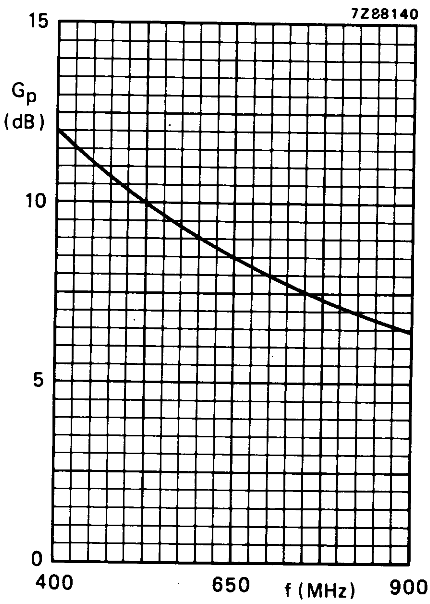


Fig. 22.

Conditions for Figs 20; 21 and 22:

The graphs apply to either transistor section assuming class-AB push-pull operation.
Typical values; V_{CE} = 25 V; $I_{C(ZS)}$ = 0,1 A;
P_L = 17,5 W (P.E.P.); T_h = 70 °C.

APPLICATION INFORMATION

R.F. performance in u.h.f. class-AB operation (c.w.)

f_{vision} (MHz)	V_{CE} (V)	$I_{C(ZS)}$ (A)	T_h (°C)	P_L (W)	$I_{C1} = I_{C2}$ (A)	η (%)	G_p* (dB)
860	25	2 x 0,1	25	12,5			typ. 7,5
				38	typ. 1,25	typ. 60	typ. 6,5
860	25	2 x 0,1	70	12,5			typ. 7,0
				30	typ. 1,10	typ. 55	typ. 6,0

* Typical values are based on 1 dB gain compression. Using a 3rd order amplitude transfer characteristic, 1 dB compression corresponds with 30% sync input/25% sync output compression in television service (negative modulation, C.C.I.R. system).

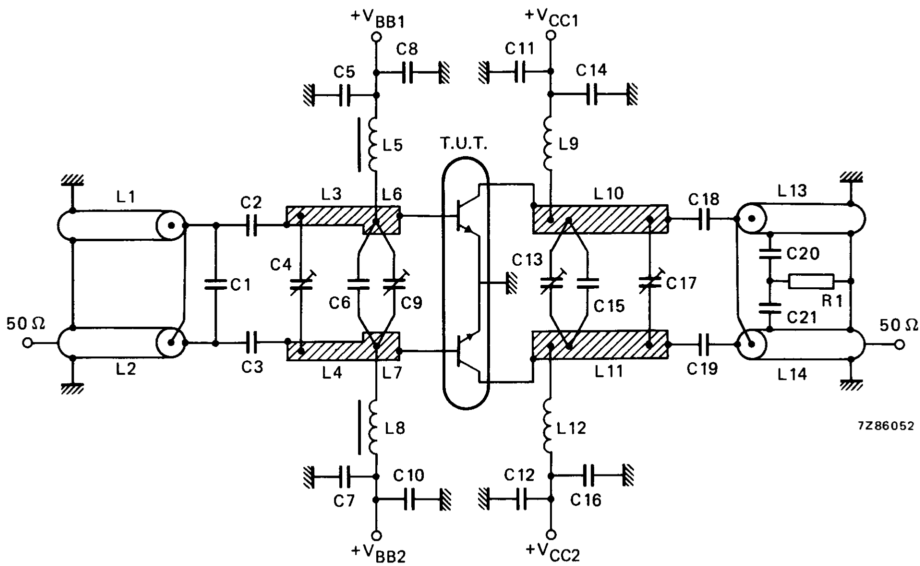


Fig. 16 Class-AB test circuit at f_{vision} = 860 MHz.

List of components:

C1 = C6 = C15 = 4,7 pF (500 V) multilayer ceramic chip capacitor (ATC▲)
C2 = C3 = C18 = C19 = 33 pF multilayer ceramic chip capacitor (cat. no. 2222 851 13339)
C4 = C9 = C13 = C17 = 1,2 to 3,5 pF film dielectric trimmer (cat. no. 2222 809 05001)
C5 = C7 = C14 = C16 = 100 nF multilayer ceramic chip capacitor (cat. no. 2222 852 59104)
C8 = C10 = C11 = C12 = 220 pF multilayer ceramic chip capacitor (cat. no. 2222 852 13221)
C20 = C21 = 1 pF (500 V) multilayer ceramic chip capacitor (ATC▲)

C9 and C13 are placed 8,0 and 14,0 mm from transistor edge, respectively.

▲ ATC means American Technical Ceramics.

L1 = L2 = L13 = L14 = 50 Ω semi-rigid cable; outer diameter 2,2 mm; length 29,0 mm. These cables are soldered on 75 Ω striplines (1,1 mm x 28,0 mm). The centre conductors of the cables L1 and L13 are not connected.

L3 = L4 = 52 Ω stripline (2,0 mm x 16,5 mm)
L5 = L8 = 470 nH microchoke
L6 = L7 = 39 Ω stripline (3,1 mm x 8,0 mm)
L9 = L12 = 1 turn Cu wire (1,0 mm); int. dia. 5,5 mm; leads 2 x 3,5 mm
L10 = L11 = 39 Ω stripline (3,1 mm x 34,0 mm)

L3, L4, L6, L7, L10 and L11 are striplines on a double Cu-clad printed-circuit board with PTFE fibre-glass dielectric (ϵ_r = 2,74); thickness 1/32".

R1 = 10 Ω carbon resistor

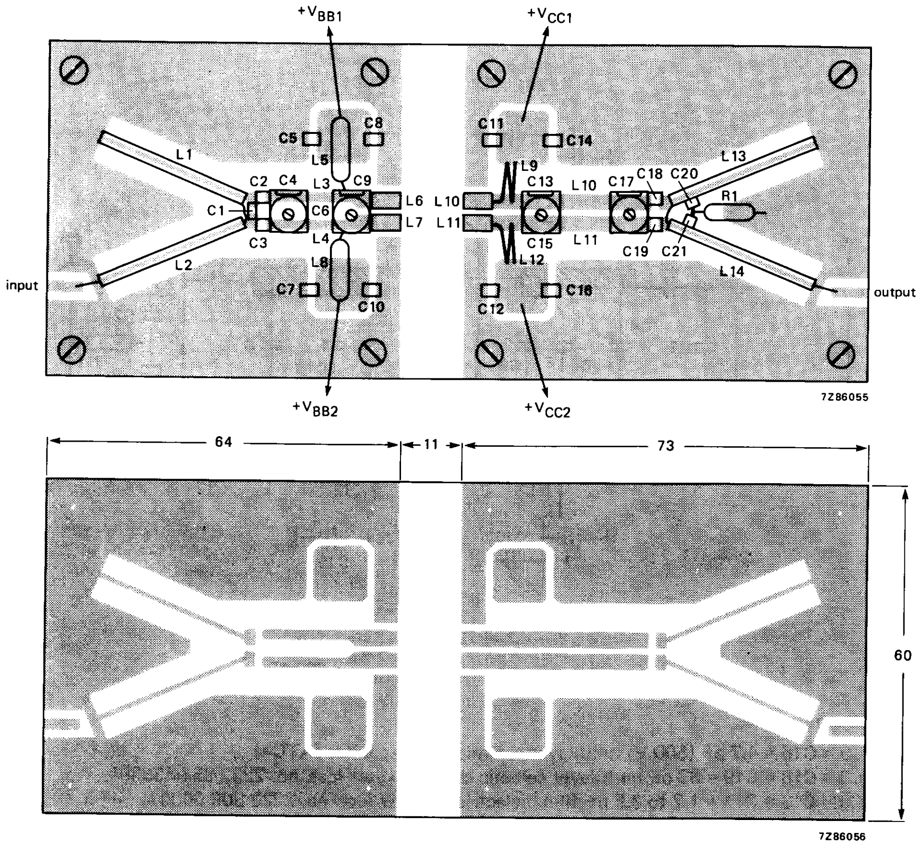


Fig. 17 Component layout and printed-circuit board for 860 MHz class-AB test circuit.

The circuit and the componenets are on one side of the PTFE fibre-glass board, the other side is unetched copper to serve as a ground-plane. Earth connections are made by means of bolts. Additionally copper straps are used under the emitters and at the input and output to provide direct contact between the copper on the component side and the ground-plane.

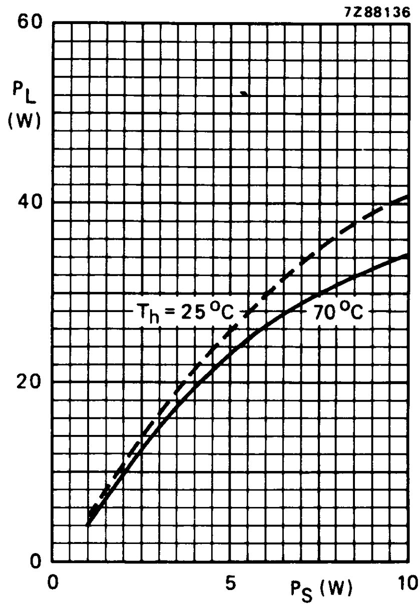


Fig. 18 Typical values; V_{CE} = 25 V; $I_{C(ZS)}$ = 2 x 0,1 A; f_{vision} = 860 MHz.

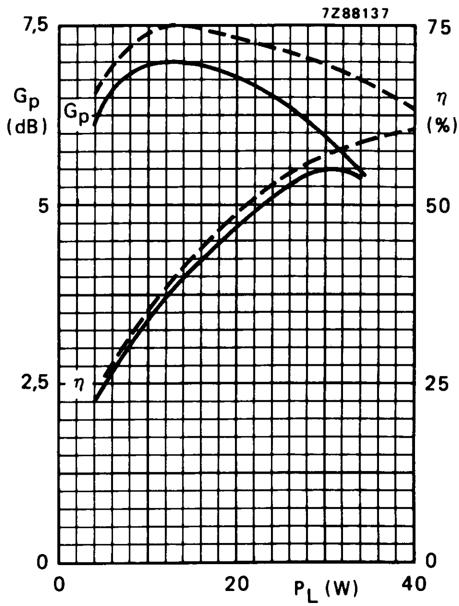


Fig. 19 Typical values; V_{CE} = 25 V; $I_{C(ZS)}$ = 2 x 0,1 A; – – – T_h = 25 °C; —— T_h = 70 °C; f_{vision} = 860 MHz.

Ruggedness in class-AB operation

The BLV57 is capable of withstanding a load mismatch (VSWR ⩽ 2 through all phases) up to 30 W (r.m.s. value) or (VSWR ⩽ 50 through all phases) up to 19 W under the following conditions: V_{CE} = 25 V; T_h = 70 °C; f = 860 MHz; $R_{th\ mb\text{-}h}$ = 0,25 K/W.

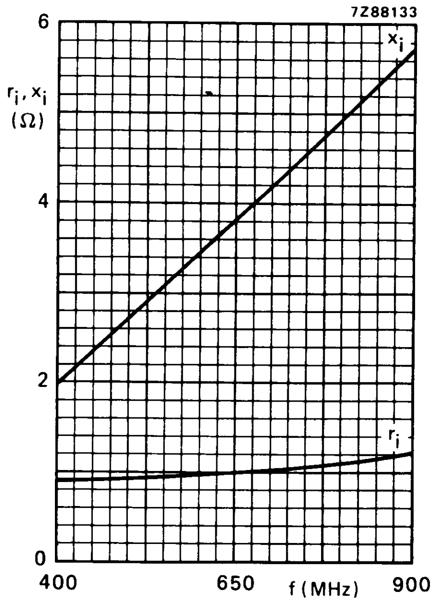


Fig. 13 Input impedance (series components).

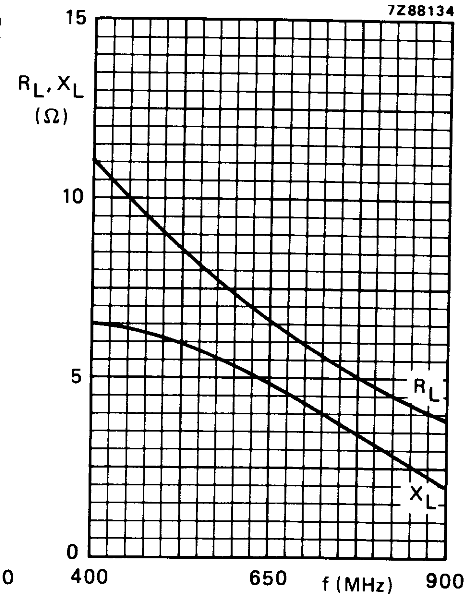


Fig. 14 Load impedance (series components).

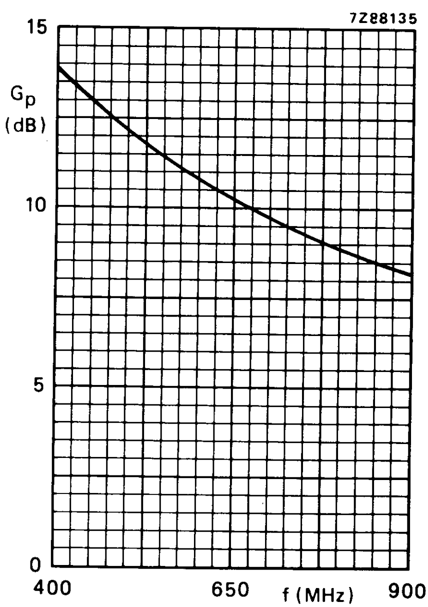


Fig. 15.

Conditions for Figs 13, 14 and 15:

The graphs apply to either transistor section assuming class-A push-pull operation.
Typical values; V_{CE} = 25 V; I_C = 0,85 A;
T_h = 70 °C.

U.H.F. LINEAR POWER TRANSISTOR

N-P-N silicon planar epitaxial transistor in SOT-171 envelope primarily intended for use as linear amplifier in u.h.f. television transmitters.

Features:

- internal input matching to achieve an optimum wideband capability and high power gain
- emitter-ballasting resistors for lower junction temperatures.
- titanium-platinum-gold ensures long life and excellent reliability.

The transistor has a 6-lead flange envelope with a ceramic cap. All leads are isolated from the flange.

QUICK REFERENCE DATA

R.F. performance up to T_h = 25 °C in common emitter class-AB circuit.

mode of operation	V_{CE} V	f MHz	P_L W	G_p dB	η_C %
class AB; c.w.	25	860	30	min. 7,0	min. 50

MECHANICAL DATA

Dimensions in mm

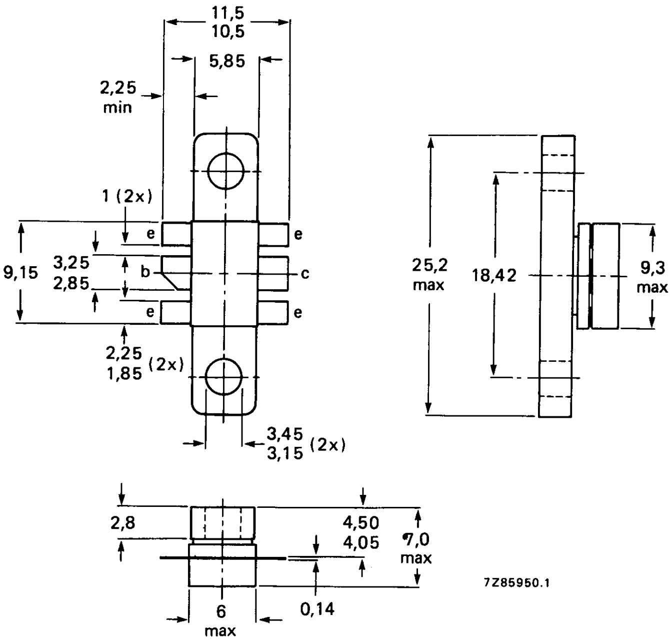
SOT-171 (see Fig. 1).

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-171.



Torque on screw: min. 0,6 Nm (6 kg.cm)
max. 0,75 Nm (7,5 kg.cm)

Recommended screw : cheese-head 4-40 UNC/2A

Heatsink compound must be applied sparingly and evenly distributed.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-base voltage (open emitter)	V_{CBO}	max.	50 V
Collector-emitter voltage (open base)	V_{CEO}	max.	27 V
Emitter-base voltage (open collector)	V_{EBO}	max.	3,5 V
Collector current			
d.c. or average	I_C	max.	3 A
(peak value); f > 1 MHz	I_{CM}	max.	9 A
Total power dissipation			
at T_{mb} = 25 °C; f > 1 MHz	P_{tot}	max.	70 W
Storage temperature	T_{stg}	−65 to +150 °C	
Operating junction temperature	T_j	max.	200 °C

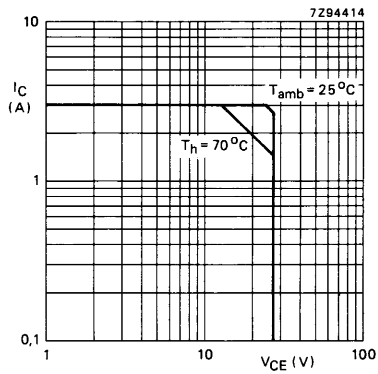


Fig. 2 D.C. SOAR; $R_{th\ mb-h}$ = 0,4 K/W.

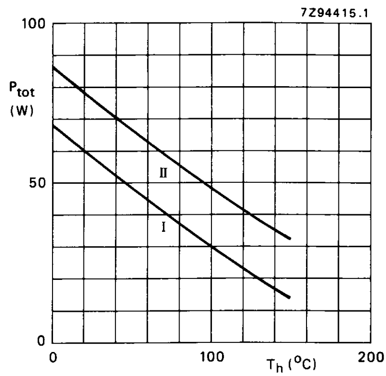


Fig. 3 Power/temperature derating curves versus heatsink temperature.

I Continuous operation (f > 1 MHz)

II Short-time operation during mismatch (f > 1 MHz)

MAXIMUM THERMAL RESISTANCE

Dissipation = 50 W; T_{amb} = 25 °C

From junction to mounting base	$R_{th\ j-mb}$	max.	2,3 K/W
From mounting base to heatsink	$R_{th\ mb-h}$	max.	0,4 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-base breakdown voltage open emitter; I_C = 50 mA	$V_{(BR)CBO}$	min.	50 V
Collector-emitter breakdown voltage open base; I_C = 100 mA	$V_{(BR)CEO}$	min.	27 V
Emitter-base breakdown voltage open collector; I_E = 10 mA	$V_{(BR)EBO}$	min.	3,5 V
Collector leakage current V_{BE} = 0; V_{CE} = 27 V	I_{CES}	max.	10 mA
Second breakdown energy L = 25 mH; f = 50 Hz; R_{BE} = 10 Ω	E_{SBR}	min.	4 mJ
D.C. current gain V_{CE} = 20 V; I_C = 2 A	h_{FE}	min.	15
Collector capacitance at f = 1 MHz $I_E = i_e$ = 0; V_{CB} = 25 V	C_c	typ.	44 pF
Feedback capacitance at f = 1 MHz I_C = 0; V_{CE} = 25 V	C_{re}	typ.	30 pF
Collector-flange capacitance	C_{cf}	typ.	2 pF

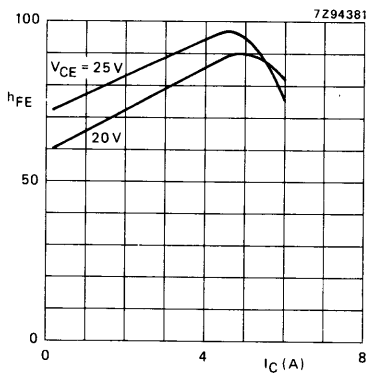


Fig. 4 D.C. current gain versus collector current; T_j = 25 °C.

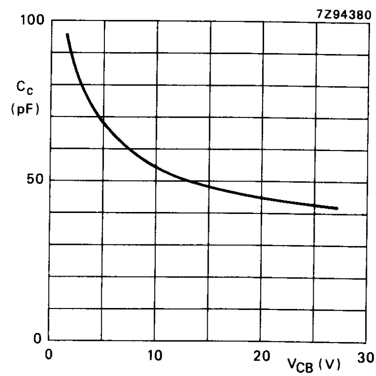


Fig. 5 Output capacitance versus V_{CB}; $I_E = i_e$ = 0; f = 1 MHz.

APPLICATION INFORMATION

R.F. performance up to T_h = 25 °C in common emitter class-AB circuit (c.w.); $R_{th\ mb\text{-}h}$ = 0,4 K/W

f (MHz)	V_{CE} (V)	$I_{C(ZS)}$ (mA)	Gp (dB)	P_L (W)	η (%)	ΔGp (dB)▲
860	25	60	min. 7,0 typ. 8,5	30	min. 50 typ. 55	max. 1,0 typ. 0,2

▲ Assuming a 3rd-order amplitude transfer characteristic, 1 dB gain compression corresponds with 30% sync input/25% sync output compression in television service (negative modulation, C.C.I.R. system).

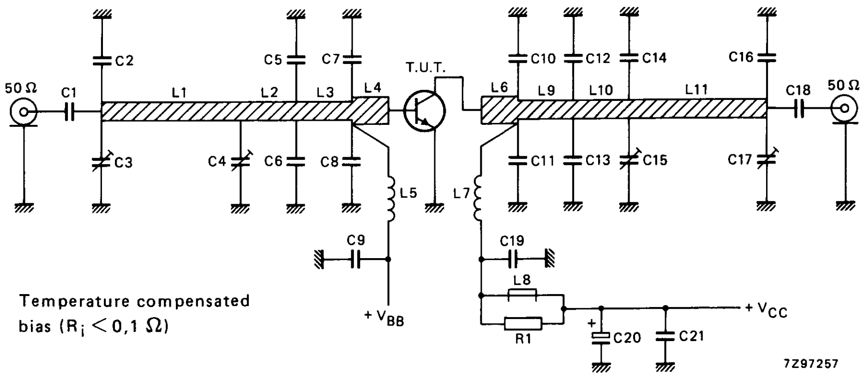


Fig. 6 Class-AB test circuit at f = 860 MHz.

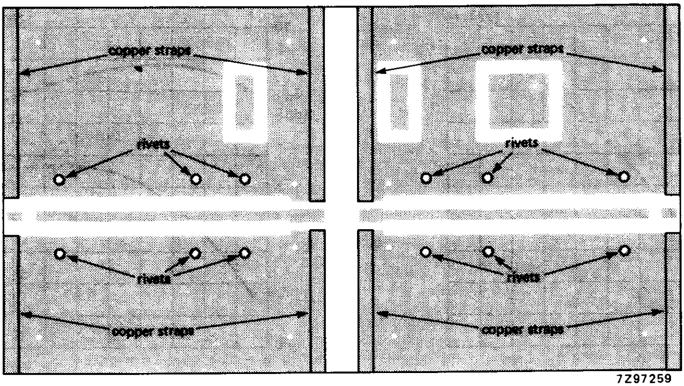
List of components:

C1 = C18 = 33 pF multilayer ceramic chip capacitor*
C2 = C14 = C16 = 3,6 pF multilayer ceramic chip capacitor*
C3 = C4 = C15 = C17 = 1,4 – 5,5 pF film dielectric trimmer (cat. no. 2222 809 09001)
C5 = C6 = 1,8 pF multilayer ceramic chip capacitor*
C7 = C8 = 6,2 pF multilayer ceramic chip capacitor*
C9 = C21 = 330 pF multilayer ceramic chip capacitor*
C10 = C11 = 5,6 pF multilayer ceramic chip capacitor**
C12 = 5,6 pF multilayer ceramic chip capacitor*
C13 = 6,2 pF multilayer ceramic chip capacitor*
C19 = 10 pF multilayer ceramic chip capacitor*
C20 = 6,8 μF (63 V) electrolytic capacitor
L1 = L11 = 50 Ω stripline (26 mm x 2,4 mm)
L2 = L3 = 50 Ω stripline (9,5 mm x 2,4 mm)
L4 = 42,6 Ω stripline (6,0 mm x 3,0 mm)
L5 = 60 nH; 4 turns closely wound enamelled Cu-wire (0,4 mm) int. dia. 3 mm; leads 2 x 5 mm.
L6 = 42,6 Ω stripline (4,0 mm x 3,0 mm)
L7 = 45 nH; 4 closely wound enamelled Cu-wire (1 mm); int. dia. 4 mm; leads 2 x 5 mm
L8 = Ferroxcube h.f. choke, grade 3B (cat.no. 4312 020 36642)
L9 = 50 Ω stripline (9,0 mm x 2,4 mm)
L10 = 50 Ω stripline (13,5 mm x 2,4 mm)
R1 = 10 Ω ± 5%, 1 W metal film resistor

The striplines are on a double Cu-clad printed circuit board with a P.T.F.E. fibre-glass dielectric (ϵ_r = 2,2); thickness 1/32 inch.

* American Technical Ceramics type 100B or capacitor of the same quality.

** American Technical Ceramics type 100A or capacitor of the same quality.



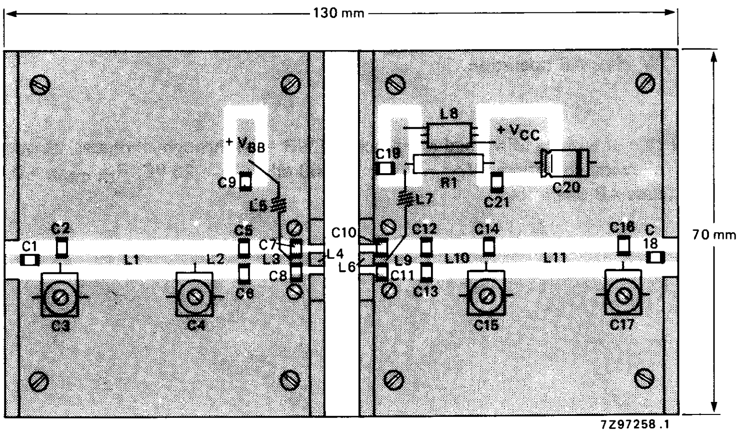


Fig. 7 Printed circuit board and component layout for 860 MHz class-AB test circuit.

The circuit and the components are on one side of the PTFE fibre-glass board; the other side is unetched copper serving as a ground plane. Earth connections are made by fixing screws, hollow rivets and copper straps around the board and under the bases to provide a direct contact between the copper on the component side and the ground plane.

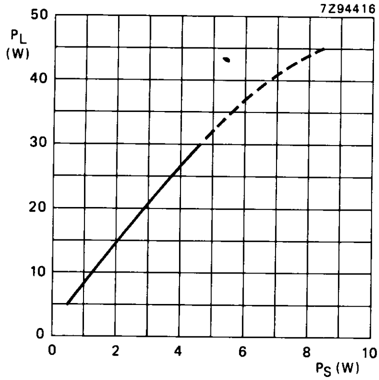


Fig. 8 Load power versus source power.

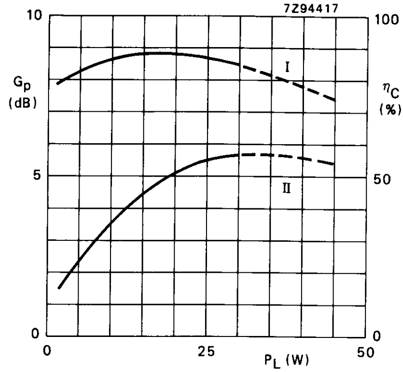


Fig. 9 Power gain (I) and efficiency versus load power (II).

Conditions for Figs 8 and 9:

Typical values; V_{CE} = 25 V; f = 860 MHz; $I_{C(ZS)}$ = 60 mA; T_h = 25 °C
$R_{th\ mb\text{-}h}$ = 0,4 K/W; class-AB operation.

RUGGEDNESS

The BLV59 is capable of withstanding load mismatch (VSWR = 10 through all phases) at rated load power under the following conditions; V_{CE} = 25 V; f = 860 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0,4 K/W; $I_{C(ZS)}$ = 60 mA (class-AB operation).

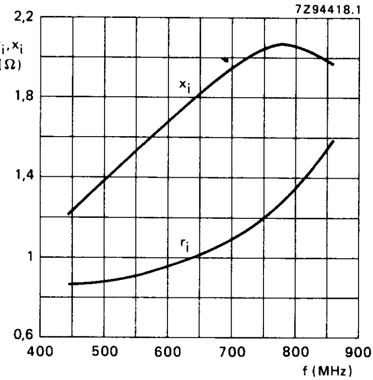


Fig. 10 Input impedance (series components).

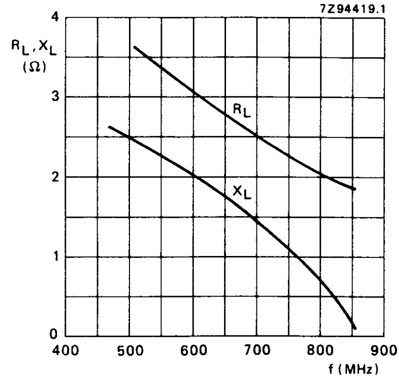


Fig. 11 Load impedance (series components).

Conditions for Figs 10, 11 and 12

Typical values; V_{CE} = 25 V; P_L = 30 W; f = 470 to 860 MHz; T_h = 25 °C;
$R_{th\ mb\text{-}h}$ = 0,4 K/W; $I_{C(ZS)}$ = 60 mA; class-AB operation.

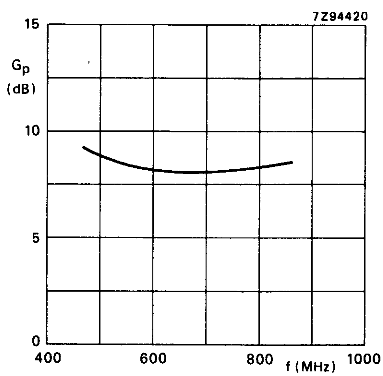


Fig. 12 Power gain versus frequency.

V.H.F. POWER TRANSISTOR

N-P-N silicon planar epitaxial transistor primarily intended for use in mobile radio transmitters in the 175 MHz communications band.

Features

- multi-base structure and emitter-ballasting resistors for an optimum temperature profile
- gold metallization ensures excellent reliability
- internal matching to achieve an optimum wideband capability and high power gain

The transistor has a 6-lead flange envelope with a ceramic cap (SOT-119). All leads are isolated from the flange.

QUICK REFERENCE DATA

R.F. performance up to T_h = 25 °C in a common-emitter class-B circuit

mode of operation	V_{CE} V	f MHz	P_L W	G_p dB	η_C %
narrow band; c.w.	12,5	175	75	> 6,5	> 55

MECHANICAL DATA

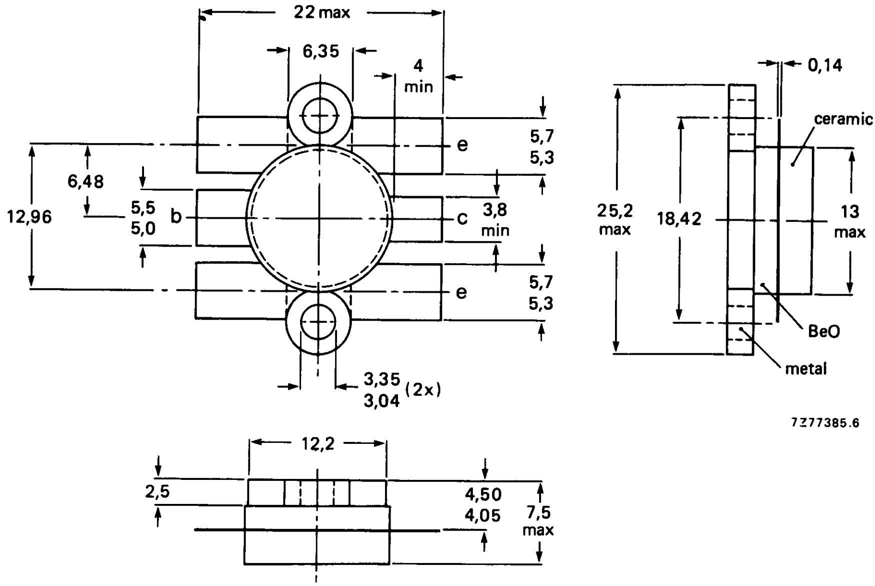
Fig. 1 SOT-119 (see Fig. 1)

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-119.



Torque on screw:	min. 0,6 Nm (6 kg.cm) max. 0,75 Nm (7,5 kg.cm)
Recommended screw:	cheese-head 4-40 UNC/2A

Heatsink compound must be applied sparingly and evenly distributed.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-base voltage (open emitter) peak value	V_{CBOM}	max.	36 V
Collector-emitter voltage (open base)	V_{CEO}	max.	16,5 V
Emitter-base voltage (open collector)	V_{EBO}	max.	4 V
Collector current d.c. or average	I_C	max.	15 A
peak value; f > 1 MHz	I_{CM}	max.	45 A
Total power dissipation at T_{mb} = 25 °C; f > 1 MHz	P_{tot}	max.	150 W
Storage temperature	T_{stg}		−65 to + 150 °C
Operating junction temperature	T_j	max.	200 °C

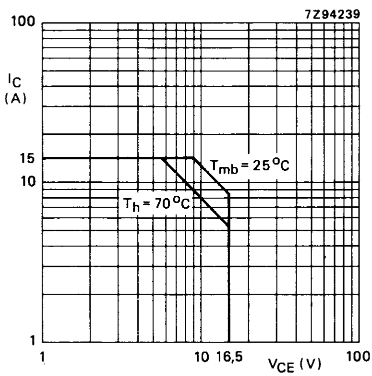


Fig. 2 D.C. soar.
$R_{th\ mb-h}$ = 0,2 K/W.

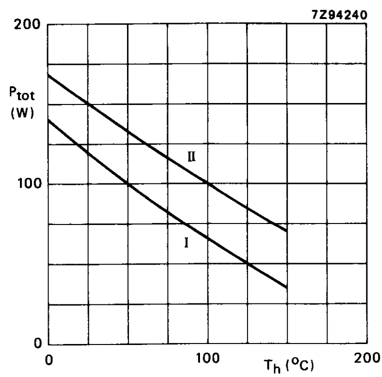


Fig. 3 Power/temperature derating curves; $R_{th\ mb-h}$ = 0,2 K/W.
I Continuous operation (f > 1 MHz)
II Short-time operation during mismatch; (f > 1 MHz).

THERMAL RESISTANCE

Dissipation = 96 W; T_{mb} = 25 °C

From junction to mounting base (r.f. operation)	$R_{th\ j-mb}$	=	1,05 K/W
From mounting base to heatsink	$R_{th\ mb-h}$	=	0,2 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-base breakdown voltage open emitter; I_C = 100 mA	$V_{(BR)CBO}$	min.	36 V
Collector-emitter breakdown voltage open base; I_C = 200 mA	$V_{(BR)CEO}$	min.	16,5 V
Emitter-base breakdown voltage open collector; I_E = 20 mA	$V_{(BR)EBO}$	min.	4 V
Collector cut-off current V_{BE} = 0; V_{CE} = 16 V	I_{CES}	max.	44 mA
Second breakdown energy L = 25 mH; f = 50 Hz; R_{BE} = 10 Ω	E_{SBR}	min.	20 mJ
D.C. current gain V_{CE} = 10 V; I_C = 10 A	h_{FE}	min. typ.	15 55
Collector capacitance at f = 1 MHz I_E = i_e = 0; V_{CB} = 12,5 V	C_c	typ.	240 pF
Feedback capacitance at f = 1 MHz I_C = 0; V_{CE} = 12,5 V	C_{re}	typ.	150 pF
Collector-flange capacitance	C_{cf}	typ.	3 pF

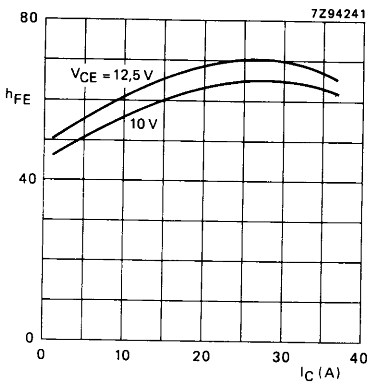


Fig. 4 D.C. current gain versus collector current; T_j = 25 °C.

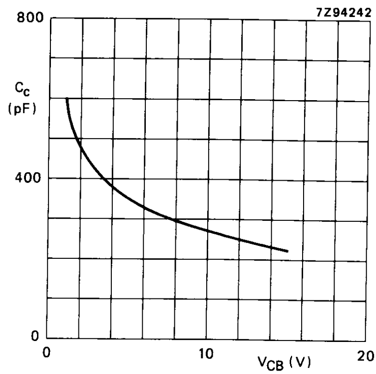


Fig. 5 Output capacitance versus V_{CB}; I_E = i_e = 0; f = 1 MHz; T_j = 25 °C.

APPLICATION

R.F. performance in c.w. operation (common-emitter circuit; class-B)
f = 175 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0,2 K/W

mode of operation	V_{CE} V	P_L W	G_p dB	η_C %
narrow band; c.w.	12,5	75	> 6,5 typ. 7,5	> 55 typ. 63

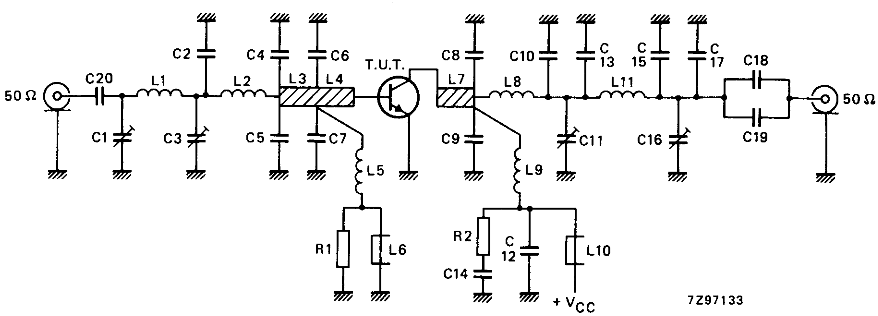


Fig. 6 Class-B test circuit at f = 175 MHz.

List of components:

C1 = 5 to 60 pF film dielectric trimmer (cat. no. 2222 809 07011)
C2 = 10 pF multilayer ceramic chip capacitor*
C3 = C16 = 4 to 40 pF film dielectric trimmer (cat. no. 2222 809 07008)
C4 = C5 = 75 pF multilayer ceramic chip capacitor
C6 = C7 = 100 pF multilayer ceramic chip capacitor*
C8 = C9 = 2 x 75 pF multilayer ceramic chip capacitors* in parallel
C10 = C13 = 39 pF multilayer ceramic chip capacitor*
C11 = 2,5 to 20 pF film dielectric trimmer (cat. no. 2222 809 07004)
C12 = 2 x 820 pF multilayer ceramic chip capacitors in parallel*
C14 = 100 nF polyester capacitor
C15 = C17 = 12 pF multilayer ceramic chip capacitor*
C18 = C19 = 470 pF multilayer ceramic chip capacitor*
C20 = 820 pF multilayer ceramic chip capacitor*

* American Technical Ceramics capacitor type 100B or capacitor of the same quality.

L1 = 1 turn silver-plated Cu-wire (2,0 mm); int. dia. 10 mm; leads 2 x 4 mm
L2 = 1 turn silver-plated Cu-wire (2,0 mm); int. dia. 1 mm; leads 2 x 6 mm
L3 = strip (14 mm x 6 mm)
L4 = strip (8 mm x 6 mm)
L5 = 100 nH, 7 turns closely wound enamelled Cu-wire (0,5 mm); int. dia. 3 mm; leads 2 x 7 mm
L6 = Ferroxcube wideband h.f. choke, grade 3B (cat. no. 4312 020 36640)
L7 = strip (12 mm x 6 mm)
L8 = silver-plated copper U-shaped inductance (7 + 15 + 7) mm x 4 mm x 0,5 mm
L9 = silver-plated copper U-shaped inductance (8 + 8,5 + 6) mm x 4 mm x 0,5 mm
L10 = modified Ferroxcube wideband h.f. choke, grade 3B (cat. no. 4312 020 36640) with 3 parallel connected Cu wires (0,8 mm)
L11 = 2 turns silver-plated Cu-wire (2,0 mm); int. dia. 9 mm; length 7,5 mm; leads 2 x 3,5 mm

L3, L4 and L7 are strips on a double Cu-clad printed-circuit board with epoxy fibre-glass dielectric, (ϵ_r = 4,5) thickness 1/16 inch).

R1 = 10 Ω ± 10%, carbon resistor
R2 = 4,7 Ω ± 10%, carbon resistor

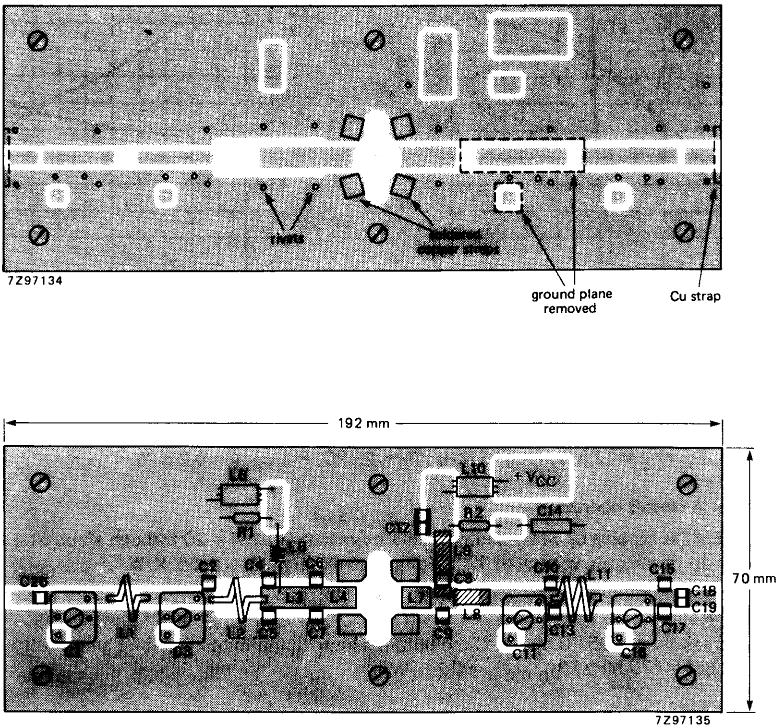


Fig. 7 Printed circuit board and component lay-out for 175 MHz class-B test circuit.

The circuit and components are on one side of the epoxy fibre-glass board. The other side, except for the area indicated by the dotted line, is unetched copper serving as a ground plane.
If the p.c.b. is in direct contact with the heatsink, the heatsink area within the dotted line has to be raised at least 0,5 mm to minimize the dielectric losses.
Earth connections are made by hollow rivets and additionally by fixing screws and copper straps under the emitters to provide a direct contact between the copper of the component side and the ground plane.

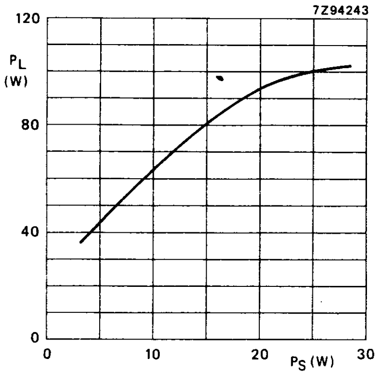


Fig. 8 Load power versus source power.

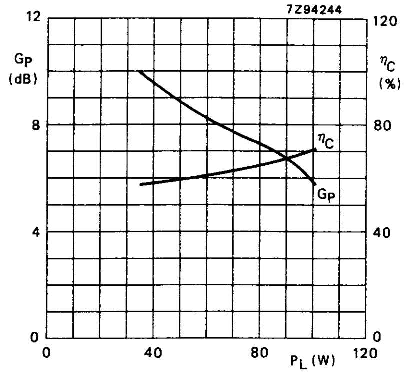


Fig. 9 Power gain and efficiency versus load power.

Condition for Figs 8 and 9:

Typical values; V_{CE} = 12,5 V; f = 175 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0,2 K/W.

Ruggedness in class-B operation

The BLV75/12 is capable of withstanding a load mismatch (VSWR = 20 through all phases) at rated load power up to a supply voltage of 12,5 V; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0,2 K/W.

Power slump

If T_h is increased from 25 °C to 70 °C the output power slump for constant P_S amounts to typ. 7% (V_{CE} = 12,5; f = 175 MHz; $R_{th\ mb\text{-}h}$ = 0,2 K/W).

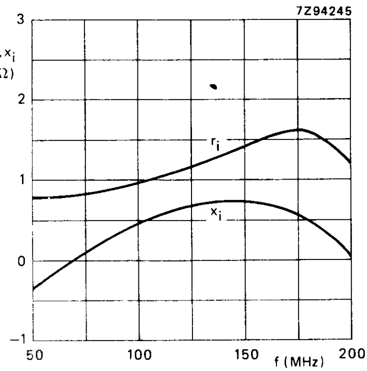


Fig. 10 Input impedance (series components).

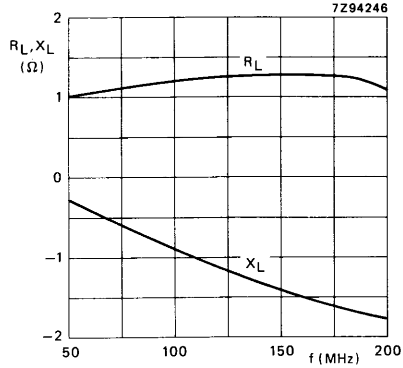


Fig. 11 Load impedance (series components).

Conditions for Figs 10, 11 and 12:

Typical values; V_{CE} = 12,5 V; P_L = 75 W; f = 50 to 200 MHz; class-B operation; $R_{th\ mb\text{-}h}$ = 0,2 K/W.

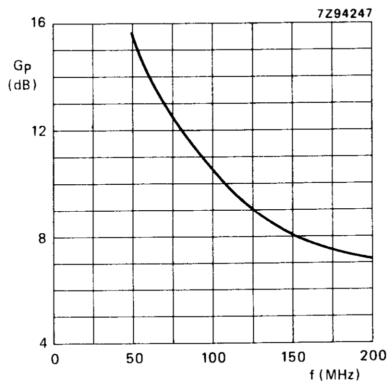


Fig. 12 Power gain versus frequency.

V.H.F. POWER TRANSISTOR

N-P-N silicon planar epitaxial transistor primarily intended for use in base stations in the v.h.f. mobile radio band.

Features:

- multi-base structure and diffused emitter ballasting resistors for an optimum temperature profile;
- gold metallization ensures excellent reliability.

The transistor has a 1/2 in. 4-lead flange envelope with a ceramic cap. All leads are isolated from the flange.

QUICK REFERENCE DATA

R.F. performance at T_h = 25 °C in a common-emitter class-B circuit

mode of operation	V_{CE} V	f MHz	P_L W	P_S W	G_p dB	η %
narrow band; c.w.	28	175	80	< 17,9	> 6,5	> 70

MECHANICAL DATA

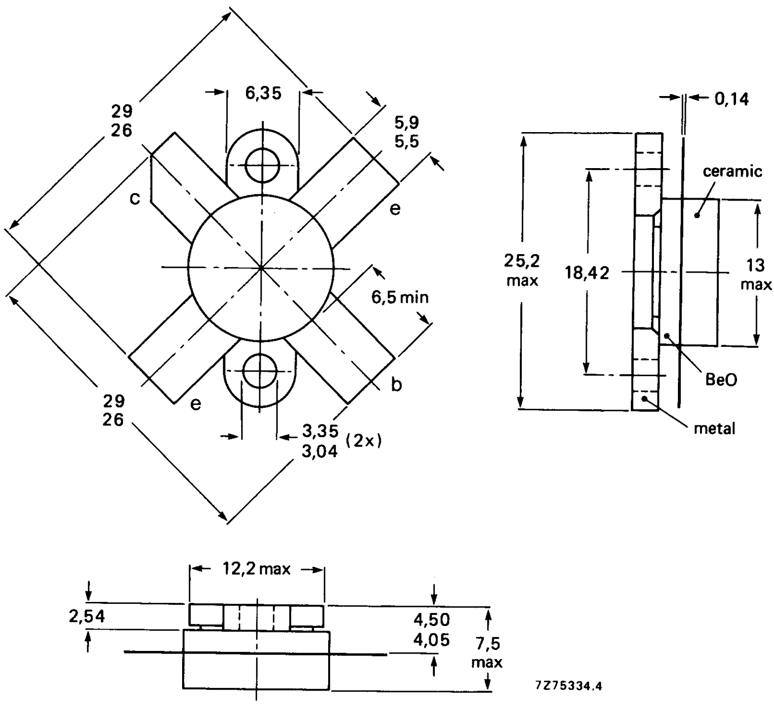
SOT-121 (see Fig. 1)

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

MECHANICAL DATA

Fig. 1 SOT-121.

Dimensions in mm



Torque on screw: min. 0,60 Nm (6,0 kg cm)
max. 0,75 Nm (7,5 kg cm)

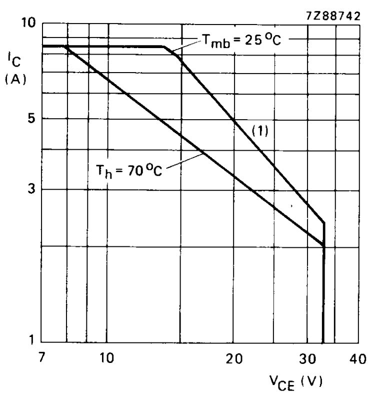
Recommended screw: cheese-head 4-40 UNC/2A

Heatsink compound must be applied sparingly and evenly distributed.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage (peak-value);			
$V_{BE} = 0$	V_{CESM}	max.	65 V
open base	V_{CEO}	max.	33 V
Emitter-base voltage (open collector)	V_{EBO}	max.	4 V
Collector current			
d.c. or average	I_C; $I_{C(AV)}$	max.	8,5 A
(peak value); f > 1 MHz	I_{CM}	max.	17,5 A
Total power dissipation at $T_{mb} = 25\ ^oC$	P_{tot}	max.	116 W
R.F. power dissipation			
f > 1 MHz; $T_{mb} = 25\ ^oC$	P_{rf}	max.	144 W
f > 1 MHz; $T_h = 70\ ^oC$	P_{rf}	max.	80 W
Storage temperature	T_{stg}		−65 to +150 °C
Operating junction temperature	T_j	max.	200 °C



(1) Second breakdown limit.

Fig. 2 D.C. SOAR.

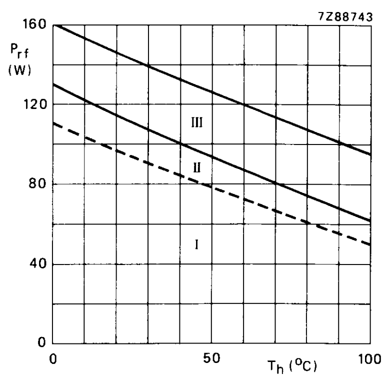


Fig. 3 Power derating curve vs. temperature.

I Continuous d.c. operation
II Continuous r.f. operation; (f > 1 MHz)
III Short-time operation during mismatch; (f > 1 MHz)

THERMAL RESISTANCE (dissipation = 90 W; $T_{mb} = 60\ ^oC$, i.e. $T_h = 33\ ^oC$)

From junction to mounting base (d.c. dissipation)	$R_{th\ j\text{-}mb(dc)}$	=	1,50 K/W
From junction to mounting base (r.f. dissipation)	$R_{th\ j\text{-}mb(rf)}$	=	1,30 K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	=	0,3 K/W

CHARACTERISTICS

T_j = 25 °C

Collector-emitter breakdown voltage			
V_{BE} = 0; I_C = 25 mA	$V_{(BR)CES}$	>	65 V
open base; I_C = 100 mA	$V_{(BR)CEO}$	>	33 V
Emitter-base breakdown voltage			
open collector; I_E = 10 mA	$V_{(BR)EBO}$	>	4 V
Collector cut-off current			
V_{BE} = 0; V_{CE} = 33 V	I_{CES}	<	10 mA
Second breakdown energy; L = 25 mH; f = 50 Hz			
open base	E_{SBO}	>	10 mJ
R_{BE} = 10 Ω	E_{SBR}	>	10 mJ
D.C. current gain*			
I_C = 3,5 A; V_{CE} = 25 V	h_{FE}	typ.	45
			15 to 100
Collector-emitter saturation voltage*			
I_C = 10 A; I_B = 2 A	V_{CEsat}	typ.	1,6 V
Transition frequency at f = 100 MHz*			
$-I_E$ = 3,5 A; V_{CB} = 25 V	f_T	typ.	575 MHz
$-I_E$ = 10 A; V_{CB} = 25 V	f_T	typ.	600 MHz
Collector capacitance at f = 1 MHz			
$I_E = I_e$ = 0; V_{CB} = 25 V	C_c	typ.	155 pF
Feedback capacitance at f = 1 MHz			
I_C = 50 mA; V_{CE} = 25 V	C_{re}	typ.	88 pF
Collector-flange capacitance	C_{cf}	typ.	4,5 pF

* Measured under pulse conditions: $t_p > 300$ μs; $\delta < 0,02$.

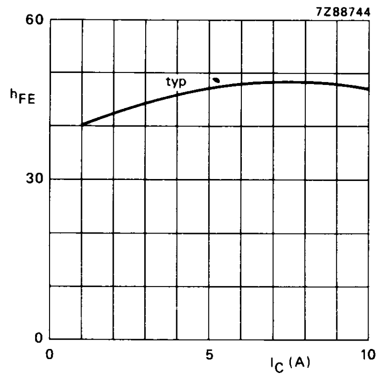


Fig. 4 V_{CE} = 25 V; T_j = 25 °C.

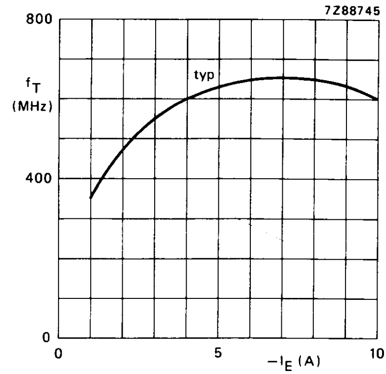


Fig. 5 V_{CB} = 25 V; f = 100 MHz; T_j = 25°C.

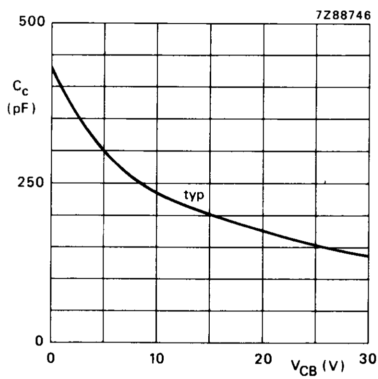


Fig. 6 I_E = I_e = 0; f = 1 MHz; T_j = 25 °C.

APPLICATION INFORMATION

R.F. performance in c.w. operation (common-emitter class-B circuit)
f = 175 MHz; T_h = 25 °C

mode of operation	V_{CE} V	P_L W	P_S W	G_P dB	I_C A	η %
narrow band; c.w.	28	80	< 17,9 typ. 16,0	> 6,5 typ. 7,0	< 4,1 typ. 3,8	> 70 typ. 75

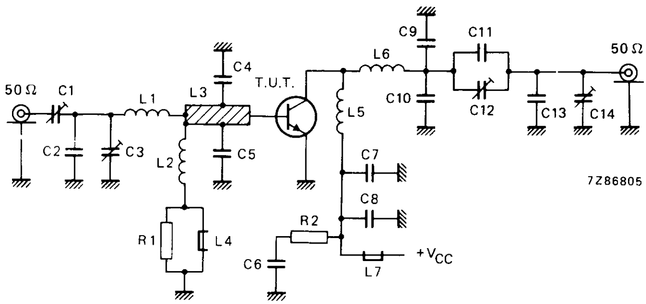


Fig. 7 Class-B test circuit at f = 175 MHz.

List of components:

C1 = C12 = C14 = 4 to 40 pF film dielectric trimmer (cat. no. 2222 809 07008)
C2 = 30 pF (500 V) multilayer ceramic chip capacitor*
C3 = 5 to 60 pF film dielectric trimmer (cat. no. 2222 809 07011)
C4 = C5 = 56 pF (500 V) multilayer ceramic chip capacitor*
C6 = 100 nF (50 V) multilayer ceramic chip capacitor
C7 = C8 = 220 pF (50 V) multilayer ceramic chip capacitor
C9 = C10 = 10 pF (500 V) multilayer ceramic chip capacitor*
C11 = 24 pF (500 V) multilayer ceramic chip capacitor*
C13 = 13 pF (500 V) multilayer ceramic chip capacitor*

L1 = Cu wire (1,8 mm); length 15 mm
L2 = 100 nH; 7 turns closely wound enamelled Cu wire (0,5 mm); int. dia. 3 mm; leads 2 x 7 mm
L3 = strip (15 mm x 8 mm); taps for C4 and C5 at 7 mm from transistor edge
L4 = L7 = Ferroxcube wide-band h.f. choke, grade 3B (cat. no. 4312 020 36640)
L5 = 1 turn Cu wire (1,8 mm); int. dia. 9 mm; leads 2 x 10 mm
L6 = 1/2 turn Cu wire (1,8 mm); int. dia. 13 mm; leads 2 x 5 mm

L3 is a strip on a double Cu-clad printed-circuit board with epoxy fibre-glass dielectric, thickness 1/16 in.

R1 = R2 = 10 Ω (± 10%) carbon resistor (0,25 W)

* American Technical Ceramics capacitors or capacitors of same quality.

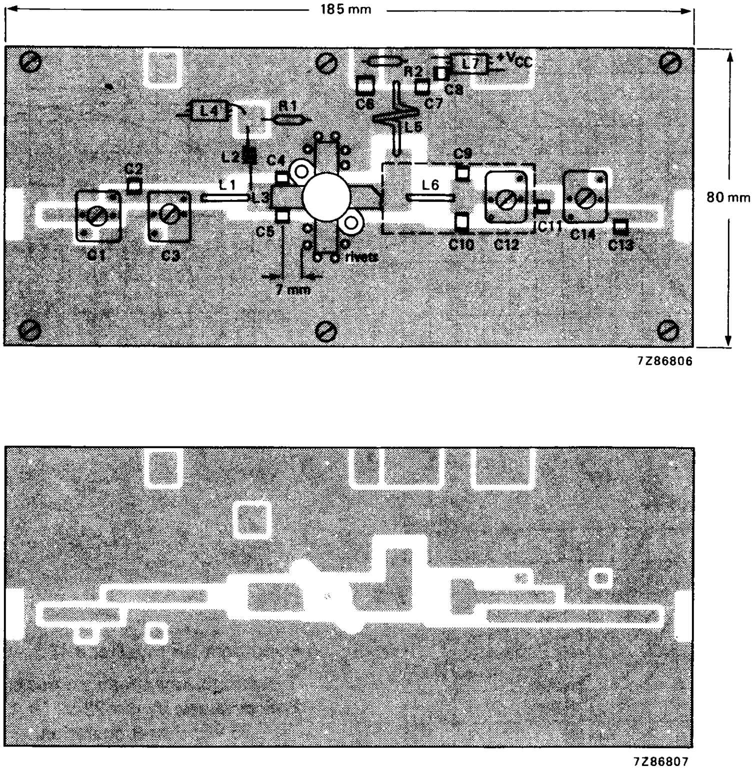


Fig. 8 Component layout and printed-circuit board for 175 MHz.

The circuit and the components are on one side of the epoxy fibre-glass board, the other side is unetched copper to serve as ground-plane. Earth connections are made by hollow rivets and additionally by fixing screws and copper straps at the input and output to provide direct contact between the copper on the component side and the ground-plane.

To minimize the dielectric losses, the ground-plane under the interconnections of L6, C9, C10, C11 and C12 has been removed.

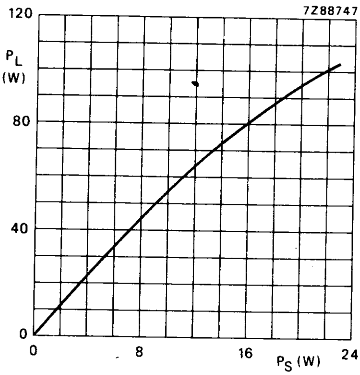


Fig. 9 Load power as a function of source power.

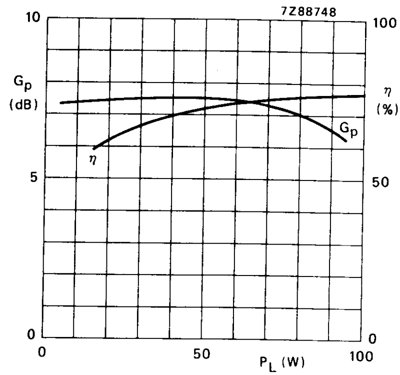


Fig. 10 Power gain and efficiency as a function of load power.

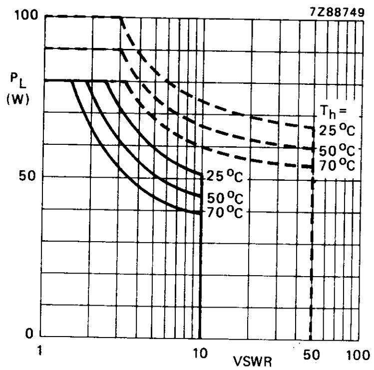


Fig. 11 R.F. SOAR at V_{CE} = 28 V.
——— f > 1 MHz (continuous);
- - - - short time operation during mismatch (f > 1 MHz).

Conditions for Figs 9 and 10:

Test circuit tuned for each power level; typical values; V_{CE} = 28 V; f = 175 MHz; T_h = 25 °C; class-B operation.

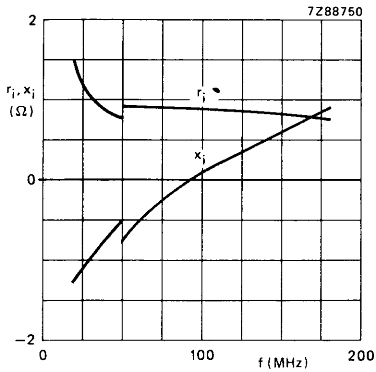


Fig. 12 Input impedance (series components).

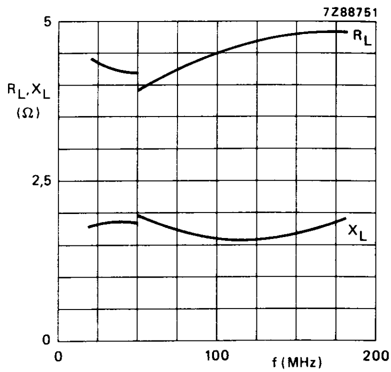


Fig. 13 Load impedance (series components).

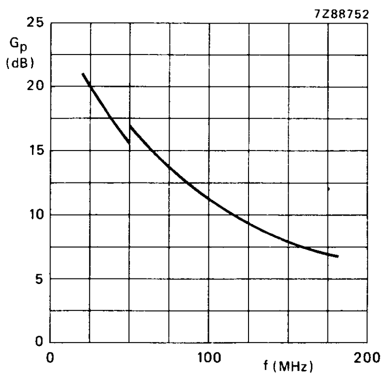


Fig. 14 Power gain as a function of frequency.

Conditions for Figs 12, 13 and 14:

Typical values; V_{CE} = 28 V; P_L = 80 W; T_h = 25 °C; class-B operation.

OPERATING NOTE for Figs 12, 13 and 14:

Below 50 MHz a base-emitter resistor of 4,7 Ω is recommended to avoid oscillation. This resistor must be effective for r.f. only.