U.H.F. POWER TRANSISTOR

N-P-N silicon planar epitaxial transistor designed for use in mobile radio transmitters in the 900 MHz band.

Features:

- diffused emitter-ballasting resistors for an optimum temperature profile
- gold metallization ensures excellent reliability.

The transistor has a 4-lead stud envelope with a ceramic cap (SOT-172). All leads are isolated from the stud.

QUICK REFERENCE DATA

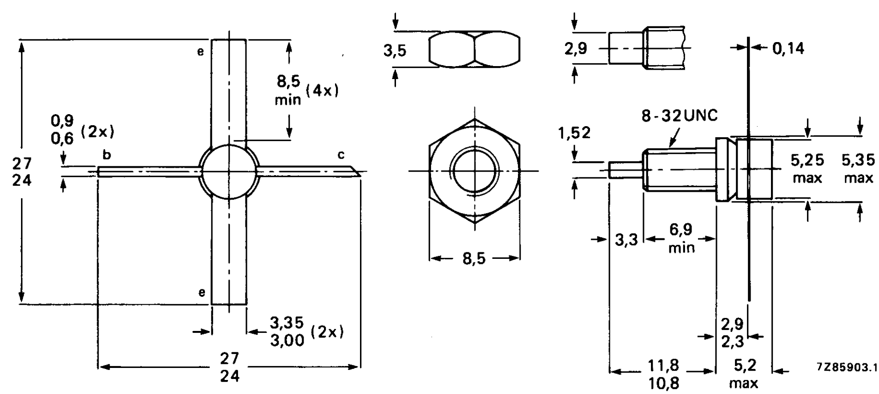
R.F. performance at T_h = 25 °C in a common-emitter class-B circuit

mode of operation	V_{CE} V	f MHz	P_L W	G_p dB	η_C %
narrow band; c.w.	12,5	900	1	> 7,5	> 50
	9,6	900	0,75	typ. 7,9	typ. 61

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-172A1.



Torque on nut: min. 0,75 Nm (7,5 kg.cm)
max. 0,85 Nm (8,5 kg.cm)

When locking is required an adhesive is preferred instead of a lock washer.

Diameter of clearance hole in heatsink: max. 4,2 mm. Mounting hole to have no burrs at either end. Deburring must leave surface flat; donot chamfer or countersink either end of hole.

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-base voltage (open emitter)	V_{CBO}	max.	36 V
Collector-emitter voltage (open base)	V_{CEO}	max.	16 V
Emitter-base voltage (open collector)	V_{EBO}	max.	3 V
Collector current			
d.c. or average	I_C; $I_{C(AV)}$	max.	0,2 A
(peak value); f > 1 MHz	I_{CM}	max.	0,6 A
D.C. power dissipation			
at T_{mb} = 115 °C	$P_{tot(dc)}$	max.	2,25 W
R.F. power dissipation			
f > 1 MHz; T_{mb} = 105 °C	$P_{tot(rf)}$	max.	3,5 W
Storage temperature	T_{stg}	−65 to + 150	°C
Operating junction temperature	T_j	max.	200 °C

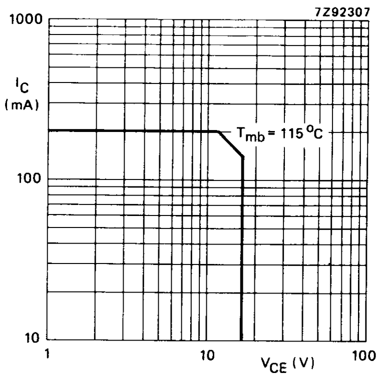


Fig. 2 D.C. SOAR.

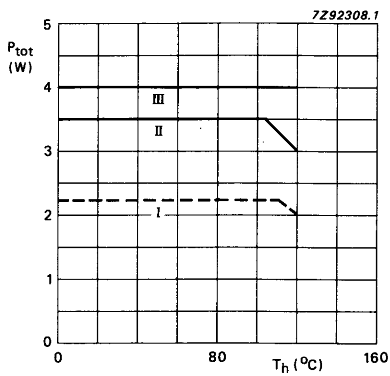


Fig. 3 Power/temperature derating curves.
I Continuous d.c. operation
II Continuous r.f. operation (f > 1 MHz)
III Short-time r.f. operation during mismatch (f > 1 MHz)

THERMAL RESISTANCE

Dissipation = 2,25 W; T_{mb} = 25 °C.

From junction to mounting base			
(d.c. dissipation)	$R_{th\ j\text{-}mb(d.c.)}$	max.	25 K/W
(r.f. dissipation)	$R_{th\ j\text{-}mb(r.f.)}$	max.	19 K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	max.	0,8 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-base breakdown voltage, open emitter; I_C = 2,5 mA	$V_{(BR)CBO}$	>	36 V
Collector-emitter breakdown voltage, open base; I_C = 10 mA	$V_{(BR)CEO}$	>	16 V
Emitter-base breakdown voltage, open collector; I_E = 0,5 mA	$V_{(BR)EBO}$	>	3 V
Collector cut-off current, V_{BE} = 0; V_{CE} = 16 V	I_{CES}	<	1 mA
Second breakdown energy, L = 25 mH; f = 50 Hz; R_{BE} = 10 Ω	E_{SBR}	>	0,3 mJ
D.C. current gain, I_C = 0,15 A; V_{CE} = 10 V	h_{FE}	>	25
Transition frequency at f = 500 MHz*, $-I_E$ = 0,15 A; V_{CB} = 12,5 V	f_T	typ.	4,8 GHz
$-I_E$ = 0,5 A; V_{CB} = 12,5 V	f_T	typ.	1,4 GHz
Collector capacitance at f = 1 MHz, $I_E = i_e$ = 0; V_{CB} = 12,5 V	C_c	typ.	1,8 pF
Feedback capacitance at f = 1 MHz, I_C = 0; V_{CE} = 12,5 V	C_{re}	typ.	1,0 pF
Collector-stud capacitance	C_{cs}	typ.	0,5 pF

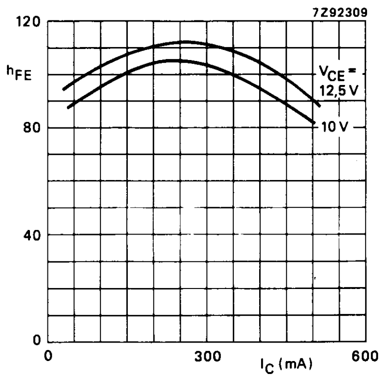


Fig. 4 T_j = 25 °C; typical values.

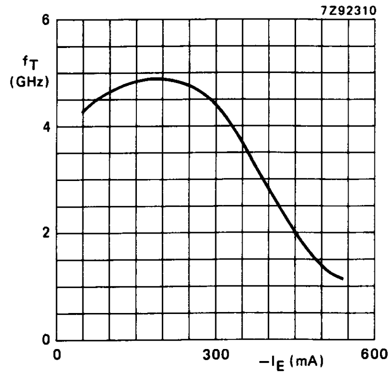


Fig. 5 V_{CB} = 12,5 V; f = 500 MHz; T_j = 25 °C; typical values.

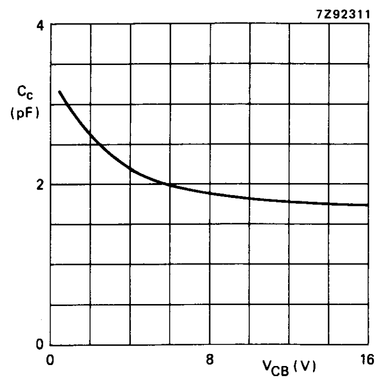


Fig. 6 $I_E = i_e$ = 0; f = 1 MHz; typical values.

* Measured under pulse conditions: t_p = 50 μs; δ < 1%.

APPLICATION INFORMATION

R.F. performance in c.w. operation (common-emitter circuit; class-B): f = 900 MHz; T_h = 25 °C.

mode of operation	V_{CE} V	P_L W	P_S W	G_P dB	I_C A	η_C %
narrow band; c.w.	12,5	1	< 0,178 typ. 0,126	> 7,5 typ. 9,0	< 0,160 typ. 0,133	> 50 typ. 60
	9,6	0,75	typ. 0,122	typ. 7,9	typ. 0,128	typ. 61

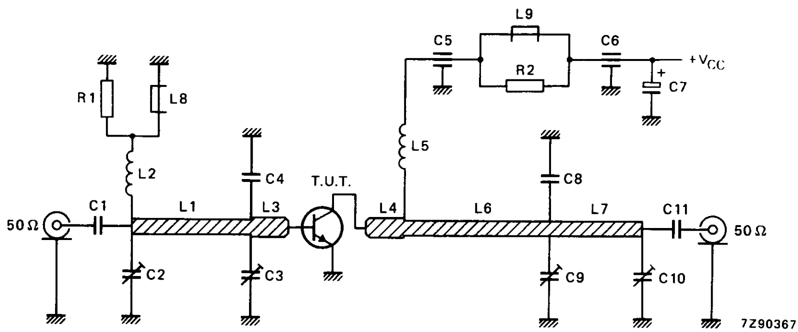


Fig. 7 Class-B test circuit at f = 900 MHz.

List of components:

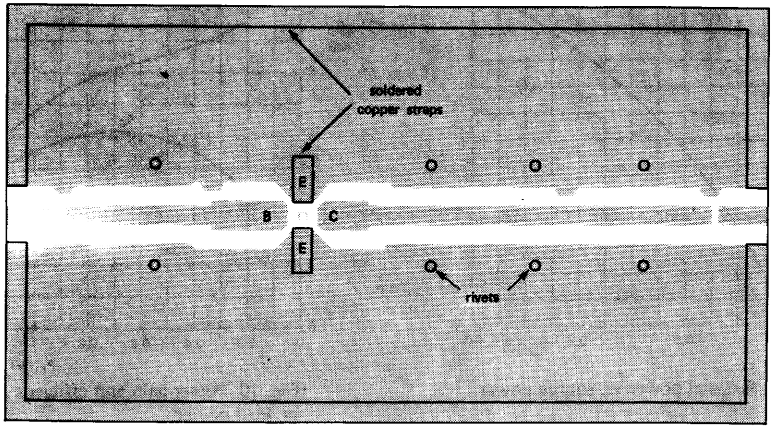
C1 = C11 = 33 pF multilayer ceramic chip capacitor
C2 = C10 = 1,4 to 5,5 pF film dielectric trimmer (cat. no. 2222 809 09001)
C3 = C9 = 1,2 to 3,5 pF film dielectric trimmer (cat. no. 2222 809 05001)
C4 = 5,6 pF multilayer ceramic chip capacitor*
C5 = 10 pF ceramic feed-through capacitor
C6 = 330 pF ceramic feed-through capacitor
C7 = 2,2 μF (35 V) tantalum electrolytic capacitor
C8 = 3,9 pF multilayer ceramic chip capacitor*

L1 = L7 = 50 Ω stripline (28,2 mm x 4,0 mm)
L2 = 60 nH; 4 turns closely wound enamelled Cu wire (0,4 mm); int. dia. 3 mm; leads 2 x 5 mm
L3 = 38 Ω stripline (14,6 mm x 6,0 mm)
L4 = 38 Ω stripline (10,0 mm x 6,0 mm)
L5 = 280 nH; 15 turns closely wound enamelled Cu wire (0,4 mm); int. dia. 3 mm; leads 2 x 5 mm
L6 = 50 Ω stripline (37,7 mm x 4,0 mm)
L8 = L9 = Ferroxcube wideband h.f. choke, grade 3B (cat. no. 4312 020 36642)

R1 = R2 = 10 Ω ± 10%; 0,25 W metal film resistor

L1, L3, L4, L6 and L7 are striplines on a double Cu-clad printed circuit board with P.T.F.E. fibre-glass dielectric (ϵ_r = 2,74); thickness 1/16 inch.

* American Technical Ceramics capacitor type 100A or capacitor of same quality.



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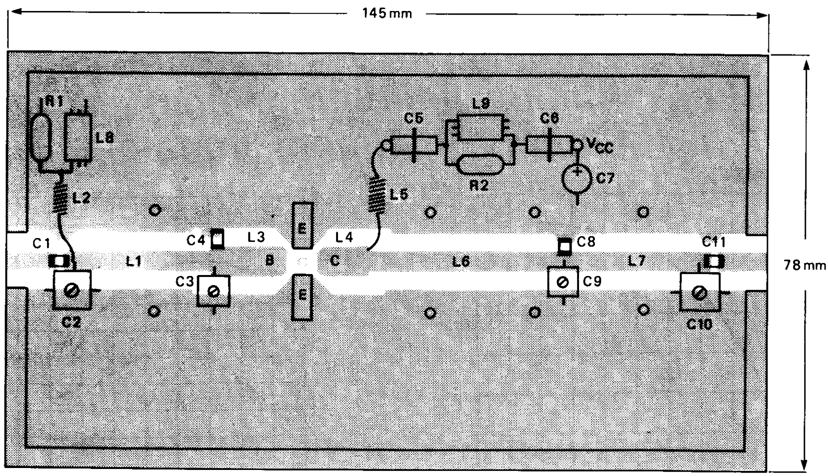

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Fig. 8 Printed circuit board and component lay-out for 900 MHz class-B test circuit.

Note

The circuit and the components are on one side of the P.T.F.E. fibre-glass board; the other side is unetched copper serving as ground plane. Earth connections are made by hollow rivets and also by fixing-screws and copper straps around the board and under the emitters to provide a direct contact between the copper on the component side and the ground plane.

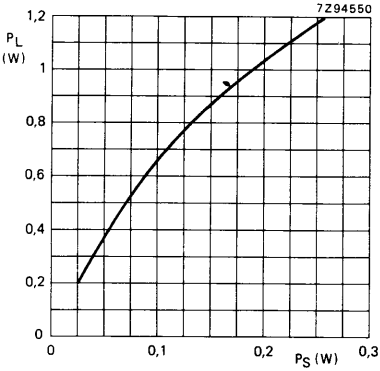

Fig. 9 Load power vs. source power.

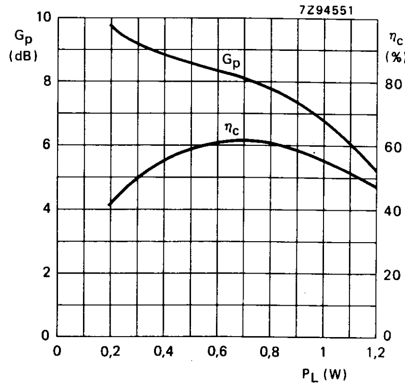

Fig. 10 Power gain and efficiency vs. load power.

Conditions for Figs 9 and 10:
V_{CE} = 9,6 V; f = 900 MHz; T_h = 25 °C; class-B operation; typical values.

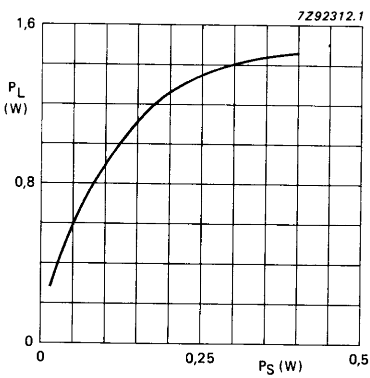

Fig. 11 Input impedance (series components).

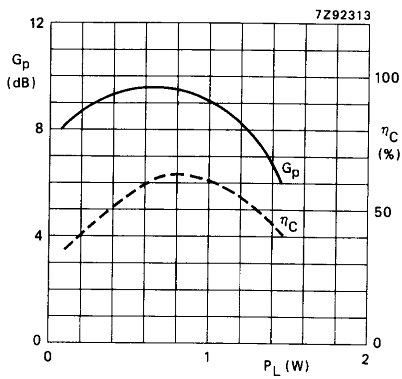

Fig. 12 Load impedance (series components).

Conditions for Figs 11 and 12:
V_{CE} = 12,5 V; P_L = 1 W; f = 900 MHz; T_h = 25 °C; class-B operation; typical values.

RUGGEDNESS

The device is capable to withstand a full load mismatch (VSWR = 50; all phases) at rated load power up to a supply voltage of 15,5 V at T_h = 25 °C.

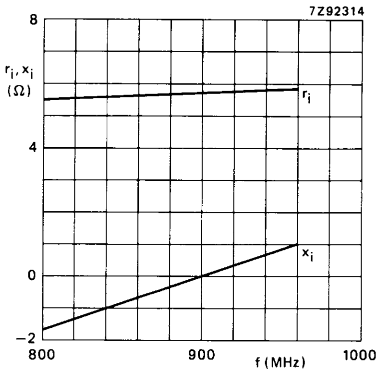

Fig. 13 Input impedance (series components).

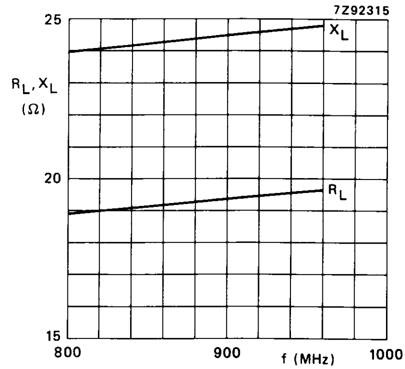

Fig. 14 Load impedance (series components).

Conditions for Figs 13 and 14:
V_{CE} = 12,5 V; P_L = 1 W; f = 800–960 MHz; T_h = 25 °C; class-B operation; typical values.

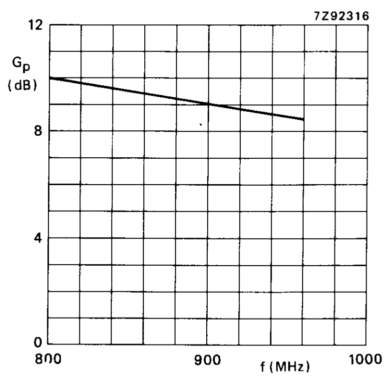

Fig. 15 Power gain vs. frequency.
V_{CE} = 12,5 V; P_L = 1 W; f = 800–960 MHz; T_h = 25 °C; class-B operation; typical values.

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N-P-N silicon planar epitaxial transistor designed for use in mobile radio transmitters in the 900 MHz band.

Features:

- multi-base structure and diffused emitter-ballasting resistors for an optimum temperature profile
- gold metallization ensures excellent reliability.

The transistor has a 4-lead stud envelope with a ceramic cap (SOT-172). All leads are isolated from the stud.

QUICK REFERENCE DATA

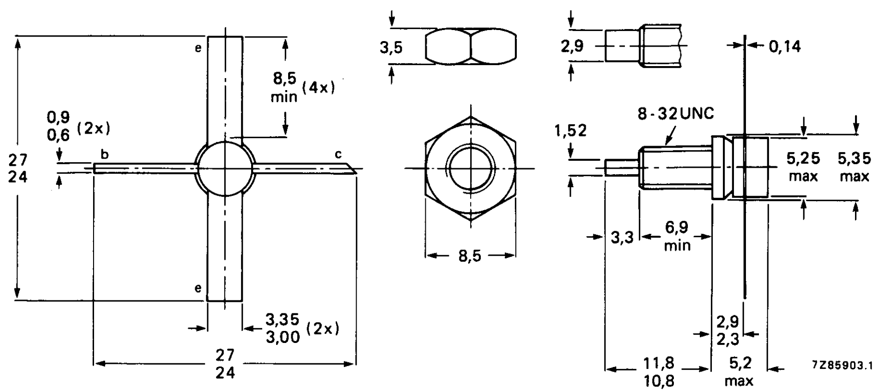
R.F. performance at T_h = 25 °C in a common-emitter class-B circuit

mode of operation	V_{CE} V	f MHz	P_L W	G_p dB	η_C %
narrow band; c.w.	12,5	900	2	> 6,5	> 50
	9,6	900	1,5	typ. 6,6	typ. 60

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-172A1.



Torque on nut: min. 0,75 Nm
(7,5 kg.cm)
max. 0,85 Nm
(8,5 kg.cm)

When locking is required an adhesive is preferred instead of a lock washer.

Diameter of clearance hole in heatsink: max. 4,2 mm.
Mounting hole to have no burrs at either end.
Deburring must leave surface flat; donot chamfer or countersink either end of hole.

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-base voltage (open emitter)	V_{CBO}	max.	36 V
Collector-emitter voltage (open base)	V_{CEO}	max.	16 V
Emitter-base voltage (open collector)	V_{EBO}	max.	3 V
Collector current			
d.c. or average	I_C; $I_{C(AV)}$	max.	0,4 A
(peak value); f > 1 MHz	I_{CM}	max.	1,2 A
D.C. power dissipation at T_{mb} = 90 °C	$P_{tot(dc)}$	max.	4,5 W
R.F. power dissipation f > 1 MHz; T_{mb} = 90 °C	$P_{tot(rf)}$	max.	6 W
Storage temperature	T_{stg}		−65 to + 150 °C
Operating junction temperature	T_j	max.	200 °C

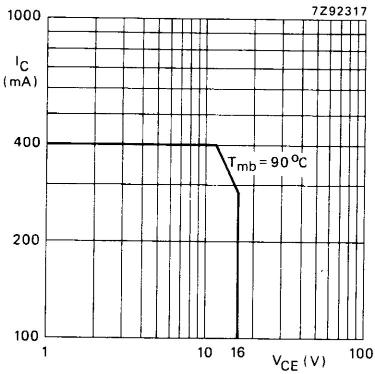


Fig. 2 D.C. SOAR.

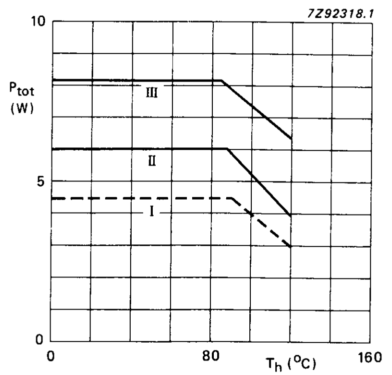


Fig. 3 Power/temperature derating curves
I Continuous d.c. operation
II Continuous r.f. operation (f > 1 MHz)
III Short-time r.f. operation during mismatch (f > 1 MHz)

THERMAL RESISTANCE

Dissipation = 4,5 W; T_{mb} = 25 °C

From junction to mounting base			
(d.c. dissipation)	$R_{th\ j\text{-}mb(d.c.)}$	max.	20 K/W
(r.f. dissipation)	$R_{th\ j\text{-}mb(d.c.)}$	max.	15 K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	max.	0,8 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-base breakdown voltage, open emitter; I_C = 5 mA	$V_{(BR)CBO}$	>	36 V
Collector-emitter breakdown voltage, open base; I_C = 10 mA	$V_{(BR)CEO}$	>	16 V
Emitter-base breakdown voltage, open collector; I_E = 0,5 mA	$V_{(BR)EBO}$	>	3 V
Collector cut-off current, V_{BE} = 0; V_{CE} = 16 V	I_{CES}	<	2,5 mA
Second breakdown energy, L = 25 mH; f = 50 Hz; R_{BE} = 10 Ω	E_{SBR}	>	0,55 mJ
D.C. current gain, I_C = 0,3 A; V_{CE} = 10 V	h_{FE}	>	25
Transition frequency at f = 500 MHz*, $-I_E$ = 0,3 A; V_{CB} = 12,5 V	f_T	typ.	4 GHz
$-I_E$ = 1,0 A; V_{CB} = 12,5 V	f_T	typ.	1 GHz
Collector capacitance at f = 1 MHz, $I_E = i_e$ = 0; V_{CB} = 12,5 V	C_c	typ.	3,5 pF
Feed-back capacitance at f = 1 MHz, I_C = 0; V_{CE} = 12,5 V	C_{re}	typ.	2,0 pF
Collector-stud capacitance	C_{cs}	typ.	0,5 pF

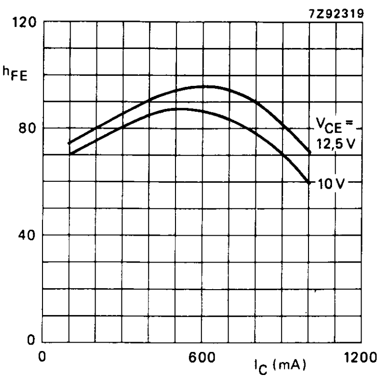


Fig. 4 T_j = 25 °C; typical values.

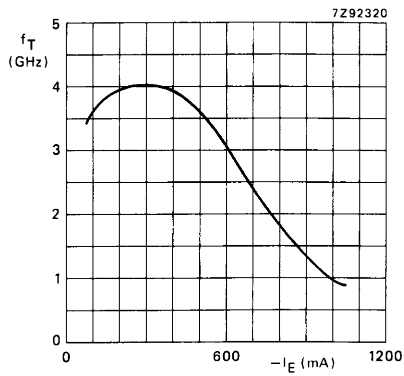


Fig. 5 V_{CB} = 12,5 V; t_p = 50 μs; T_j = 25 °C; typical values.

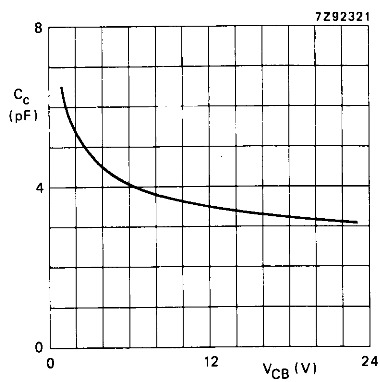


Fig. 6 $I_E = i_e$ = 0; f = 1 MHz; typical values.

* Measured under pulse conditions: t_p = 50 μs; δ < 1%.

APPLICATION INFORMATION

R.F. performance in c.w. operation (common-emitter circuit; class-B): f = 900 MHz; T_h = 25 °C.

mode of operation	V_{CE}	P_L W	P_S W	G_P dB	I_C A	η_C %
narrow band; c.w.	12,5	2	< 0,450 typ. 0,332	> 6,5 typ. 7,8	< 0,320 typ. 0,267	> 50 typ. 60
	9,6	1,5	typ. 0,328	typ. 6,6	typ. 0,260	typ. 60

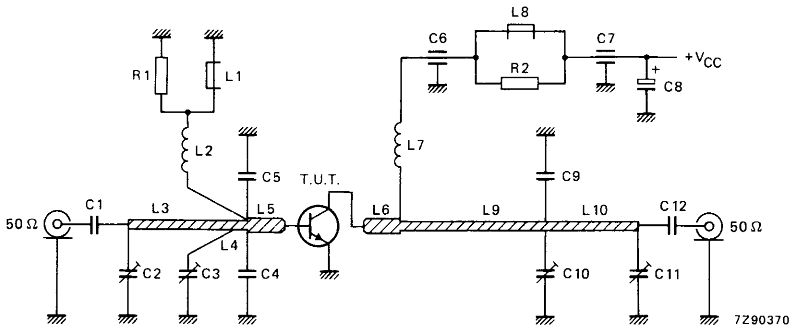


Fig. 7 Class-B test circuit at f = 900 MHz.

List of components:

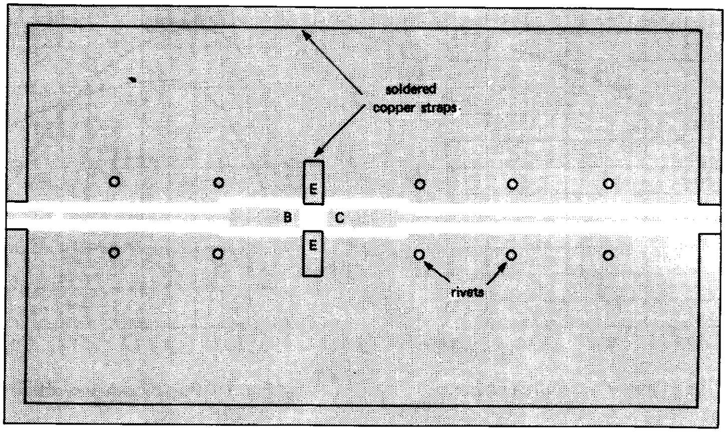
C1 = C12 = 33 pF multilayer ceramic chip capacitor
C2 = C3 = C11 = 1,4 to 5,5 pF film dielectric trimmer (cat. no. 2222 809 09001)
C4 = C5 = 5,6 pF multilayer ceramic chip capacitor*
C6 = 10 pF ceramic feed-through capacitor
C7 = 330 pF ceramic feed-through capacitor
C8 = 2,2 μF (35 V) tantalum electrolytic capacitor
C9 = 3,9 pF multilayer ceramic chip capacitor*
C10 = 1,2 to 3,5 pF film dielectric trimmer (cat. no. 2222 809 05001)

L1 = L8 = Ferroxcube wideband h.f. choke, grade 3B (cat. no. 4312 020 36642)
L2 = 60 nH; 4 turns closely wound enamelled Cu wire (0,4 mm); int. dia. 3 mm; leads 2 x 5 mm
L3 = 50 Ω stripline (23,3 mm x 1,85 mm)
L4 = 50 Ω stripline (4,0 mm x 1,85 mm)
L5 = L6 = 29 Ω stripline (14,0 mm x 4,0 mm)
L7 = 280 nH; 15 turns closely wound enamelled Cu wire (0,4 mm); int. dia. 3 mm; leads 2 x 5 mm
L9 = 50 Ω stripline (22,7 mm x 1,85 mm)
L10 = 50 Ω stripline (28,0 mm x 1,85 mm)

R1 = R2 = 10 Ω ± 10%; 0,25 W metal film resistor

L3, L4, L5, L6, L9 and L10 are striplines on a double Cu-clad printed circuit board with P.T.F.E. fibre-glass dielectric (ϵ_r = 2,74); thickness 1/32 inch.

* American Technical Ceramics capacitor type 100A or capacitor of same quality.



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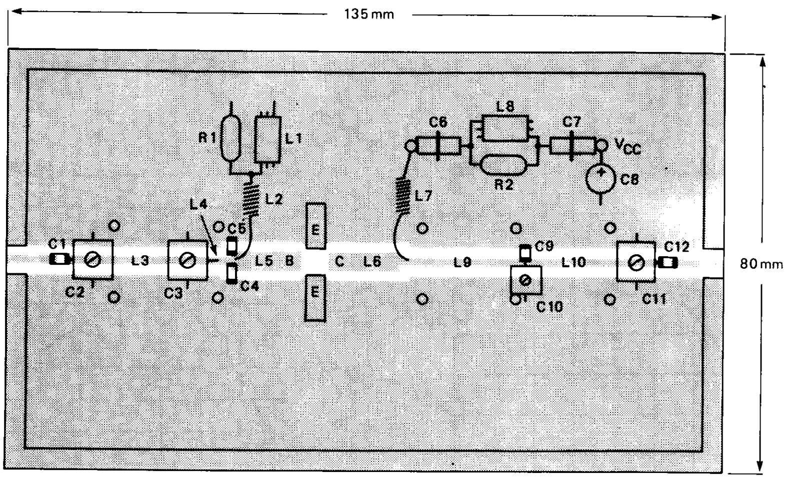

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Fig. 8 Printed circuit board and component lay-out for 900 MHz class-B test circuit.

Note

The circuit and the components are on one side of the P.T.F.E. fibre-glass board; the other side is unetched copper serving as ground plane. Earth connections are made by hollow rivets and also by fixing-screws and copper straps around the board and under the emitters to provide a direct contact between the copper on the component side and the ground plane.

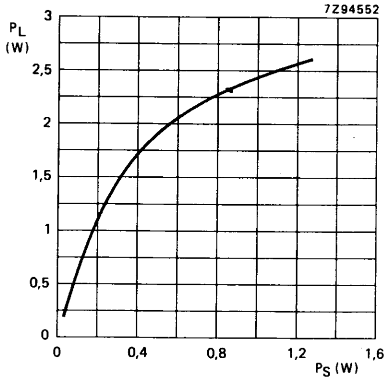


Fig. 9 Load power vs. source power.

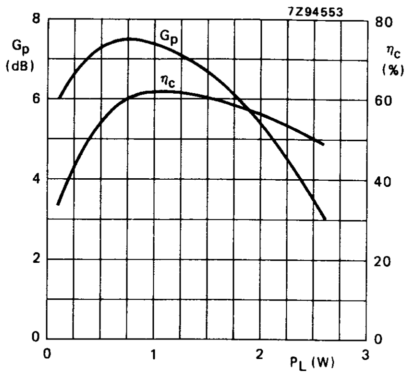


Fig. 10 Power gain and efficiency vs. load power.

Conditions for Figs 9 and 10:
V_{CE} = 9,6 V; f = 900 MHz; T_h = 25 °C; class-B operation; typical values.

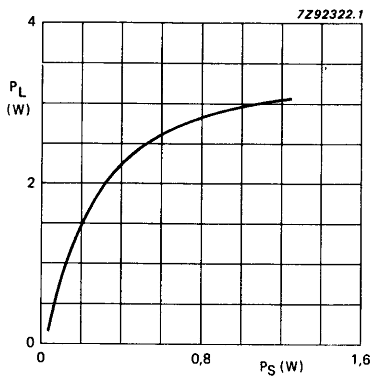


Fig. 11 Input impedance (series components).

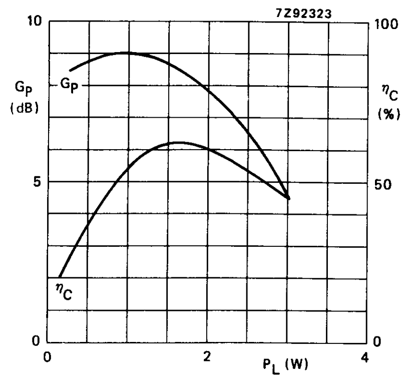


Fig. 12 Load impedance (series components).

Conditions for Figs 11 and 12:
V_{CE} = 12,5 V; P_L = 2 W; f = 900 MHz; T_h = 25 °C; class-B operation; typical values.

RUGGEDNESS

The device is capable to withstand a full load mismatch (VSWR = 50; all phases) at rated load power up to a supply voltage of 15,5 V at T_h = 25 °C.

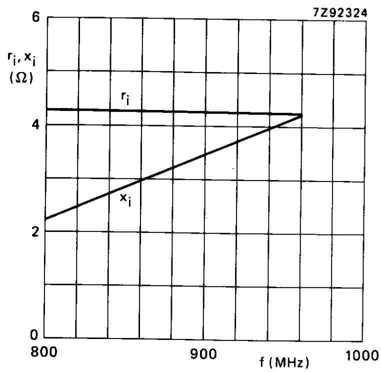


Fig. 13 Input impedance (series components).

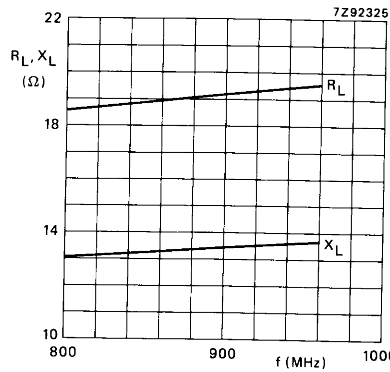


Fig. 14 Load impedance (series components).

Conditions for Figs 13 and 14:
V_{CE} = 12,5 V; P_L = 2 W; f = 800–960 MHz; T_h = 25 °C; class-B operation; typical values.

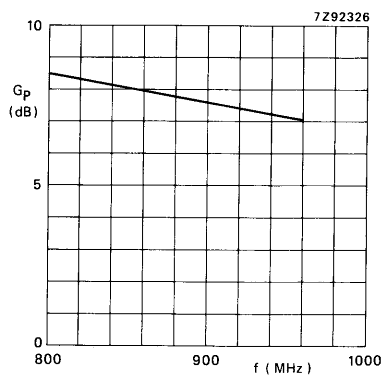


Fig. 15 Power gain vs. frequency.
V_{CE} = 12,5 V; P_L = 2 W; f = 800–960 MHz; T_h = 25 °C; class-B operation; typical values.

U.H.F. POWER TRANSISTOR

N-P-N silicon planar epitaxial transistor primarily intended for use in mobile radio transmitters in the 900 MHz communications band.

Features:

- multi-base structure and emitter-ballasting resistors for an optimum temperature profile
- internal input matching to achieve an optimum wideband capability and high power gain
- gold metallization ensures excellent reliability.

The transistor has a 6-lead flange envelope with a ceramic cap (SOT-171). All leads are isolated from the flange.

QUICK REFERENCE DATA

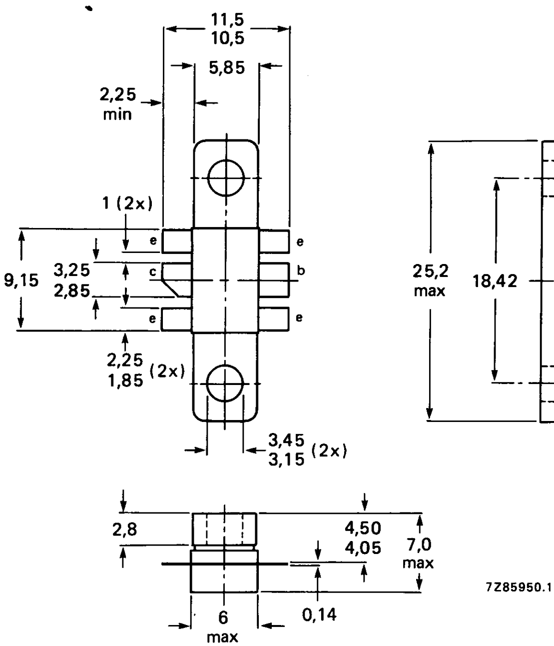
R.F. performance at T_h = 25 °C in a common-emitter class-B test circuit

mode of operation	V_{CE} V	f MHz	P_L W	G_p dB	η_C %
narrow band; c.w.	12,5	900	4	> 7,5	> 50
	9,6	900	3	typ. 7,3	typ. 56

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

MECHANICAL DATA Dimensions in mm

Fig. 1 SOT-171.



Torque on screw: min. 0,6 Nm (6 kg.cm)
max. 0,75 Nm (7,5 kg.cm)

Recommended screw: cheese-head 4-40 UNC/2A.

Heatsink compound must be applied sparingly and evenly distributed.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-base voltage (open emitter)				
peak value	V_{CBOM}	max.	36	V
Collector-emitter voltage (open base)	V_{CEO}	max.	16	V
Emitter-base voltage (open collector)	V_{EBO}	max.	3	V
Collector current				
d.c. or average	I_C	max.	0,8	A
(peak value); f > 1 MHz	I_{CM}	max.	2,4	A
Total power dissipation				
at T_{mb} = 94 °C	$P_{tot(dc)}$	max.	9	W
at T_{mb} = 94 °C; f > 1 MHz	$P_{tot(rf)}$	max.	12	W
Storage temperature	T_{stg}	−65 to + 150		°C
Operating junction temperature	T_j	max.	200	°C

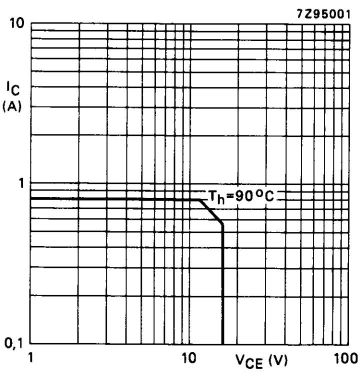


Fig. 2 D.C. SOAR.
$R_{th\ mb\text{-}h}$ = 0,4 K/W.

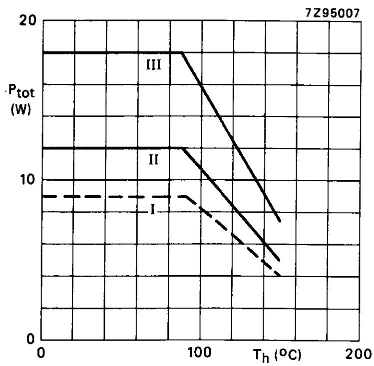


Fig. 3 Power/temperature derating curves.

I Continuous operation
II Continuous operation (f > 1 MHz)
III Short-time operation during mismatch; (f > 1 MHz)

THERMAL RESISTANCE

Dissipation = 6 W; T_{mb} = 128 °C

From junction to mounting base				
(d.c. dissipation)	$R_{th\ j\text{-}mb(dc)}$	max.	12	K/W
(r.f. dissipation)	$R_{th\ j\text{-}mb(rf)}$	max.	9	K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	max.	0,4	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-base breakdown voltage, open emitter; I_C = 10 mA	$V_{(BR)CBO}$	>	36 V
Collector-emitter breakdown voltage, open base; I_C = 20 mA	$V_{(BR)CEO}$	>	16 V
Emitter-base breakdown voltage, open collector; I_E = 1 mA	$V_{(BR)EBO}$	>	3 V
Collector cut-off current, V_{BE} = 0; V_{CE} = 16 V	I_{CES}	<	5 mA
Second breakdown energy, L = 25 mH; f = 50 Hz; R_{BE} = 10 Ω	E_{SBR}	>	1 mJ
D.C. current gain, I_C = 0,6 A; V_{CE} = 10 V	h_{FE}	>	25
Transition frequency at f = 500 MHz*, $-I_E$ = 0,6 A; V_{CE} = 12,5 V	f_T	typ.	4 GHz
Collector capacitance at f = 1 MHz, $I_E = i_e$ = 0; V_{CB} = 12,5 V	C_c	typ.	8 pF
Feed-back capacitance at f = 1 MHz, I_C = 0; V_{CE} = 12,5 V	C_{re}	typ.	5 pF
Collector-flange capacitance	C_{cf}	typ.	2 pF

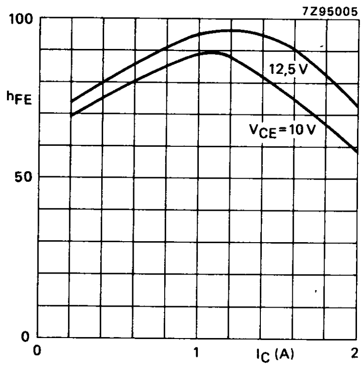


Fig. 4 T_j = 25 °C; typical values.

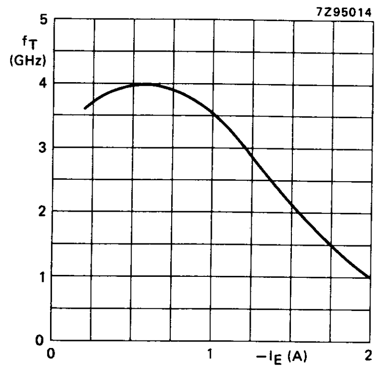


Fig. 5 V_{CB} = 12,5 V; f = 500 MHz; T_j = 25 °C; typical values.

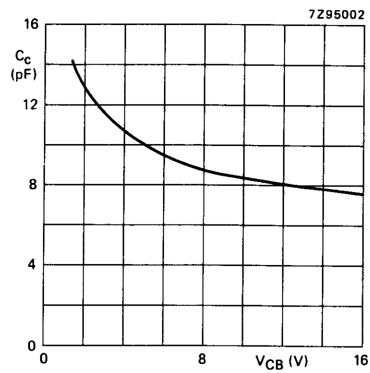


Fig. 6 $I_E = i_e$ = 0; f = 1 MHz; typical values.

* Measured under pulse conditions: t_p = 50 μs; δ < 1%.

APPLICATION INFORMATION

R.F. performance in c.w. operation (common-emitter circuit; class-B): f = 900 MHz; T_h = 25 °C.

mode of operation	V_{CE} V	P_L W	P_S W	G_P dB	I_C A	η_C %
narrow band; c.w.	12,5	4	< 0,71 typ. 0,57	> 7,5 typ. 8,5	< 0,64 typ. 0,56	> 50 typ. 57
	9,6	3	typ. 0,56	typ. 7,3	typ. 0,56	typ. 56

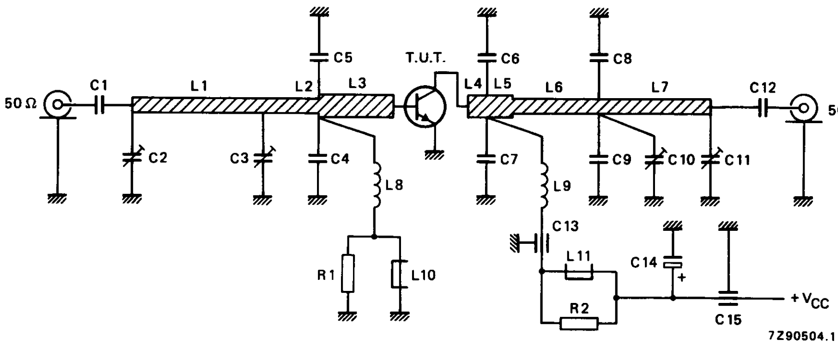


Fig. 7 Class-B test circuit at f = 900 MHz.

List of components:

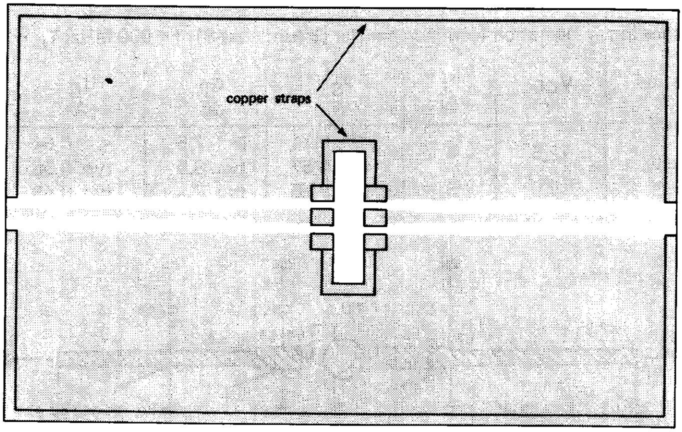
C1 = C12 = 33 pF multilayer ceramic chip capacitor
C2 = C3 = C10 = C11 = 1,4 to 5,5 pF film dielectric trimmer
(cat. no. 2222 809 09001)
C4 = C5 = 3,9 pF multilayer ceramic chip capacitor*
C6 = C7 = C8 = C9 = 6,2 pF multilayer ceramic chip capacitor*
C13 = 10 pF ceramic feed-through capacitor
C14 = 6,8 μF (63 V) electrolytic capacitor
C15 = 330 pF ceramic feed-through capacitor

L1 = 50 Ω stripline (29,5 mm x 2,4 mm)
L2 = 50 Ω stripline (5,5 mm x 2,4 mm)
L3 = 42,7 Ω stripline (16,8 mm x 3,0 mm)
L4 = 42,7 Ω stripline (7,5 mm x 3,0 mm)
L5 = 42,7 Ω stripline (2,0 mm x 3,0 mm)
L6 = 50 Ω stripline (8,5 mm x 2,4 mm)
L7 = 50 Ω stripline (28,0 mm x 2,4 mm)
L8 = 60 nH; 4 turns closely wound enamelled Cu-wire (0,4 mm); int. dia. 3 mm; leads 2 x 5 mm
L9 = 45 nH; 4 turns enamelled Cu-wire (1,0 mm); length 6 mm; int. dia. 4 mm; leads 2 x 5 mm
L10 = L11 = Ferroxcube wideband h.f. choke, grade 3B (cat. no. 4312 020 36642)

R1 = R2 = 10 Ω ± 10%; 0,25 W; metal film resistor

L1 to L7 are striplines on a double Cu-clad printed circuit board with P.T.F.E. fibre-glass dielectric (ϵ_r = 2,2); thickness 1/32 inch.

* American Technical Ceramics capacitors type 100A or capacitor of same quality.



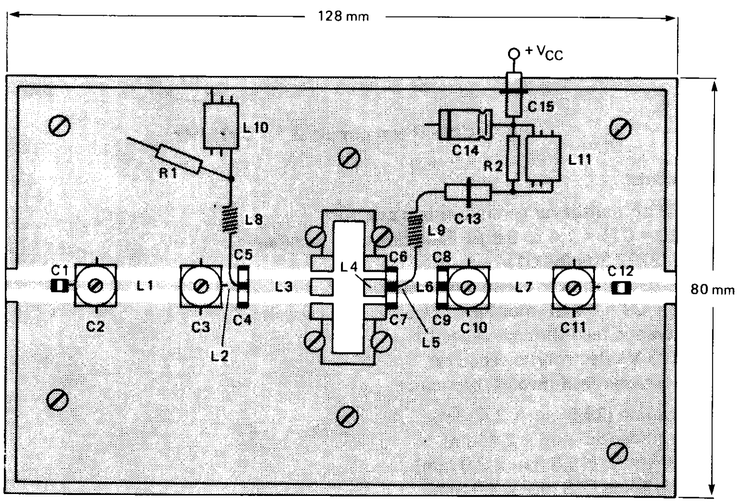


Fig. 8 Printed circuit board and component lay-out for 900 MHz class-B test circuit.

Note

The circuit and the components are on one side of the P.T.F.E. fibre-glass board; the other side is unetched copper serving as ground plane. Earth connections are made by fixing screws and copper straps around the board and under the emitters to provide a direct contact between the copper on the component side and the ground plane.

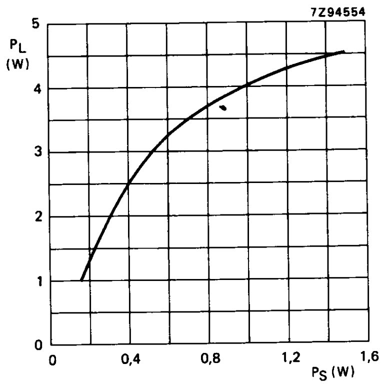


Fig. 9 Load power vs. source power.

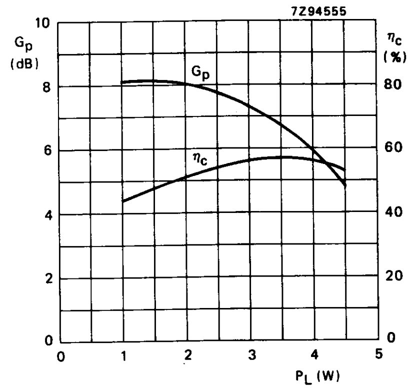


Fig. 10 Power gain and efficiency vs. load power.

Conditions for Figs 9 and 10:

V_{CE} = 9,6 V; f = 900 MHz; T_h = 25 °C; class-B operation; typical values.

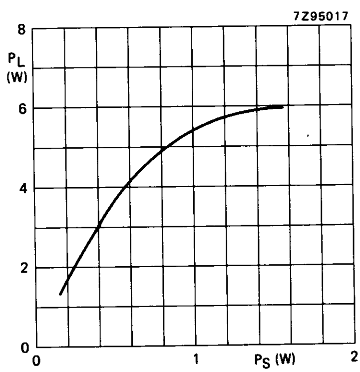


Fig. 11 Load power vs. source power.

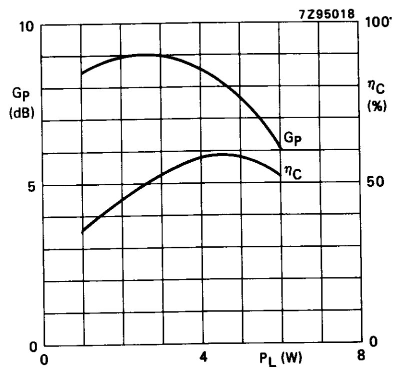


Fig. 12 Power gain and efficiency vs. load power.

Conditions for Figs 11 and 12:

V_{CE} = 12,5 V; f = 900 MHz; T_h = 25 °C; class-B operation; typical values.

RUGGEDNESS

The device is capable of withstanding a full load mismatch (VSWR = 50; all phases) at rated load power up to a supply voltage of 15,5 V and at T_h = 25 °C.

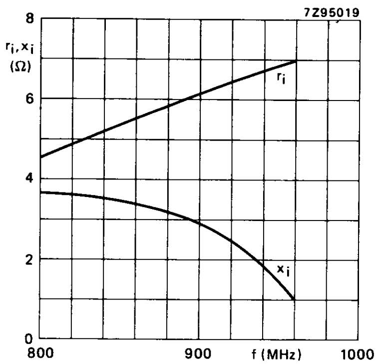


Fig. 13 Input impedance (series components).

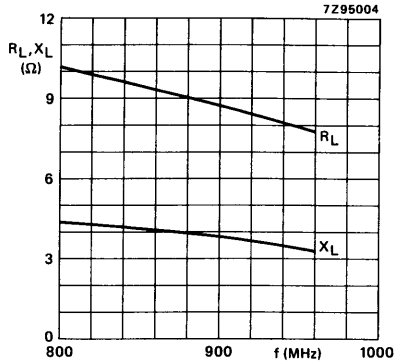


Fig. 14 Load impedance (series components).

Conditions for Figs 13 and 14:
V_{CE} = 12,5 V; P_L = 4 W; f = 800–960 MHz; T_h = 25 °C; class-B operation; typical values.

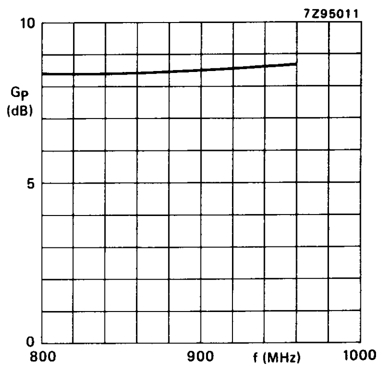


Fig. 15 Power gain vs. frequency.

V_{CE} = 12,5 V; P_L = 4 W; f = 800–960 MHz; T_h = 25 °C; class-B operation; typical values.

U.H.F. POWER TRANSISTOR

N-P-N silicon planar epitaxial transistor primarily intended for use in mobile radio transmitters in the 900 MHz communications band.

Features:

- multi-base structure and emitter-ballasting resistors for an optimum temperature profile
- internal input matching to achieve an optimum wideband capability and high power gain
- gold metallization ensures excellent reliability.

The transistor has a 6-lead flange envelope with a ceramic cap (SOT-171). All leads are isolated from the flange.

QUICK REFERENCE DATA

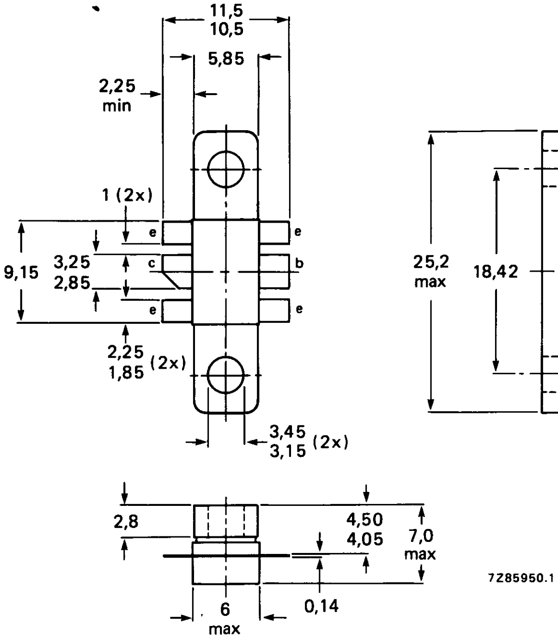
R.F. performance at T_h = 25 °C in a common-emitter class-B test circuit

mode of operation	V_{CE} V	f MHz	P_L W	G_P dB	η_C %
narrow band; c.w.	12,5 9,6	900 900	8 6	> 6,5 typ. 6,0	> 50 typ. 59

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

MECHANICAL DATA Dimensions in mm

Fig. 1 SOT-171.



Torque on screw: min. 0,6 Nm (6 kg.cm)
max. 0,75 Nm (7,5 kg.cm)

Recommended screw: cheese-head 4-40 UNC/2A

Heatsink compound must be applied sparingly and evenly distributed.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-base voltage (open emitter) peak value	V_{CBOM}	max.	36 V
Collector-emitter voltage (open base)	V_{CEO}	max.	16 V
Emitter-base voltage (open collector)	V_{EBO}	max.	3 V
Collector current			
d.c. or average	I_C; $I_{C\,AV}$	max.	1,6 A
(peak value); f > 1 MHz	I_{CM}	max.	4,8 A
Total power dissipation			
at T_{mb} = 67 °C	$P_{tot(dc)}$	max.	18 W
at T_{mb} = 67 °C; f > 1 MHz	$P_{tot(rf)}$	max.	24 W
Storage temperature	T_{stg}		−65 to + 150 °C
Operating junction temperature	T_j	max.	200 °C

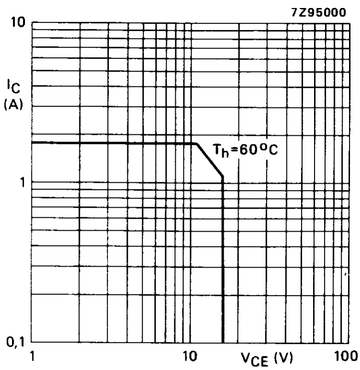


Fig. 2 D.C.-SOAR.
$R_{th\,mb-h}$ = 0,4 K/W

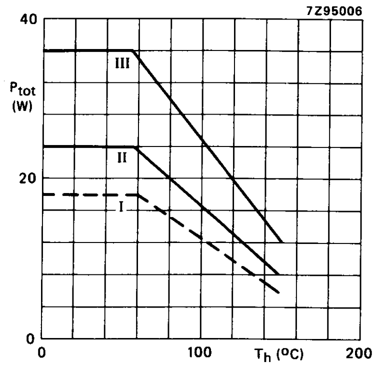


Fig. 3 Power/temperature derating curves.

I Continuous operation
II Continuous operation (f > 1 MHz)
III Short-time operation during mismatch; (f > 1 MHz)

THERMAL RESISTANCE

Dissipation = 12 W; T_{mb} = 112 °C

From junction to mounting base			
(d.c. dissipation)	$R_{th\,j-mb(dc)}$	max.	7,0 K/W
(r.f. dissipation)	$R_{th\,j-mb\,(rf)}$	max.	5,2 K/W
From mounting base to heatsink	$R_{th\,mb-h}$	max.	0,4 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-base breakdown voltage open emitter; I_C = 20 mA	$V_{(BR)CBO}$	>	36 V
Collector-emitter breakdown voltage open base; I_C = 40 mA	$V_{(BR)CEO}$	>	16 V
Emitter-base breakdown voltage open collector; I_E = 2 mA	$V_{(BR)EBO}$	>	3 V
Collector cut-off current V_{BE} = 0; V_{CE} = 16 V	I_{CES}	<	10 mA
Second breakdown energy L = 25 mH; f = 50 Hz; R_{BE} = 10 Ω	E_{SBR}	>	2 mJ
D.C. current gain I_C = 1,2 A; V_{CE} = 10 V	h_{FE}	>	25
Transition frequency at f = 500 MHz* $-I_E$ = 1,2 A; V_{CE} = 12,5 V	f_T	typ.	4 GHz
Collector capacitance at f = 1 MHz $I_E = i_e$ = 0; V_{CB} = 12,5 V	C_c	typ.	15 pF
Feed-back capacitance at f = 1 MHz I_C = 0; V_{CE} = 12,5 V	C_{re}	typ.	9 pF
Collector-flange capacitance	C_{cf}	typ.	2 pF

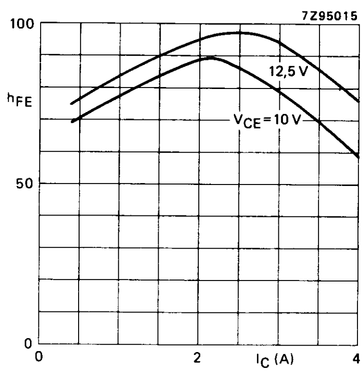


Fig. 4 T_j = 25 °C; typical values.

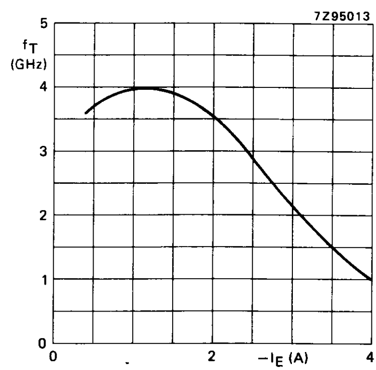


Fig. 5 V_{CB} = 12,5 V; f = 500 MHz; T_j = 25 °C; typical values.

* Measured under pulse conditions: t_p = 50 μs; $\delta < 1\%$.

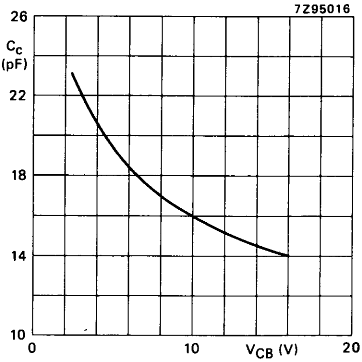


Fig. 6 $I_E = i_e = 0$; f = 1 MHz; typical values.

APPLICATION INFORMATION

R.F. performance in c.w. operation (common-emitter circuit; class-B): f = 900 MHz; T_h = 25 °C.

mode of operation	V_{CE} V	P_L W	P_S W	G_P dB	I_C A	η_C %
narrow band; c.w.	12,5	8	< 1,8 typ. 1,5	> 6,5 typ. 7,3	< 1,28 typ. 1,1	> 50 typ. 58
	9,6	6	typ. 1,5	typ. 6,0	typ. 1,05	typ. 59

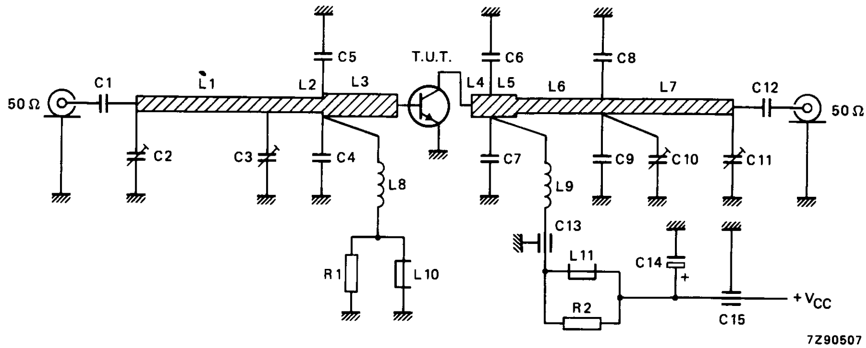


Fig. 7 Class-B test circuit at f = 900 MHz.

List of components:

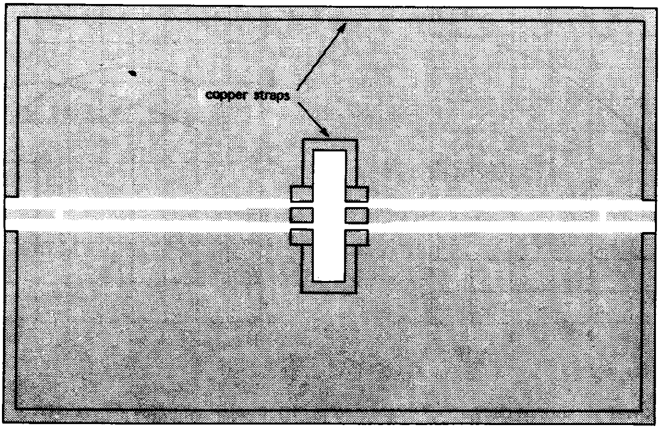
C1 = C12 = 33 pF multilayer ceramic chip capacitor
C2 = C3 = C10 = C11 = 1,4 to 5,5 pF film dielectric trimmer
(cat. no. 2222 809 09001)
C4 = C5 = 4,7 pF multilayer ceramic chip capacitor*
C6 = C7 = 5,6 pF multilayer ceramic chip capacitor*
C8 = C9 = 3,3 pF multilayer ceramic chip capacitor*
C13 = 10 pF ceramic feed-through capacitor
C14 = 6,8 μF (63 V) electrolytic capacitor
C15 = 330 pF ceramic feed-through capacitor

L1 = L7 = 50 Ω stripline (29,0 x 2,4 mm)
L2 = 50 Ω stripline (6,0 mm x 2,4 mm)
L3 = 42,7 Ω stripline (13,1 mm x 3,0 mm)
L4 = 42,7 Ω stripline (4,4 mm x 3,0 mm)
L5 = 42,7 Ω stripline (4,6 mm x 3,0 mm)
L6 = 50 Ω stripline (11,0 x 2,4 mm)
L8 = 60 nH; 4 turns closely wound enamelled Cu-wire (0,4 mm); int. dia. 3 mm; leads 2 x 5 mm
L9 = 45 nH; 4 turns enamelled Cu-wire (1,0 mm); length 6 mm; int. dia 4 mm; leads 2 x 5 mm
L10 = L11 = Ferroxcube wideband h.f. choke, grade 3B (cat. no. 4312 020 36642)

R1 = R2 = 10 Ω ± 10%; 0,25 W, metal film resistor

L1 to L7 are striplines on a double Cu-clad printed circuit board with P.T.F.E. fibre-glass dielectric (ϵ_r = 2,2); thickness 1/32 inch.

* American Technical Ceramics capacitor type 100A or capacitor of same quality.



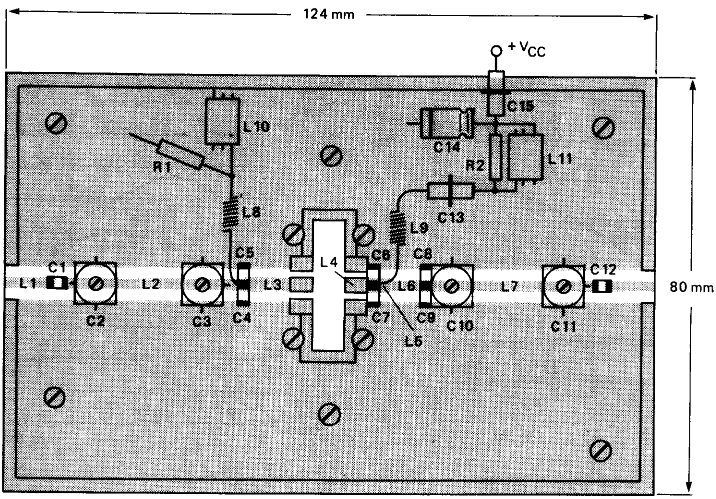


Fig. 8 Printed circuit board and component lay-out for 900 MHz class-B test circuit.

Note

The circuit and the components are on one side of the P.T.F.E. fibre-glass board; the other side is unetched copper serving as ground plane. Earth connections are made by fixing screws and copper straps around the board and under the emitters to provide a direct contact between the copper on the component side and the ground plane.

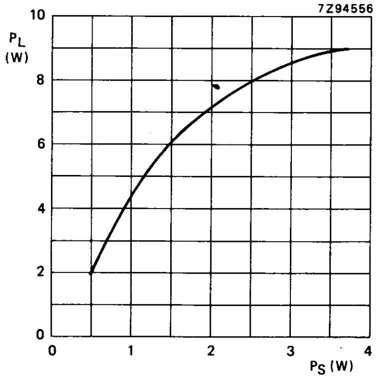


Fig. 9 Load power vs. source power.

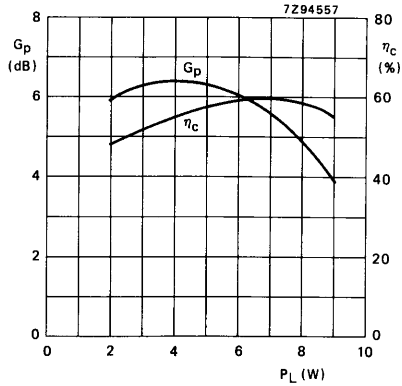


Fig. 10 Power gain and efficiency vs. load power.

Conditions for Figs 9 and 10:

V_{CE} = 9,6 V; f = 900 MHz; T_h = 25 °C; class-B operation; typical values.

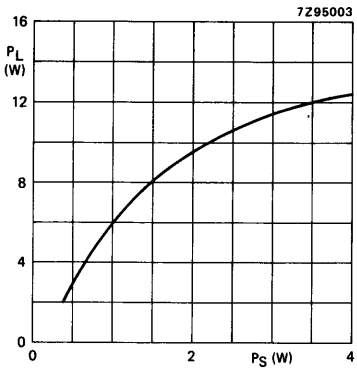


Fig. 11 Load power vs. source power.

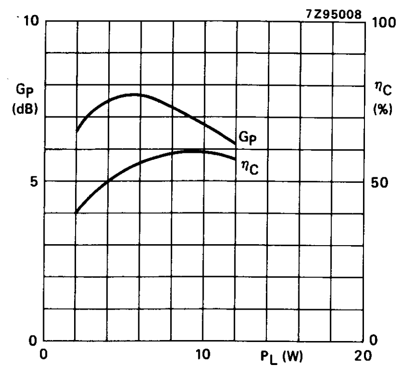


Fig. 12 Power gain and efficiency vs. load power.

Conditions for Figs 11 and 12:

V_{CE} = 12,5 V; f = 900 MHz; T_h = 25 °C; class-B operation; typical values.

RUGGEDNESS

The device is capable of withstanding a full load mismatch (VSWR = 50; all phases) at rated load power up to a supply voltage of 15,5 V and at T_h = 25 °C.

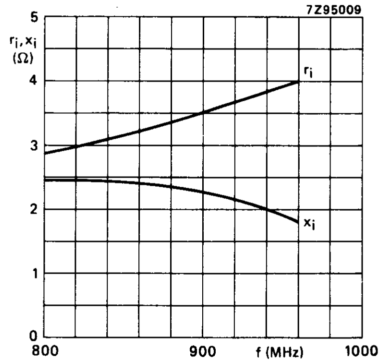


Fig. 13 Input impedance (series components).

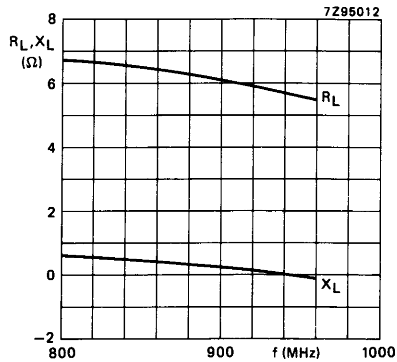


Fig. 14 Load impedance (series components).

Conditions for Figs 13 and 14:

V_{CE} = 12,5 V; P_L = 8 W; f = 800–960 MHz; T_h = 25 °C; class-B operation; typical values.

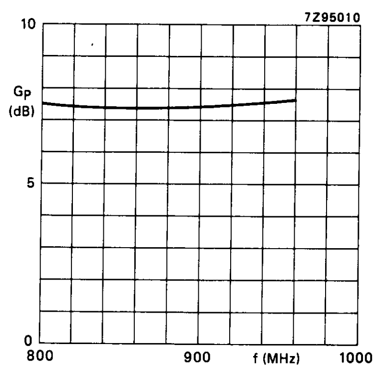


Fig. 15 Power gain vs. frequency.

V_{CE} = 12,5 V; P_L = 8 W; f = 800–960 MHz; T_h = 25 °C; class-B operation; typical values.

U.H.F. POWER TRANSISTOR

N-P-N silicon planar epitaxial transistor primarily intended for common base, class-B operation in mobile radio transmitters for the 900 MHz communication band.

Features:

- emitter-ballasting resistors for an optimum temperature profile
- gold metallization ensures excellent reliability
- internal input matching to achieve an optimum wideband capability and stable operation

The transistor has a 6-lead flange envelope with a ceramic cap (SOT-171). All leads are isolated from the flange.

QUICK REFERENCE DATA

R.F. performance up to T_h = 25 °C in a common-base class-B circuit

mode of operation	V_{CB} V	f MHz	P_L W	G_p dB	η_C %
narrow band; c.w.	12,5	900	15	> 6	> 50

MECHANICAL DATA

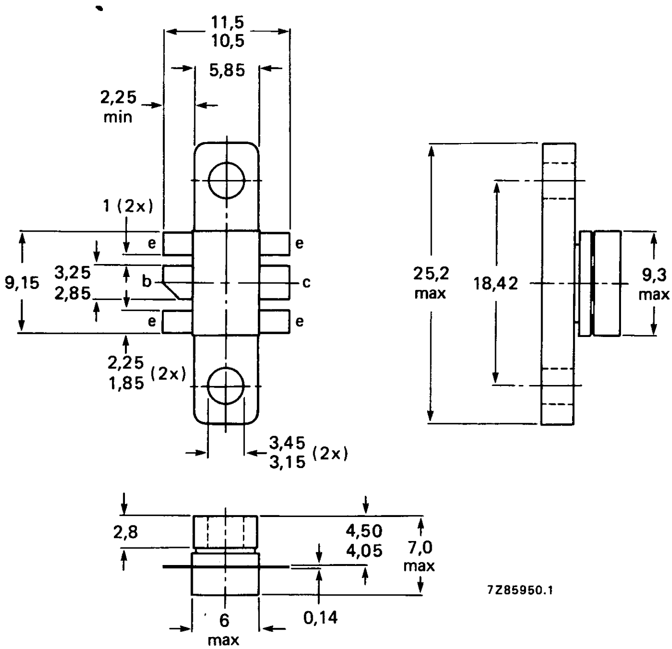
SOT-171 (see Fig. 1).

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-171.



Torque on screw:	min. 0,6 Nm (6 kg.cm) max. 0,75 Nm (7,5 kg.cm)
Recommended screw:	cheese-head 4-40 UNC/2A

Heatsink compound must be applied sparingly and evenly distributed.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-base voltage (open emitter)	V_{CBO}	max.	36 V
Collector-emitter voltage (open base)	V_{CEO}	max.	16 V
Emitter-base voltage (open collector)	V_{EBO}	max.	3,5 V
Collector current			
d.c. or average	I_C	max.	3 A
peak value; $f > 1$ MHz	I_{CM}	max.	9 A
Total power dissipation			
at $T_{mb} = 25\ ^oC$; $f > 1$ MHz	P_{tot}	max.	45 W
Storage temperature	T_{stg}		−65 to +150 °C
Operating junction temperature	T_j	max.	200 °C

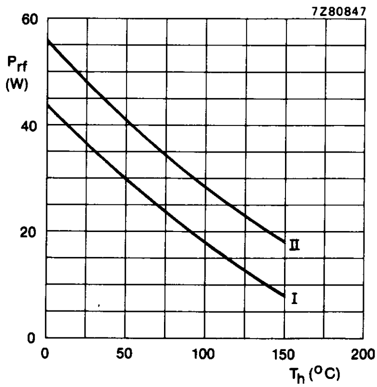


Fig. 2 Power/temperature derating curves;
I Continuous operation ($f > 1$ MHz)
II Short-time operation during mismatch;
($f > 1$ MHz)

THERMAL RESISTANCE

From junction to mounting base (r.f. operation)	$R_{th\ j\text{-}mb}$	max.	4 K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	max.	0,4 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-base breakdown voltage open emitter; I_C = 25 mA	$V_{(BR)CBO}$	min.	36 V
Collector-emitter breakdown voltage open base; I_C = 50 mA	$V_{(BR)CEO}$	min.	16 V
Emitter-base breakdown voltage open collector; I_E = 5 mA	$V_{(BR)EBO}$	min.	3,5 V
Collector cut-off current V_{BE} = 0; V_{CE} = 16 V	I_{CES}	max.	10 mA
Second breakdown energy L = 25 mH; f = 50 Hz; R_{BE} = 10 Ω	E_{SBR}	min.	4,5 mJ
D.C. current gain V_{CE} = 10 V; I_C = 2 A	h_{FE}	min. typ.	15 65
Collector capacitance at f = 1 MHz I_E = i_e = 0; V_{CB} = 12,5 V	C_c	typ.	33 pF
Feedback capacitance at f = 1 MHz I_E = 0; V_{CB} = 12,5 V	C_{rb}	typ.	9 pF
→ Collector-flange capacitance	C_{cf}	typ.	2 pF

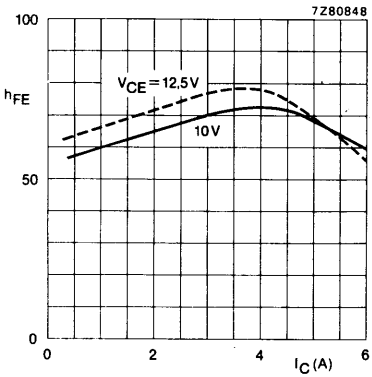


Fig. 3 D.C. current gain versus collector current; T_j = 25 °C. Typical values.

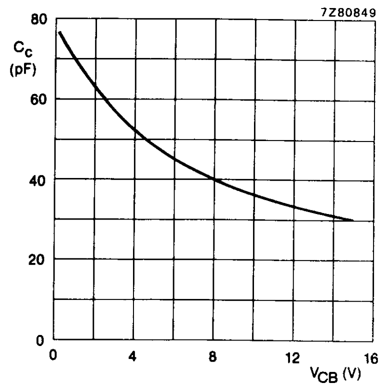


Fig. 4 Output capacitance versus V_{CB}; I_E = i_e = 0; f = 1 MHz. Typical values.

APPLICATION INFORMATION

R.F. performance in c.w. operation (common-base circuit; class-B)
f = 900 MHz; T_h = 25 °C

mode of operation	V_{CB} V	P_L W	G_p dB	η_C %
narrow band; c.w.	12,5	15	> 6,0 typ. 7,0	> 50 typ. 61

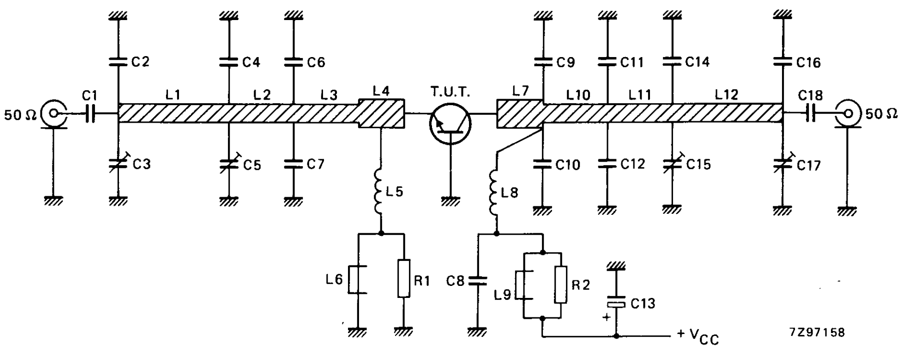


Fig. 5 Class-B test circuit at f = 900 MHz.

List of components:

$C_1 = C_{18}$ = 330 pF multilayer ceramic chip capacitor *
$C_2 = C_4 = C_{16}$ = 5,6 pF multilayer ceramic chip capacitor *
$C_3 = C_5 = C_{15} = C_{17}$ = 1,4 to 5,5 pF film dielectric trimmer
(cat. no. 2222 809 09001)
$C_6 = C_7$ = 4,3 pF multilayer ceramic chip capacitor *
C_8 = 330 pF multilayer ceramic chip capacitor
$C_9 = C_{10}$ = 5,6 pF multilayer ceramic chip capacitors **
$C_{11} = C_{12}$ = 6,2 pF multilayer ceramic chip capacitor *

C_{13} = 6,8 μF (63 V) electrolytic capacitor
C_{14} = 2,2 pF multilayer ceramic chip capacitor *
L_1 = L_{12} = 50 Ω stripline (24 mm x 2,4 mm)
L_2 = L_{11} = 50 Ω stripline (10 mm x 2,4 mm)
L_3 = 50 Ω stripline (8 mm x 2,4 mm)
L_4 = L_7 = 41 Ω (3 mm x 3,2 mm)
L_5 = L_8 = 4 turns Cu-wire (1,0 mm); int. dia. 4 mm; length 5 mm;
leads 2 x 7 mm
L_6 = L_9 = Ferroxcube wideband h.f. choke; grade 3B (cat. no 4312 020 36642)
L_{10} = 50 Ω stripline (7 mm x 2,4 mm)

R_1 = R_2 = 10 Ω ± 10 %; 0,25 W, metal film resistor
The striplines are on a double Cu-clad printed circuit board with P.T.F.E. fibre-glass dielectric (ϵ_r = 2,2); thickness 1/32 inch.

* American Technical Ceramics capacitor type 100B or capacitor of the same quality.
** Idem type 100A.

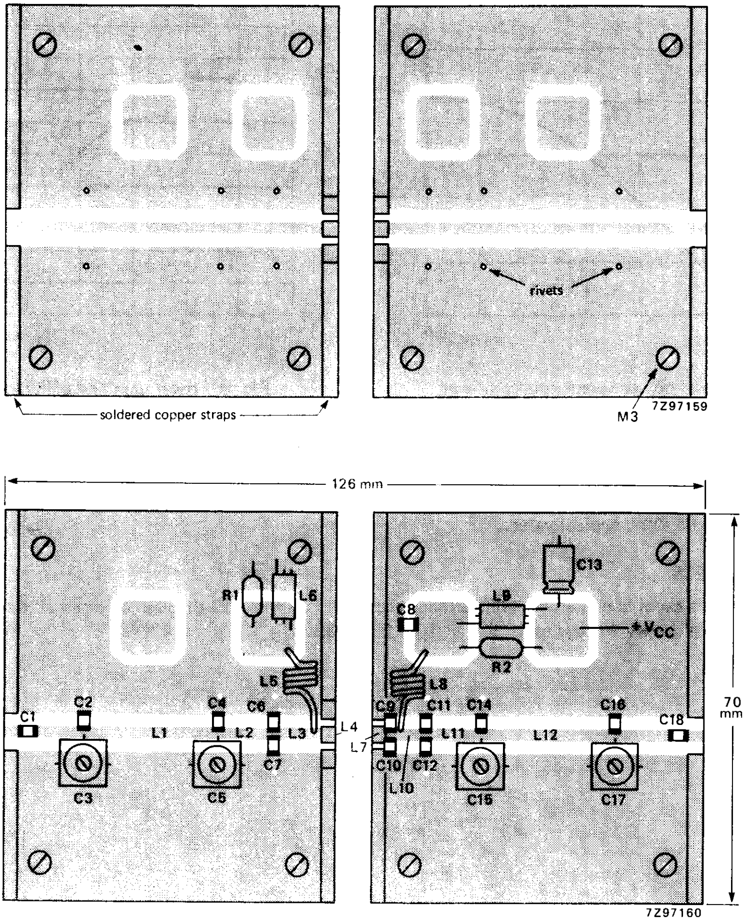


Fig. 6 Printed circuit board and component lay-out for 900 MHz class-B test circuit.

The circuit and components are on one side of the P.T.F.E. fibre-glass board; the other side is unetched copper serving as a ground plane.
Earth connections are made by fixing screws, hollow rivets and copper straps around the board and under the bases to provide a direct contact between the copper of the component side and the ground plane.

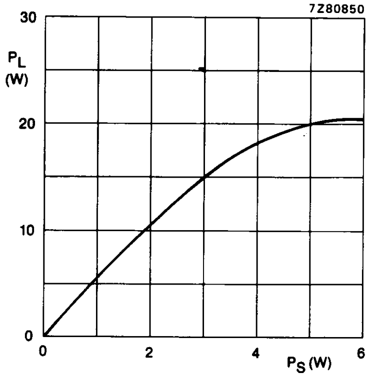


Fig. 7 Load power versus source power.

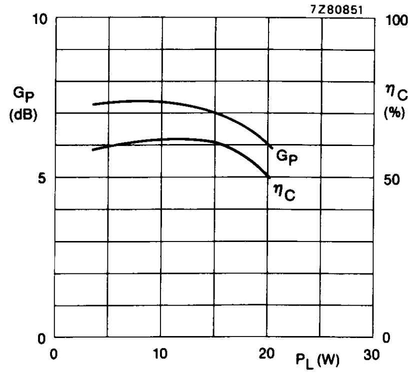


Fig. 8 Power gain and efficiency versus load power.

Conditions for Figs 7 and 8:

V_{CB} = 12,5 V; f = 900 MHz; T_h = 25 ^oC; class-B operation;
$R_{th\ mb\text{-}h}$ = 0,4 K/W; typical values.

RUGGEDNESS

The BLV94 is capable of withstanding a load mismatch (VSWR = 50 through all phases) at rated load power up to a supply voltage of 15,5 V at T_h = 25 ^oC and $R_{th\ mb\text{-}h}$ = 0,4 K/W.

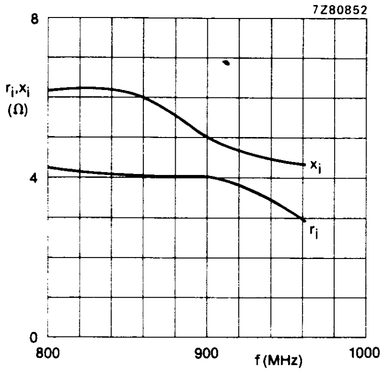


Fig. 9 Input impedance (series components).

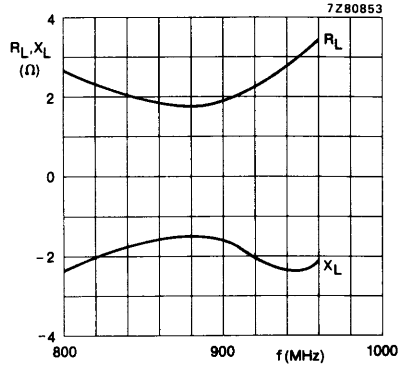


Fig. 10 Load impedance (series components).

Conditions for Figs 9, 10 and 11:

Typical values; V_{CE} = 12,5 V; P_L = 15 W; f = 800 to 960 MHz;
$R_{th\ mb\text{-}h}$ = 0,4 K/W; T_h = 25 °C.

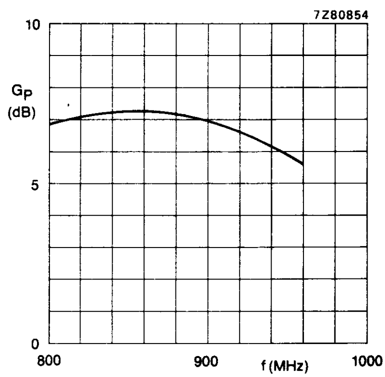


Fig. 11 Power gain versus frequency.

U.H.F. POWER TRANSISTOR

N-P-N silicon planar epitaxial transistor in SOT-171 envelope intended for use in class-B operated base station transmitters in the 900 MHz communications band.

Features

- internal matching to achieve an optimum wideband capability and stable operation.
- emitter-ballasting resistors for an optimum temperature profile.
- gold metallization ensures excellent reliability.

The transistor has a 6-lead flange envelope with a ceramic cap. All leads are isolated from the flange.

QUICK REFERENCE DATA

R.F. performance up to T_h = 25 °C in common-base class-B circuit.

mode of operation	V_{CB} V	f MHz	P_L W	G_p dB	η_C %
narrow band; c.w.	24	900	30	> 7,0	> 55

MECHANICAL DATA

Dimensions in mm

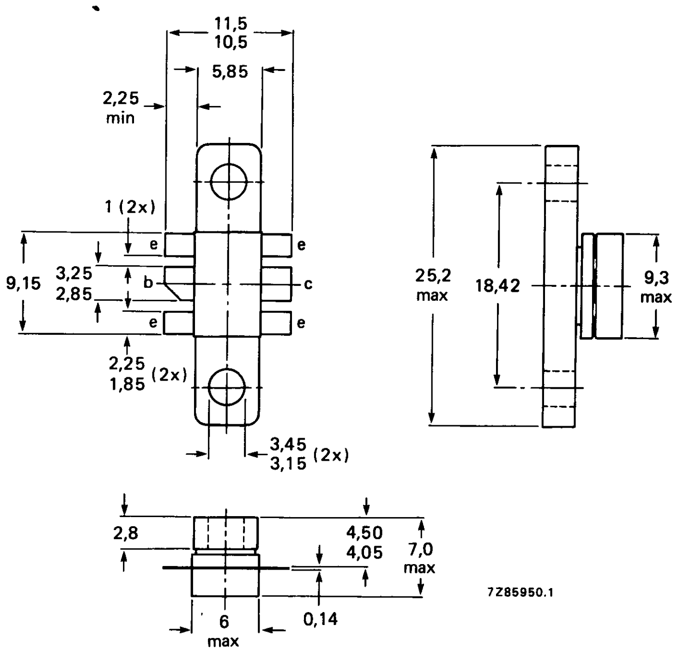
Fig. 1 SOT-171.

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-171.



Torque on screw: min. 0,6 Nm (6 kg.cm)
max. 0,75 Nm (7,5 kg.cm)

Recommended screw: cheese-head 4-40 UNC/2A

Heatsink compound must be applied sparingly and evenly distributed.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-base voltage (open emitter)	V_{CBO}	max.	50 V
Collector-emitter voltage (open base)	V_{CEO}	max.	27 V
Emitter-base voltage (open collector)	V_{EBO}	max.	3,5 V
Collector current			
d.c. or average	I_C	max.	3 A
peak value; f > 1 MHz	I_{CM}	max.	9 A
Total power dissipation			
at T_{mb} = 25 °C; f > 1 MHz	P_{tot}	max.	60 W
Storage temperature	T_{stg}	−65 to + 150 °C	
Operating junction temperature	T_j	max.	200 °C

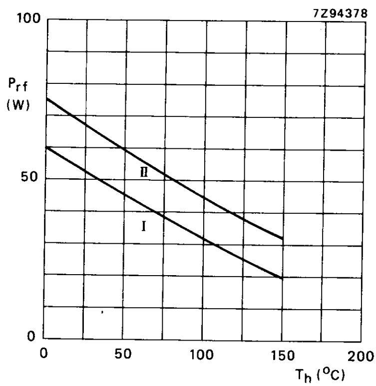


Fig. 2 Power/temperature derating curves.
I Continuous operation (f > 1 MHz)
II Short-time operating during mismatch (f > 1 MHz)

THERMAL RESISTANCE

Dissipation = 60 W; T_{amb} = 25 °C.

From junction to mounting base (r.f. operation)	$R_{th\ j\text{-}mb}$	max.	2,9 K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	max.	0,4 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

Collector-base breakdown voltage open emitter; I_C = 50 mA	$V_{(BR)CBO}$	min.	50 V
Collector-emitter breakdown voltage open base; I_C = 100 mA	$V_{(BR)CEO}$	min.	27 V
Emitter-base breakdown voltage open collector; I_E = 10 mA	$V_{(BR)EBO}$	min.	3,5 V
Collector-emitter leakage current V_{BE} = 0; V_{CE} = 27 V	I_{CES}	max.	10 mA
Second breakdown energy L = 25 mH; f = 50 Hz; R_{BE} = 10 Ω	E_{SBR}	min.	4 mJ
D.C. current gain V_{CE} = 20 V; I_C = 2 A	h_{FE}	min.	15
Collector capacitance at f = 1 MHz $I_E = i_e$ = 0; V_{CB} = 24 V	C_c	typ.	44 pF
Feedback capacitance at f = 1 MHz I_E = 0; V_{CB} = 24 V	C_{rb}	typ.	14 pF
→ Collector-flange capacitance	C_{cf}	typ.	2 pF

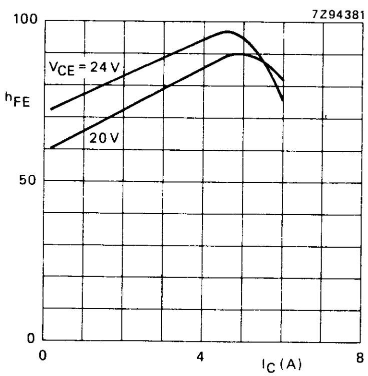


Fig. 3 D.C. current gain versus collector current; T_j = 25 °C.

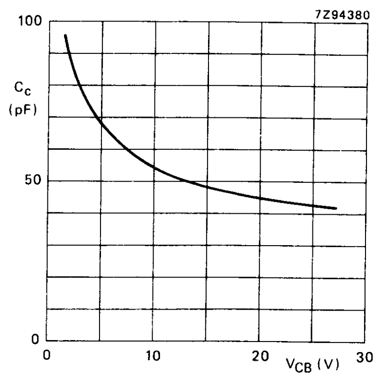


Fig. 4 Collector capacitance versus V_{CB}; $I_E = i_e$ = 0; f = 1 MHz.

APPLICATION INFORMATION

R.F. performance at T_h = 25 °C in common-base class-B circuit.

mode of operation	V_{CB} V	f MHz	P_L W	G_P dB	η_C %
narrow band; c.w.	24	900	30	> 7,0 typ. 8,0	> 55 typ. 63

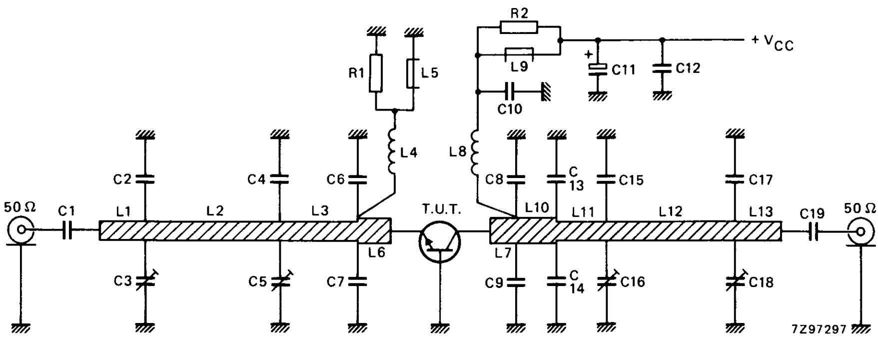


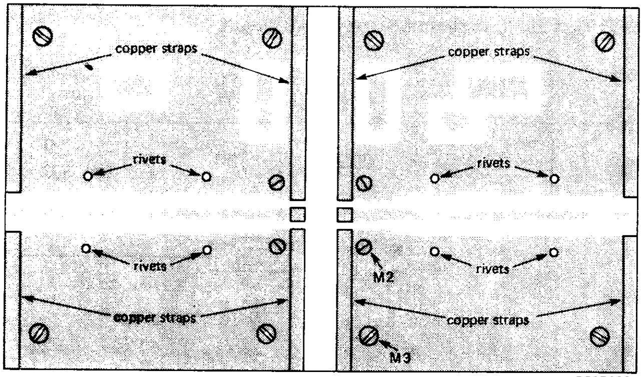
Fig. 5 Class-B test circuit at f = 900 MHz.

List of components:

C1 = C10 = C19 = 330 pF multilayer ceramic chip capacitor
C2 = C4 = C13 = C14 = C15 = C17 = 6,2 pF multilayer ceramic chip capacitor*
C3 = C5 = C16 = C18 = 1,4 to 5,5 pF dielectric trimmer (cat. no. 2222 809 09001)
C6 = 6,2 pF multilayer ceramic chip capacitor**
C7 = C8 = C9 = 6,8 pF multilayer ceramic chip capacitor*
C11 = 2,2 μF (63 V) electrolytic capacitor
C12 = 3 x 100 nF multilayer ceramic chip capacitor in parallel
L1 = L13 = 50 Ω stripline (9,0 mm x 2,4 mm)
L2 = 50 Ω stripline (24,0 mm x 2,4 mm)
L3 = 50 Ω stripline (13,0 mm x 2,4 mm)
L4 = 250 nH; 9 turns closely wound enamelled Cu-wire (1,0 mm) int. dia. 4 mm; leads 2 x 7 mm
L5 = L9 = Ferroxcube wide-band h.f. choke, grade 3B (cat. no. 4312 020 26642)
L6 = 43 Ω stripline (5,5 mm x 3,0 mm)
L7 = 43 Ω stripline (3,0 mm x 3,0 mm)
L8 = 65 nH; 5 turns closely wound enamelled Cu-wire (1,0 mm) int. dia. 4 mm; leads 2 x 7 mm
L10 = 43 Ω stripline (7,5 mm x 3,0 mm)
L11 = 50 Ω stripline (8,0 mm x 2,4 mm)
L12 = 50 Ω stripline (24,0 mm x 2,4 mm)
R1 = 1 Ω ± 5% (0,25 W) metal film resistor
R2 = 10 Ω ± 5% (0,25 W) metal film resistor

The striplines are on a double Cu-clad printed circuit board with PTFE fibre-glass dielectric (ϵ_r = 2,2); thickness 1/32 inch.

* Americal Technical Ceramics capacitor type 100B or capacitor of the same quality.
** Idem type 100A.



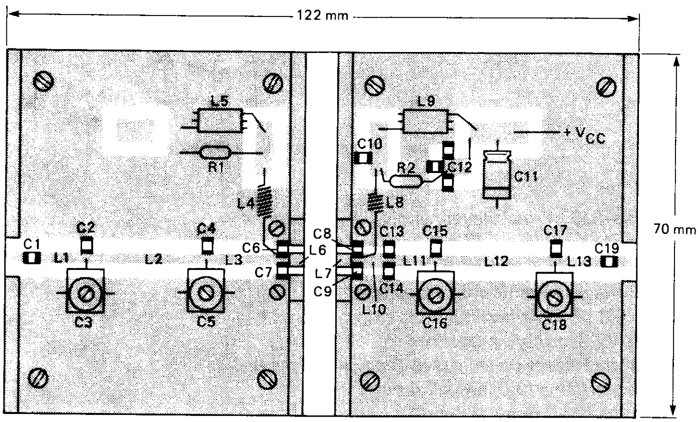


Fig. 6 Printed circuit board and component layout for 900 MHz class-B test circuit.

The circuit and the components are on one side of the PTFE fibre-glass board; the other side is unetched copper serving as a ground plane. Earth connections are made by fixing screws, hollow rivets and copper straps around the board and under the bases to provide a direct contact between the copper on the component side and the ground plane.

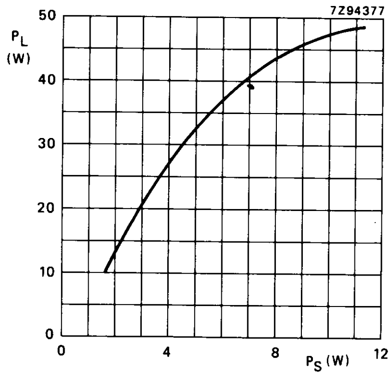


Fig. 7 Load power versus source power.

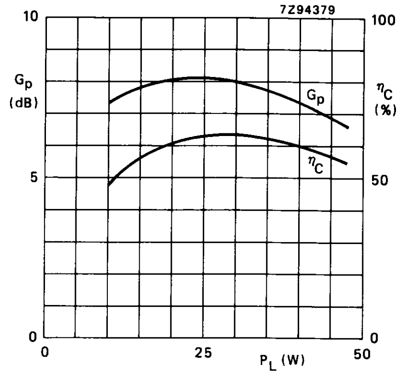


Fig. 8 Power gain and efficiency versus load power.

Conditions for Figs 7 and 8:

Typical values; V_{CB} = 24 V; f = 900 MHz; T_h = 25 °C; class-B operation; $R_{th\ mb\text{-}h}$ = 0,4 K/W.

RUGGEDNESS

The BLV97 is capable of withstanding a full load mismatch (VSWR = 50 through all phases) at rated load power and supply voltage; when T_h = 25 °C and $R_{th\ mb\text{-}h}$ = 0,4 K/W.

INPUT AND LOAD IMPEDANCES

$\overline{Z}_i$ = 1,6 + j 4,4 Ω and $\overline{Z}_L$ = 1,20 + j 3,0 Ω (series components).
Conditions: V_{CB} = 24 V; P_L = 30 W; f = 900 MHz, T_h = 25 °C; class-B operation; $R_{th\ mb\text{-}h}$ = 0,4 K/W; typical values.

U.H.F. POWER TRANSISTOR

N-P-N silicon planar epitaxial transistor in SOT-171 envelope intended for use in class-B operated base station transmitters in the 900 MHz communications band.

Features

- internal matching to achieve an optimum wideband capability and stable operation.
- emitter ballasting resistors for an optimum temperature profile.
- gold metallization ensures excellent reliability.

The transistor has a 6-lead flange envelope with a ceramic cap. All leads are isolated from the flange.

QUICK REFERENCE DATA

R.F. performance up to T_h = 25 °C in common-base class-B circuit.

mode of operation	V_{CB} V	f MHz	P_L W	G_P dB	η_C %
narrow band; c.w.	24	900	14	> 8,5	> 55

MECHANICAL DATA

Dimensions in mm

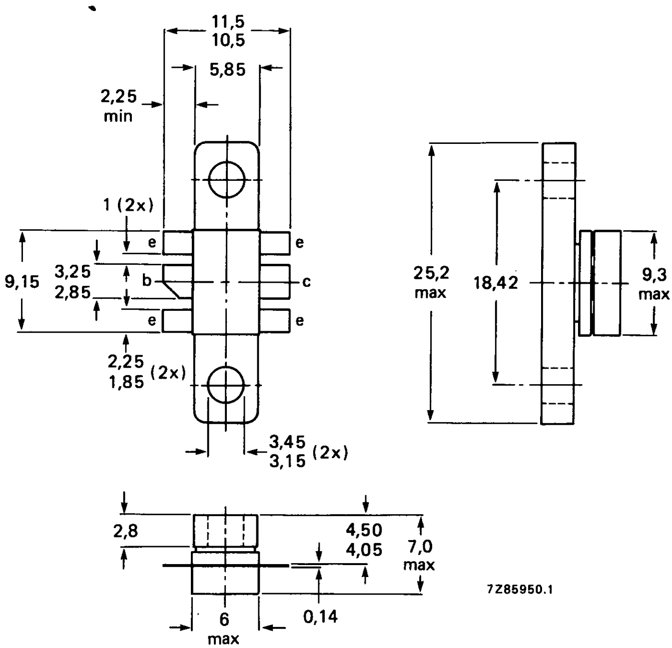
Fig. 1 SOT-171.

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-171.



Torque on screw: min. 0,6 Nm (6 kg.cm)
max. 0,75 Nm (7,5 kg.cm)

Recommended screw: cheese-head 4-40 UNC/2A

Heatsink compound must be applied sparingly and evenly distributed.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-base voltage (open emitter)	V_{CBO}	max.	50 V
Collector-emitter voltage (open base)	V_{CEO}	max.	27 V
Emitter-base voltage (open collector)	V_{EBO}	max.	3,5 V
Collector current			
d.c. or average	I_C	max.	1,5 A
peak value; f > 1 MHz	I_{CM}	max.	4,5 A
Total power dissipation			
at T_{mb} = 25 °C; f > 1 MHz	P_{tot}	max.	40 W
Storage temperature	T_{stg}		−65 to + 150 °C
Operating junction temperature	T_j	max.	200 °C

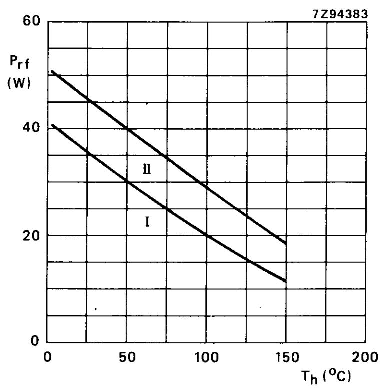


Fig. 2 Power/temperature derating curves.
I Continuous operation (f > 1 MHz)
II Short-time operation during mismatch (f > 1 MHz)

THERMAL RESISTANCE

Dissipation = 40 W; T_{amb} = 25 °C

From junction to mounting base (r.f. operation)	$R_{th\ j\text{-}mb}$	max.	4,4 K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	max.	0,4 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-base breakdown voltage open emitter; I_C = 25 mA	$V_{(BR)CBO}$	min.	50 V
Collector-emitter breakdown voltage open base; I_C = 50 mA	$V_{(BR)CEO}$	min.	27 V
Emitter-base breakdown voltage open collector; I_E = 5 mA	$V_{(BR)EBO}$	min.	3,5 V
Collector-emitter leakage current V_{BE} = 0; V_{CE} = 27 V	I_{CES}	max.	5 mA
Second breakdown energy L = 25 mH; f = 50 Hz; R_{BE} = 10 Ω	E_{SBR}	min.	2 mJ
D.C. current gain V_{CE} = 20 V; I_C = 1 A	h_{FE}	min.	15
Collector capacitance at f = 1 MHz $I_E = i_e$ = 0; V_{CB} = 24 V	C_c	typ.	23 pF
Feedback capacitance at f = 1 MHz I_E = 0; V_{CB} = 24 V	C_{rb}	typ.	7 pF
→ Collector-flange capacitance	C_{cf}	typ.	2 pF

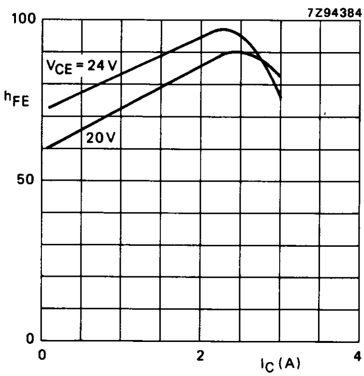


Fig. 3 D.C. current gain versus collector current; T_j = 25 °C.

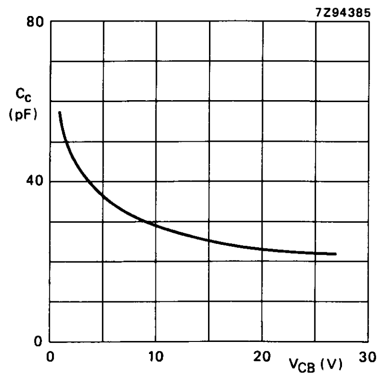


Fig. 4 Output capacitance versus V_{CB}; $I_E = i_e$ = 0; f = 1 MHz.

APPLICATION INFORMATION

R.F. performance at T_h = 25 °C in common-base class-B circuit.

mode of operation	V_{CB} V	f MHz	P_L W	G_p dB	η_C %
narrow band; c.w.	24	900	14	> 8,5 typ. 10,0	> 55 typ. 65

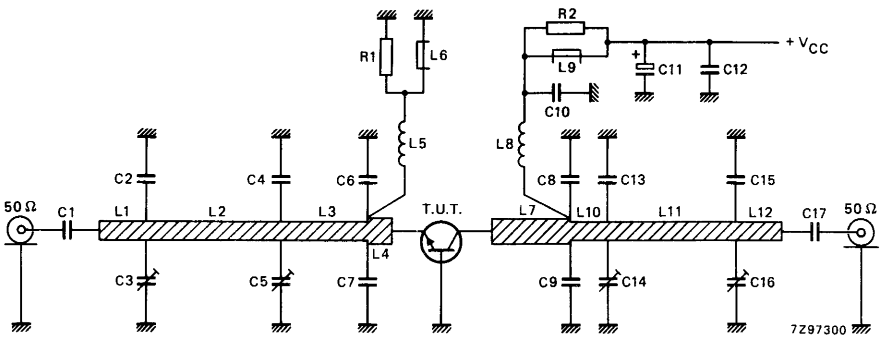


Fig. 5 Class-B test circuit at f = 900 MHz.

List of components:

C1 = C10 = C17 = 330 pF multilayer ceramic chip capacitor
C2 = C13 = 3,3 pF multilayer ceramic chip capacitor*
C3 = C5 = C14 = C16 = 1,4 to 5,5 pF film dielectric trimmer (cat. no. 2222 809 09001)
C4 = C8 = C9 = C15 = 6,2 pF multilayer ceramic chip capacitor*
C6 = C7 = 6,2 pF multilayer ceramic chip capacitor**
C11 = 2,2 μF (63 V) electrolytic capacitor
C12 = 3 x 100 nF multilayer ceramic chip capacitors in parallel
L1 = L12 = 50 Ω stripline (9,0 mm x 2,4 mm)
L2 = L11 = 50 Ω stripline (24,0 mm x 2,4 mm)
L3 = 50 Ω stripline (16,0 mm x 2,4 mm)
L4 = 43 Ω stripline (3,0 mm x 3,0 mm)
L5 = 88 nH; 9 turns closely wound enamelled Cu-wire (0,8 mm); int. dia. 3 mm length 12 mm; leads 2 x 5 mm
L6 = L9 = Ferroxcube wide-band h.f. choke, grade 3B (cat. no. 4312 020 36642)
L7 = 43 Ω stripline (14,5 mm x 3,0 mm)
L8 = 53 nH; 4 turns enamelled Cu-wire (1,0 mm); int. dia. 4 mm; length 5 mm; leads 2 x 5 mm
L10 = 50 Ω stripline (4,5 mm x 2,4 mm)

R1 = 1 Ω ± 5% (0,25 W) metal film resistor
R2 = 10 Ω ± 5% (0,25 W) metal film resistor

The striplines are on a double Cu-clad printed circuit board with PTFE fibre-glass dielectric (ϵ_r = 2,2); thickness 1/32 inch.

* Americal Technical Ceramics capacitor type 100B or capacitor of the same quality.
** Idem type 100A.

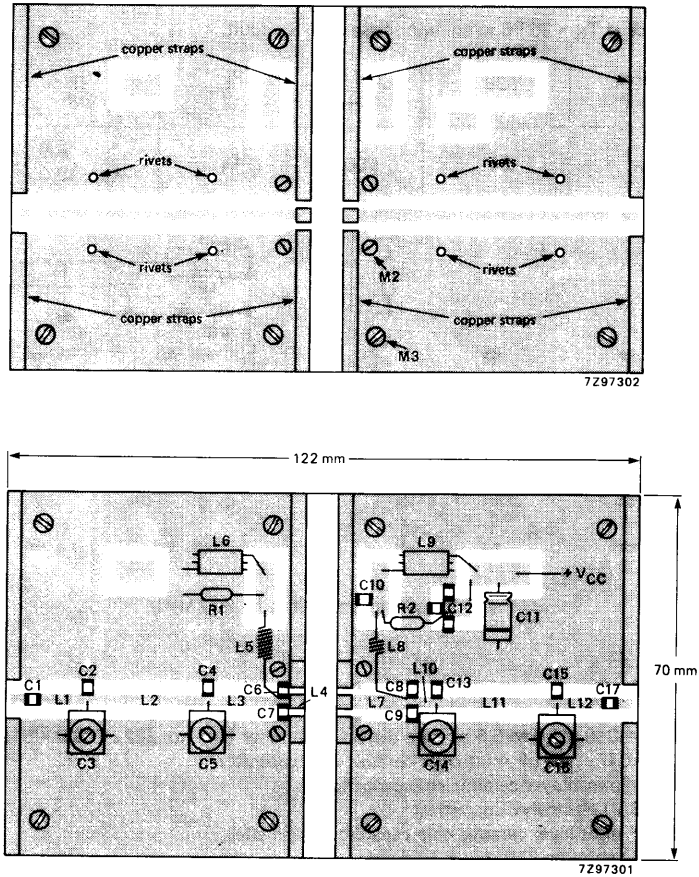


Fig. 6 Printed circuit board and component layout for 900 MHz class-B test circuit.

The circuit and the components are on one side of the PTFE fibre-glass board; the other side is unetched copper serving as a ground plane. Earth connections are made by fixing screws, hollow rivets and copper straps around the board and under the bases to provide a direct contact between the copper on the component side and the ground plane.

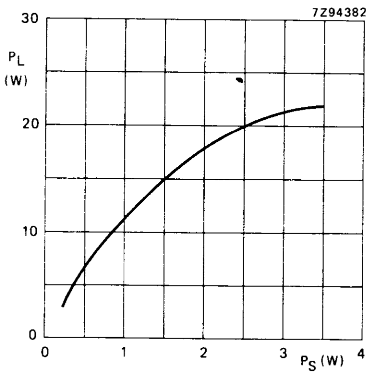


Fig. 7 Load power versus source power.

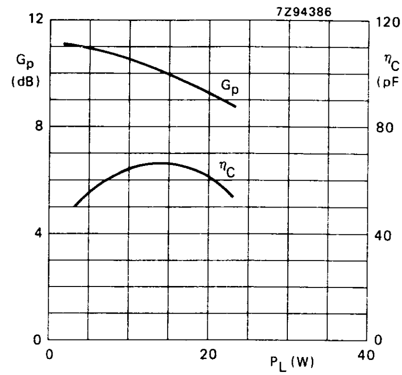


Fig. 8 Power gain and efficiency versus load power.

Conditions for Figs 7 and 8:

Typical values; V_{CB} = 24 V; f = 900 MHz; T_h = 25 °C; class-B operation; $R_{th\ mb\text{-}h}$ = 0,4 K/W.

RUGGEDNESS

The BLV98 is capable of withstanding a full load mismatch (VSWR = 50 through all phases) at rated load power and supply voltage; when T_h = 25 °C and $R_{th\ mb\text{-}h}$ = 0,4 K/W.

INPUT AND LOAD IMPEDANCES

$\overline{Z}_i$ = 5,1 + j 4,5 Ω and $\overline{Z}_L$ = 2,2 + j 3,0 Ω (series components).
Conditions: V_{CB} = 24 V; P_L = 14 W; f = 900 MHz, T_h = 25 °C; class-B operation; $R_{th\ mb\text{-}h}$ = 0,4 K/W; typical values.

U.H.F. POWER TRANSISTOR

N-P-N silicon planar epitaxial transistor primarily intended for use as a driver-stage in base stations in the 900 MHz communications band.

Features:

- emitter-ballasting resistors for an optimum temperature profile
- gold metallization ensures excellent reliability

The transistor has a 4-lead stud envelope with a ceramic cap (SOT-172). All leads are isolated from the stud.

QUICK REFERENCE DATA

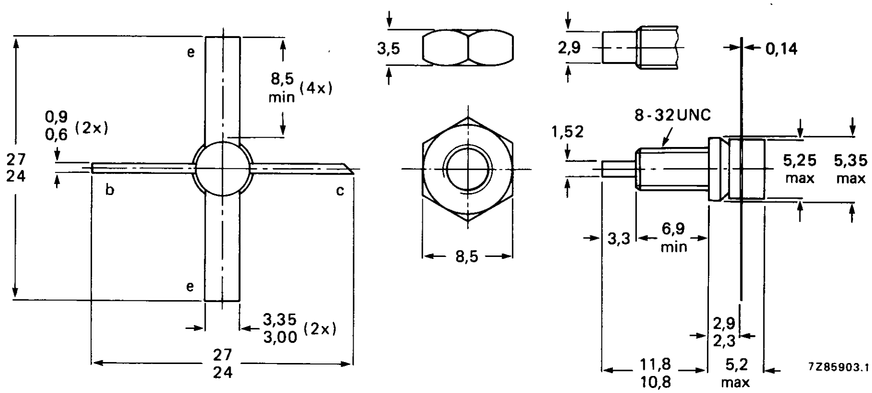
R.F. performance at T_h = 25 °C in a common-emitter class-B circuit

mode of operation	V_{CE} V	f MHz	P_L W	G_p dB	η_C %
narrow band; c.w.	24	900	2	> 8,0	> 55

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-172.



Torque on nut: min. 0,75 Nm (7,5 kg.cm)
max. 0,85 Nm (8,5 kg.cm)
When locking is required an adhesive is preferred instead of a lock washer.

Diameter of clearance hole in heatsink: max. 4,2 mm.
Mounting hole to have no burrs at either end.
Deburring must leave surface flat; donot chamfer or countersink either end of hole.

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-base voltage (open emitter)	V_{CBO}	max.	50 V
Collector-emitter voltage (open base)	V_{CEO}	max.	27 V
Emitter-base voltage (open collector)	V_{EBO}	max.	3,5 V
Collector current; d.c.	I_C	max.	0,2 A
Collector current (peak value) f > 1 MHz	I_{CM}	max.	0,6 A
Total power dissipation at T_{mb} = 50 °C; f > 1 MHz	P_{tot}	max.	6 W
Storage temperature	T_{stg}	−65 to + 150 °C	
Operating junction temperature	T_j	max.	200 °C

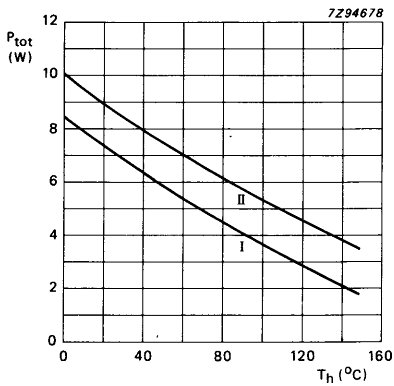


Fig. 2 Power/temperature derating curves.

I continuous r.f. operation (f > 1 MHz)

II short-time r.f. operation during mismatch (f > 1 MHz)

THERMAL RESISTANCE

P = 4,5 W; T_{mb} = 25 °C

From junction to mounting base (f > 1 MHz)	$R_{th\ j\text{-}mb}$	max.	20 K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	max.	0,8 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-base breakdown voltage open emitter; I_C = 5 mA	$V_{(BR)CBO}$	min.	50 V
Collector-emitter breakdown voltage open base; I_C = 10 mA	$V_{(BR)CEO}$	min.	27 V
Emitter-base breakdown voltage open collector; I_E = 0,5 mA	$V_{(BR)EBO}$	min.	3,5 V
Collector-emitter leakage current V_{BE} = 0; V_{CE} = 27 V	I_{CES}	max.	2 mA
Second breakdown energy at f = 50 Hz L = 25 mH; R_{BE} = 10 Ω	E_{SBR}	min.	0,5 mJ
D.C. current gain I_C = 150 mA; V_{CE} = 20 V	h_{FE}	min.	25
Collector capacitance at f = 1 MHz $I_E = i_e$ = 0; V_{CB} = 24 V	C_c	typ.	3 pF
Feedback capacitance at f = 1 MHz I_C = 0; V_{CE} = 24 V	C_{re}	typ.	1,3 pF
Collector-stud capacitance	C_{cs}	typ.	0,5 pF

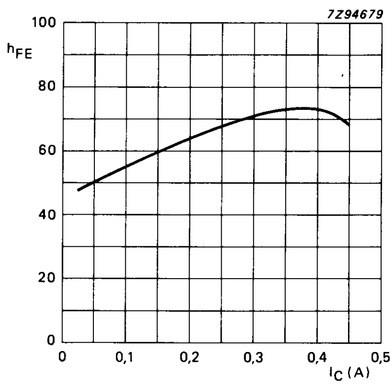


Fig. 3 V_{CE} = 20 V; T_j = 25 °C; typical values.

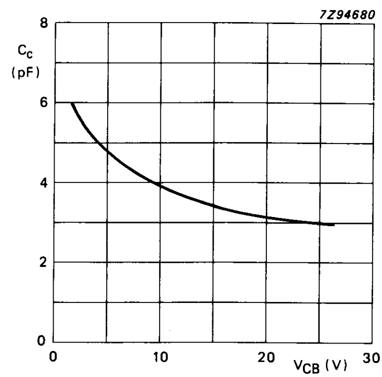


Fig. 4 $I_E = i_e$ = 0; f = 1 MHz; typical values.

APPLICATION INFORMATION

R.F. performance in c.w. operation (common-emitter circuit; class-B)
f = 900 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0,8 K/W

mode of operation	V_{CE} V	f MHz	P_L W	G_P dB	η_C %
narrow band; c.w.	24	900	2	min. 8,0 typ. 9,3	min. 55 typ. 63

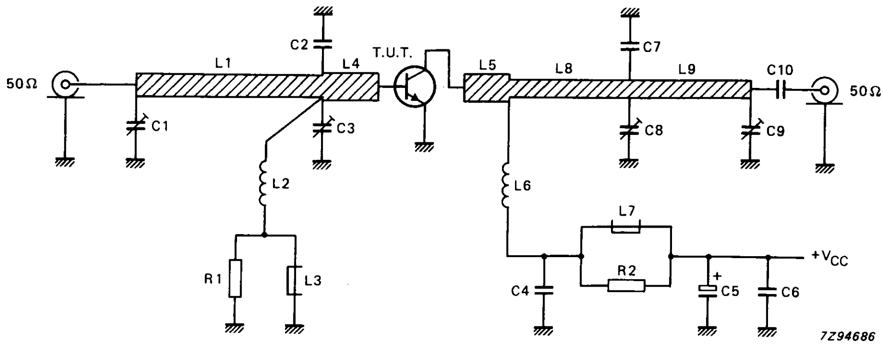


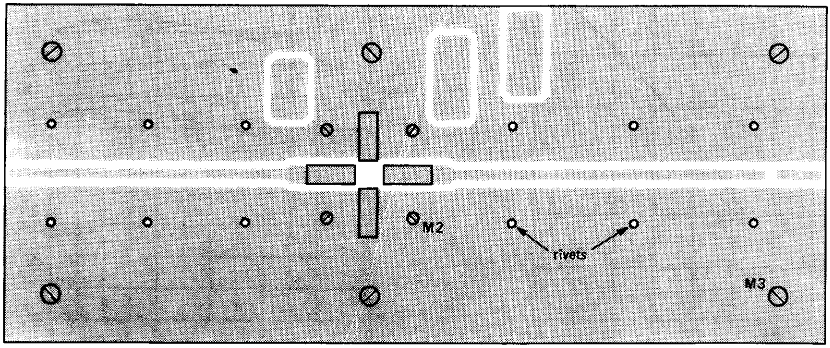
Fig. 5 class-B test circuit at f = 900 MHz.

List of components

C1 = C3 = C8 = C9	1,4 – 5,5 pF film dielectric trimmer (cat. no. 2222 809 09001)
C2	4,7 pF multilayer ceramic chip capacitor*
C4 = C6 = C10	220 pF multilayer ceramic chip capacitor
C5	1 μF (63 V) electrolytic capacitor
C7	2,2 pF multilayer ceramic chip capacitor*
L1	50 Ω stripline (48 mm x 2,4 mm)
L2	60 nH; 7 turns closely wound enamelled Cu-wire (0,4 mm); int. dia. 2 mm; leads 2 x 5 mm
L3 = L7	Ferroxcube wide-band h.f. choke; grade 3B; (cat. no. 4312 020 36642)
L4 = L5	35 Ω stripline (14 mm x 4,0 mm)
L6	120 nH; 6 turns Cu-wire (1,0 mm); int. dia. 6 mm; length 10 mm leads 2 x 5 mm
L8	50 Ω stripline (31 mm x 2,4 mm)
L9	50 Ω stripline (29 mm x 2,4 mm)
R1 = R2	10 Ω ± 5% (0,4 W) metal film resistor

The striplines are on a Cu-clad printed-circuit board with a PTFE fibre-glass dielectric (ϵ_r = 2,2); thickness 1/32 inch.

* American Technical Ceramics capacitor type 100A or capacitor of the same quality.



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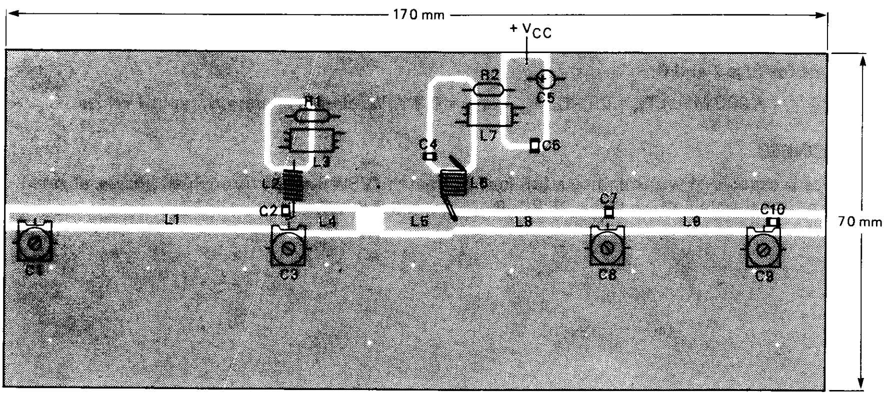

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Fig. 6 Printed-circuit board and component layout for 900 MHz class-B test circuit.

Note:

The circuit and the components are on one side of the PTFE fibre-glass board; the other side is unetched copper serving as a ground plane. Earth connections are made by hollow rivets and also by fixing screws and copper straps under the emitters to provide a direct contact between the copper on the component side and the ground plane.

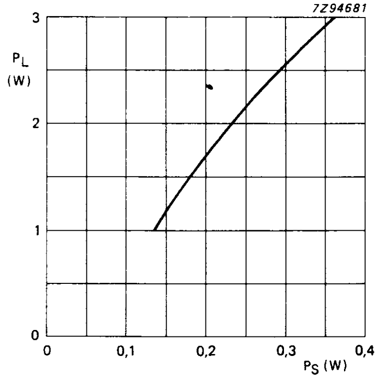

Fig. 7 Load power versus source power.

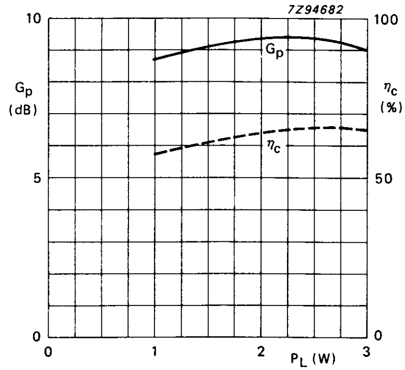

Fig. 8 Power gain and efficiency versus load power.

Conditions for Figs 7 and 8:

V_{CE} = 24 V; f = 900 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0,8 K/W; class-B operation; typical values.

RUGGEDNESS

The device is capable of withstanding a full load mismatch (VSWR = 50) through all phases, at rated load power and supply voltage (T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0,8 K/W).

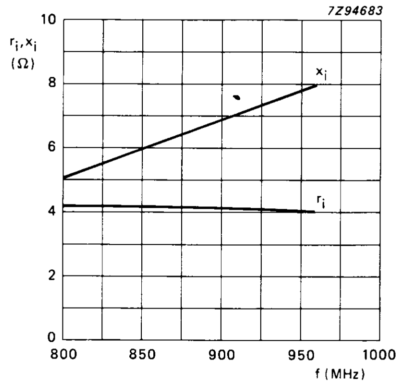

Fig. 9 Input impedance (series components).

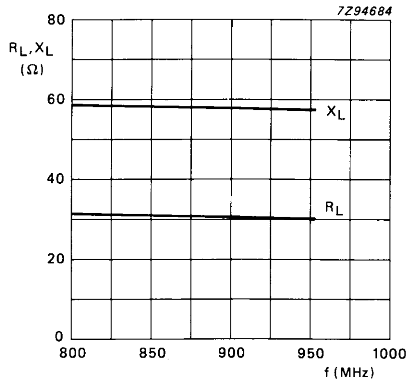

Fig. 10 Load impedance (series components).

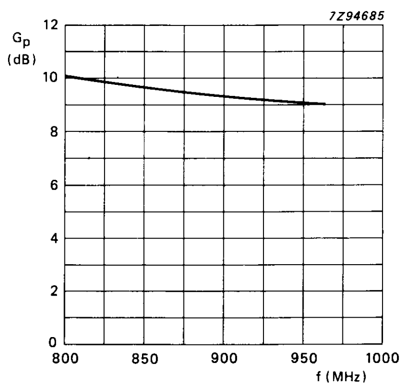

Fig. 11 Power gain versus frequency.

Conditions for Figs 9, 10 and 11:

V_{CE} = 24 V; P_L = 2 W; f = 800 – 960 MHz; $R_{th\ mb\text{-}h}$ = 0,8 K/W; T_h = 25 °C; class-B operation; typical values.