FAST GATE TURN-OFF THYRISTORS

Thyristors in SOT-93 envelopes which are capable of being turned both on and off via the gate, and may be used with gate-assisted turn-off in anode-commutated circuits. They are suitable for use in resonant power supplies, high-frequency inverters, motor control etc. The devices have no reverse blocking capability; for reverse blocking operation use with a series diode, for reverse conducting operation use with an anti-parallel diode. The anode is connected to the mounting base.

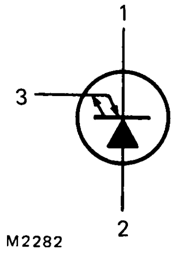
QUICK REFERENCE DATA

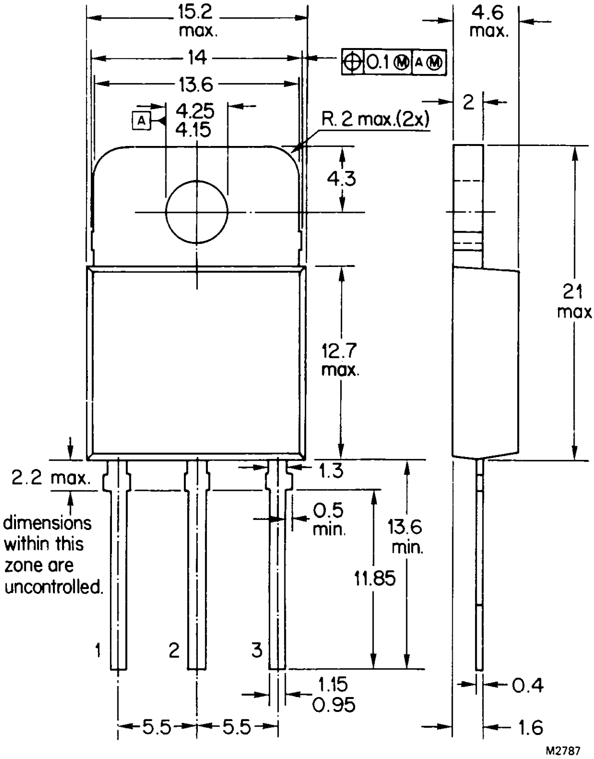
			BTR59–800R	1300R	
Repetitive peak off-state voltage	V_{DRM}	max.	800	1300	V
Controllable anode current	I_{TCRM}	max.	50		A
Average on-state current	$I_{T(AV)}$	max.	10		A
Circuit commutated turn-off time	t_q	<	1.0		μs

MECHANICAL DATA

Dimensions in mm

Fig.1 SOT93; anode connected to mounting base.





Accessories supplied on request; see data sheets Mounting instructions and accessories for SOT-93 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134).

Anode to cathode

			BTR59–800R	1300R	
Transient off-state voltage	V_{DSM}	max.	800	1300	V*
Repetitive peak off-state voltage	V_{DRM}	max.	800	1300	V*
Working off-state voltage	V_{DW}	max.	600	1000	V*
Continuous off-state voltage	V_D	max.	400	750	V*
Average on-state current (averaged over any 20 ms period) up to T_{mb} = 85 °C	$I_{T(AV)}$	max.	10		A
R.M.S. on-state current	$I_{T(RMS)}$	max.	16.5		A
Controllable anode current	I_{TCRM}	max.	50		A
Non-repetitive peak on-state current t = 10 ms; half-sinewave; T_j = 120 °C prior to surge	I_{TSM}	max.	100		A
I^2t for fusing; t = 10 ms	I^2t	max.	50		A^2s
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	105		W

Gate to cathode

Repetitive peak current T_j = 120 °C prior to surge gate-cathode forward; t = 10 ms; half-sinewave	I_{GFM}	max.	25	A
gate-cathode reverse; t = 20 µs	I_{GRM}	max.	25	A
Average power dissipation (averaged over any 20 ms period)	$P_{G(AV)}$	max.	5.0	W

Temperatures

Storage temperature	T_{stg}		−40 to +125	°C
Operating junction temperature	T_j	max.	120	°C

THERMAL RESISTANCE

From mounting base to heatsink; with heatsink compound	$R_{th\ mb\text{-}h}$	=	0.2	K/W
From junction to mounting base	$R_{th\ j\text{-}mb}$	=	0.9	K/W

---

*Measured with gate-cathode connected together.

CHARACTERISTICS

Anode to cathode

On-state voltage I_T = 10 A; I_G = 0.5 A; T_j = 120 °C	V_T	<	3.0	V*
Rate of rise of off-state voltage that will not trigger any off-state device; exponential method V_D = 2/3 V_{Dmax}; V_{GR} = 5 V; T_j = 120 °C	dV_D/dt	<	10	kV/μs
Rate of rise of off-state voltage that will not trigger any device following conduction, linear method I_T = 20 A; V_D = V_{DRMmax}; V_{GR} = 10 V; T_j = 120 °C	dV_D/dt	<	1.0	kV/μs
Off-state current V_D = V_{Dmax}; T_j = 120 °C	I_D	<	5.0	mA
Latching current; T_j = 25 °C	I_L	typ.	1.5	A**

Gate to cathode

Voltage that will trigger all devices V_D = 12 V; T_j = 25 °C	V_{GT}	>	1.5	V
Current that will trigger all devices V_D = 12 V; T_j = 25 °C	I_{GT}	>	500	mA
Minimum reverse breakdown voltage I_{GR} = 1.0 mA	$V_{(BR)GR}$	>	10	V

Switching characteristics (resistive load)

Turn-on when switched to I_T = 10 A from V_D = 250 V with I_{GF} = 2.5 A; T_j = 25 °C				
delay time	t_d	<	0.3	μs
rise time	t_r	<	1.5	μs

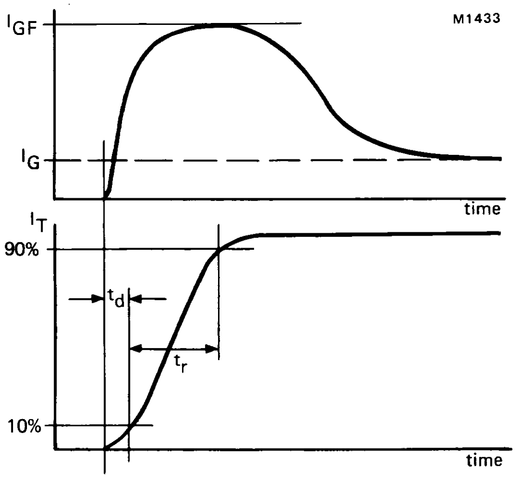


Fig.2 Waveforms.

---

*Measured under pulse conditions to avoid excessive dissipation.

**Below latching level the device behaves like a transistor with a gain dependent on current.

Switching characteristics (inductive load)

Turn-off when switched from I_T = 10 A to $V_D = V_{Dmax}$;

V_{GR} = 10 V; $L_G \leqslant 0.5$ µH; $L_S \leqslant 0.25$ µH; $C_S \geqslant 20$ nF; T_j = 85 °C

storage time	t_s	<	0.60	µs
fall time	t_f	<	0.25	µs
peak reverse gate current	I_{GR}	<	10	A

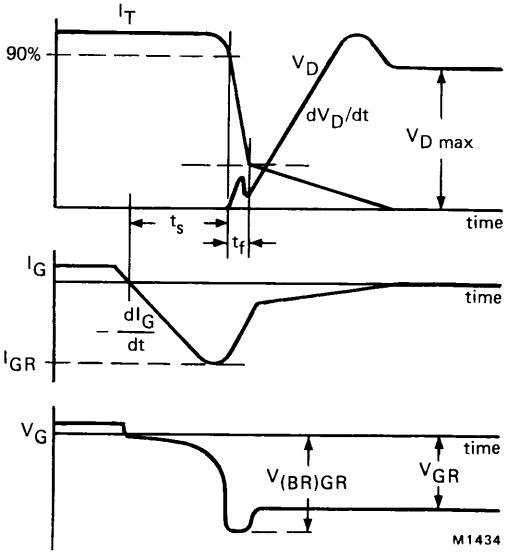


Fig.3 Waveforms.

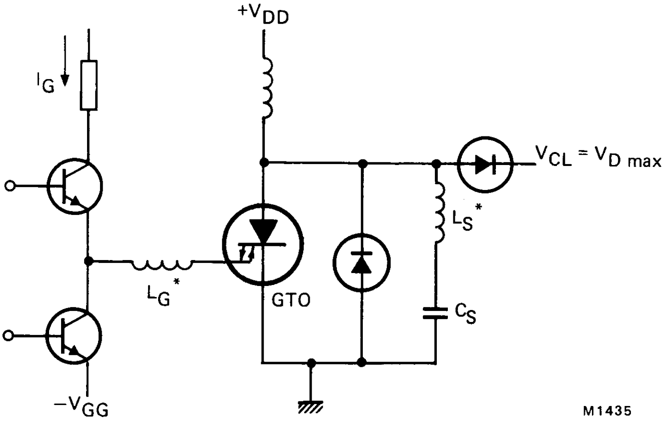


Fig.4 Inductive load test circuit.

*Indicates stray series inductance only.

Switching characteristics (circuit-commutated)*

Turn-off time

I_T = 50 A; $-dI_T/dt$ = 10 A/µs; dV_D/dt = 200 V/µs;
V_{GR} = 5 V; T_j = 120 °C t_q < 1.0 µs

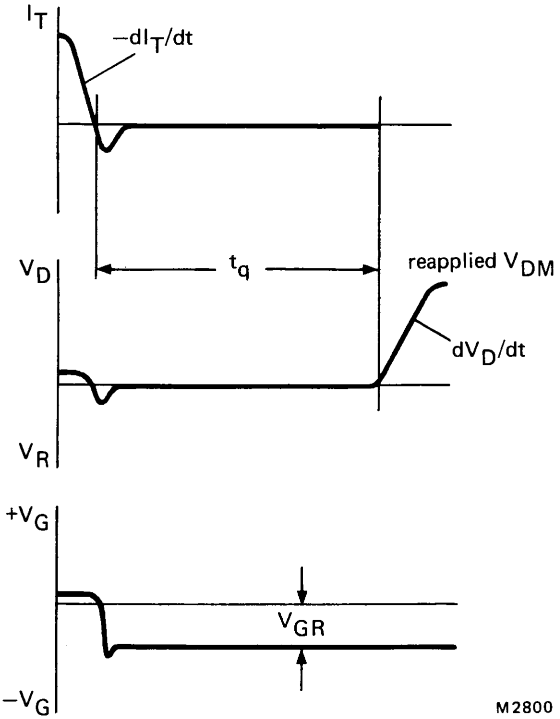


Fig.5 Circuit-commutated turn-off time definition.

---

*Figs. 7, 11, 12, 13, 15, 16, 17 do not apply to commutated turn-off.

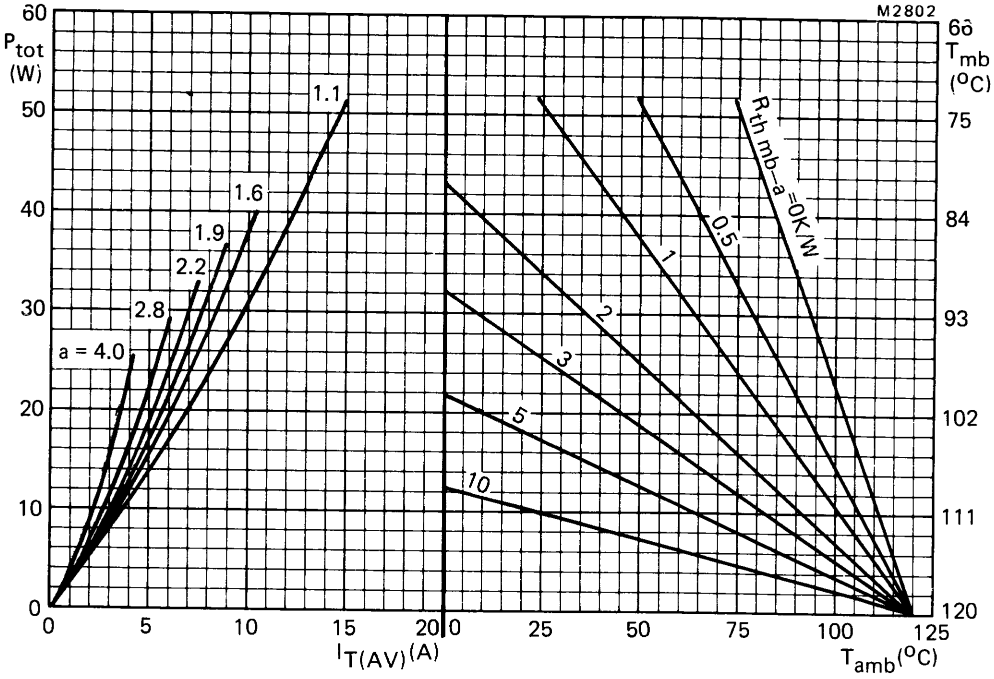


Fig.6 The right hand part shows the interrelationship between the power (derived from the left-hand part) and the maximum permissible temperatures.

$$a = \text{form factor} = \frac{I_{T(RMS)}}{I_{T(AV)}}$$

P = power excluding switching losses.

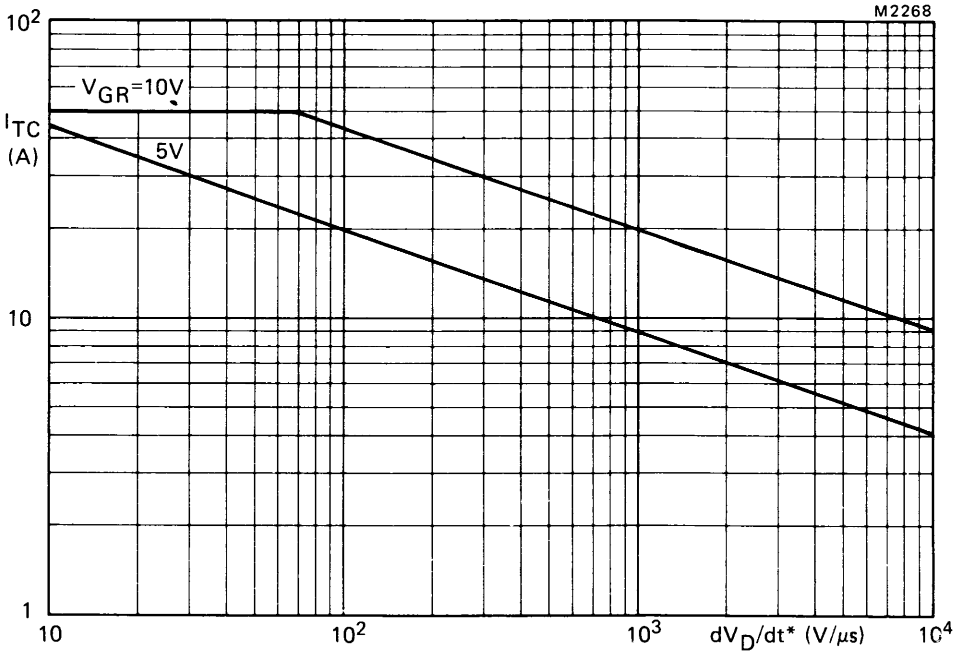


Fig.7 Anode current which can be turned off versus applied dV_D/dt^*; inductive load; $L_G \leqslant 0.5$ μH; $L_S \leqslant 0.25$ μH; T_j = 120 °C.

$^*dV_D/dt$ is calculated from I_T/C_S.

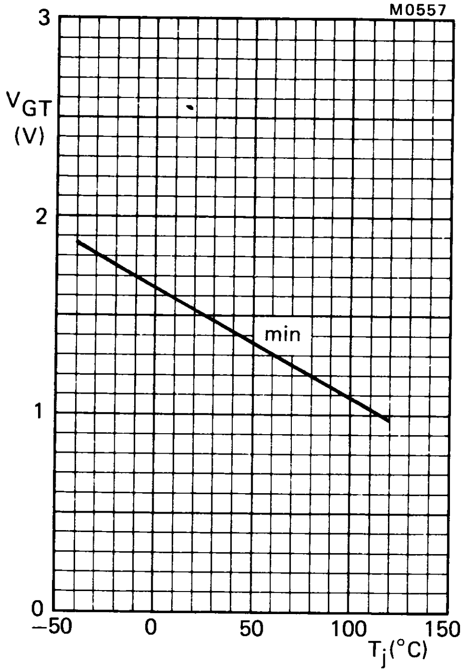


Fig.8 Minimum gate voltage that will trigger all devices as a function of junction temperature; V_D = 12 V.

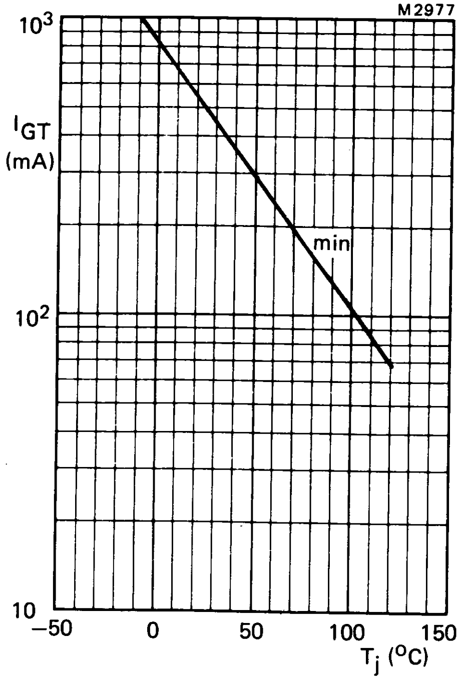


Fig.9 Minimum gate current that will trigger all devices as a function of junction temperature; V_D = 12 V.

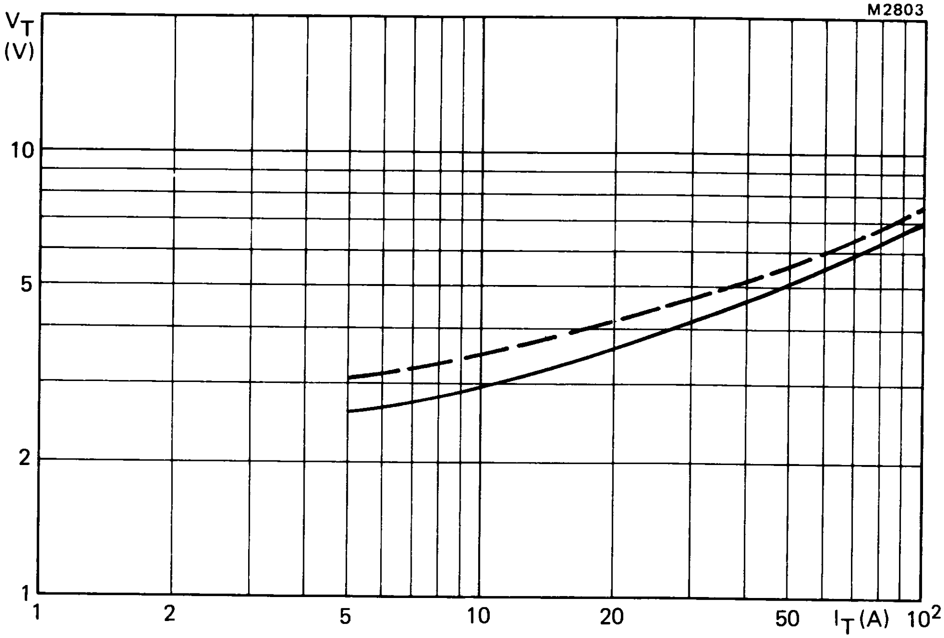


Fig.10 Maximum V_T versus I_T; — — — T_j = 25 °C; —— T_j = 120 °C; I_G = 0.5 A.

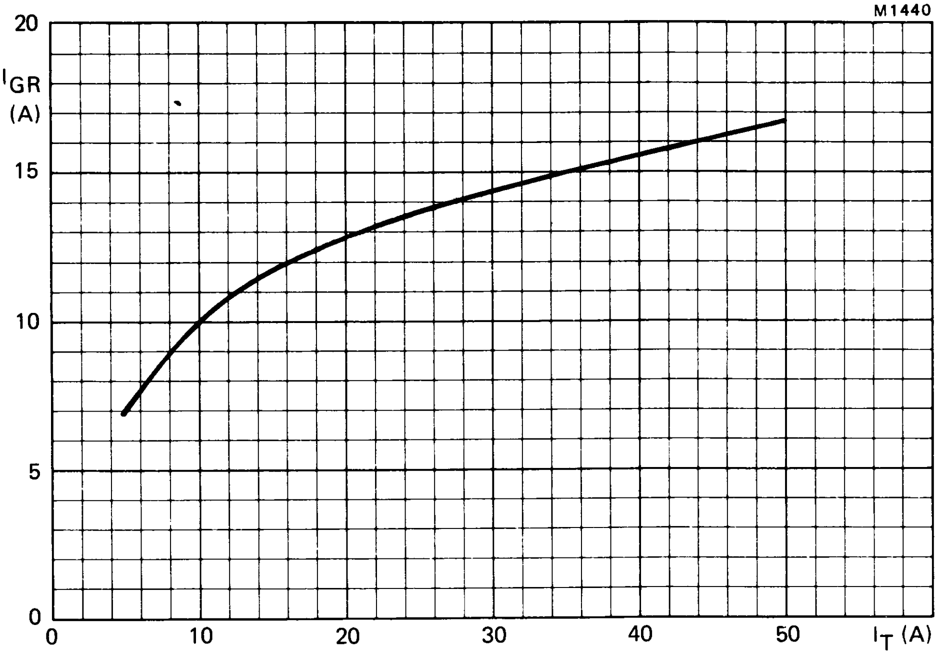


Fig.11 Peak reverse gate current versus anode current at turn-off; inductive load; V_{GR} = 10 V; I_G = 0.5 A; L_G = 0.4 μH; T_j = 120 °C; maximum values.

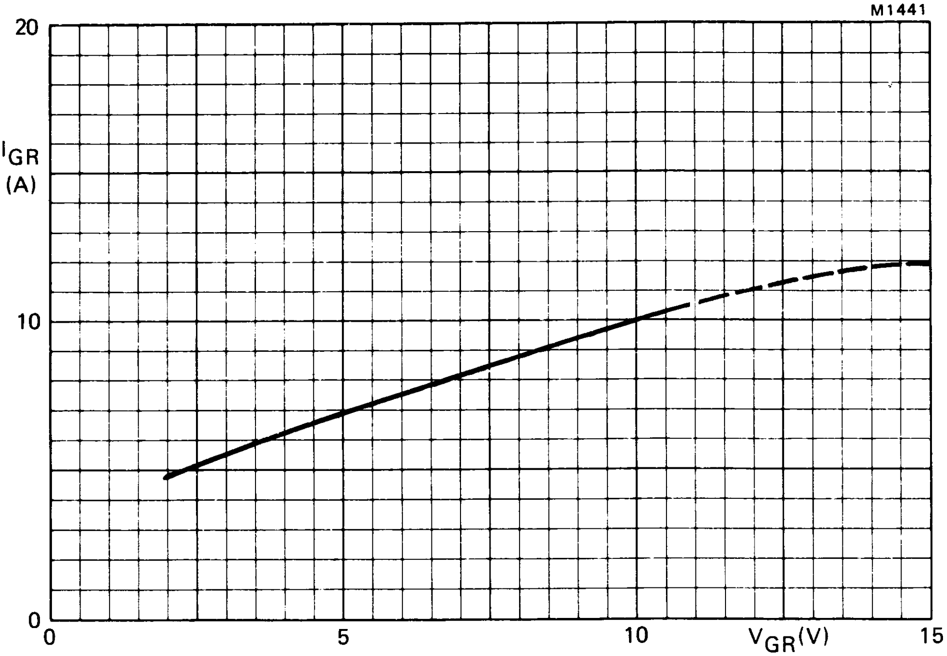


Fig.12 Peak reverse gate current versus applied reverse gate voltage; inductive load; I_T = 10 A; I_G = 0.5 A; L_G = 0.4 μH; T_j = 120 °C; maximum values.

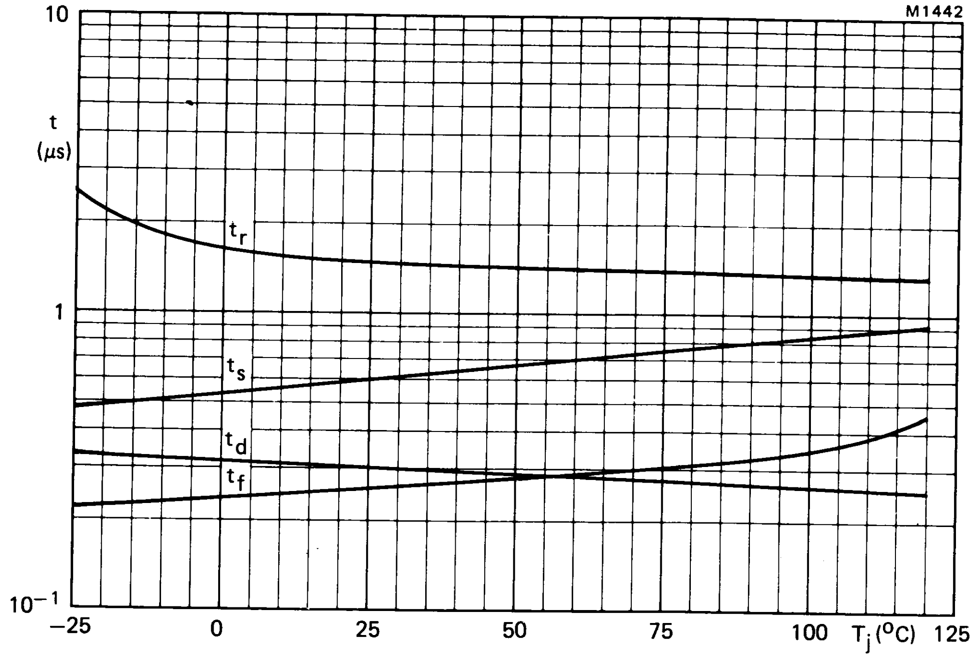


Fig.13 Switching times as a function of junction temperature; $V_D \geqslant 250$ V; $I_T = 10$ A; $I_{GF} = 1.0$ A; $V_{GR} = 10$ V; $I_G = 0.5$ A; $L_G = 0.4$ µH; maximum values.

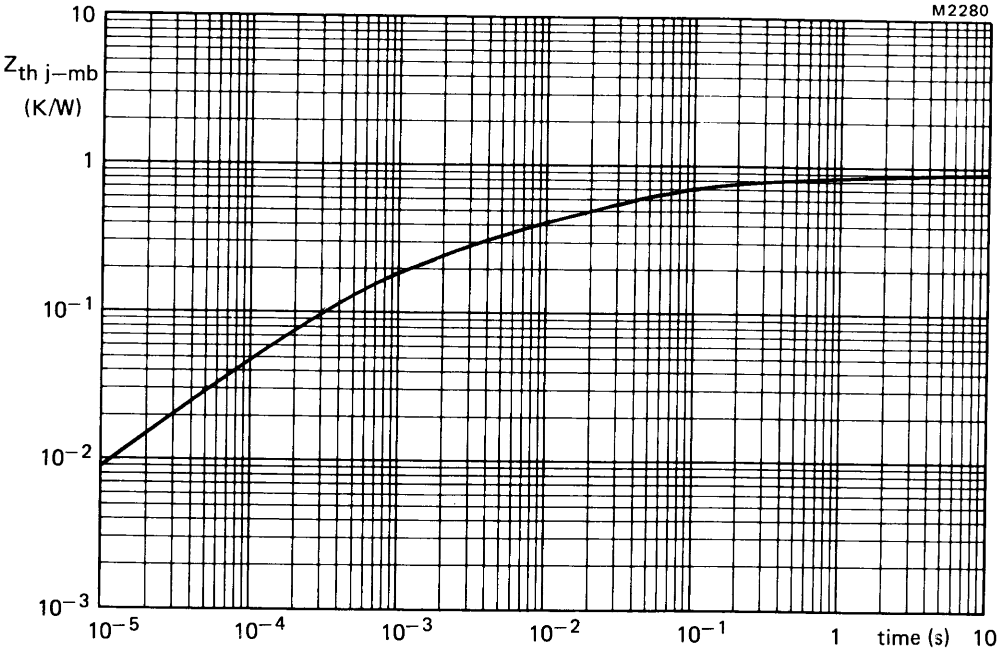


Fig.14 Transient thermal impedance.

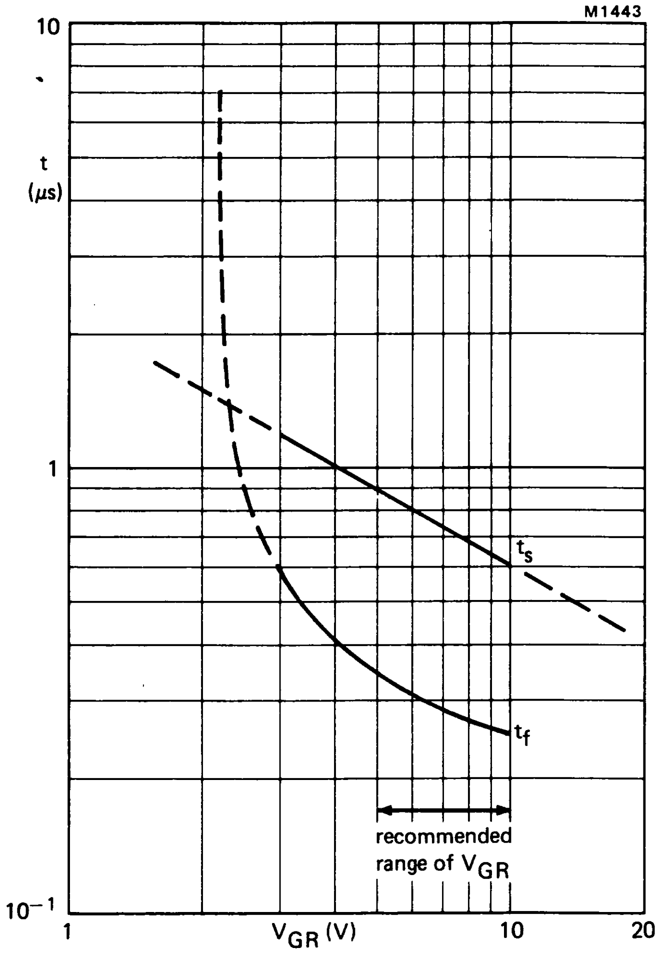


Fig.15 Storage and fall times versus applied reverse gate voltage; inductive load, I_T = 10 A; I_G = 0.5 A; L_G = 0.4 μH; T_j = 25 °C; maximum values.

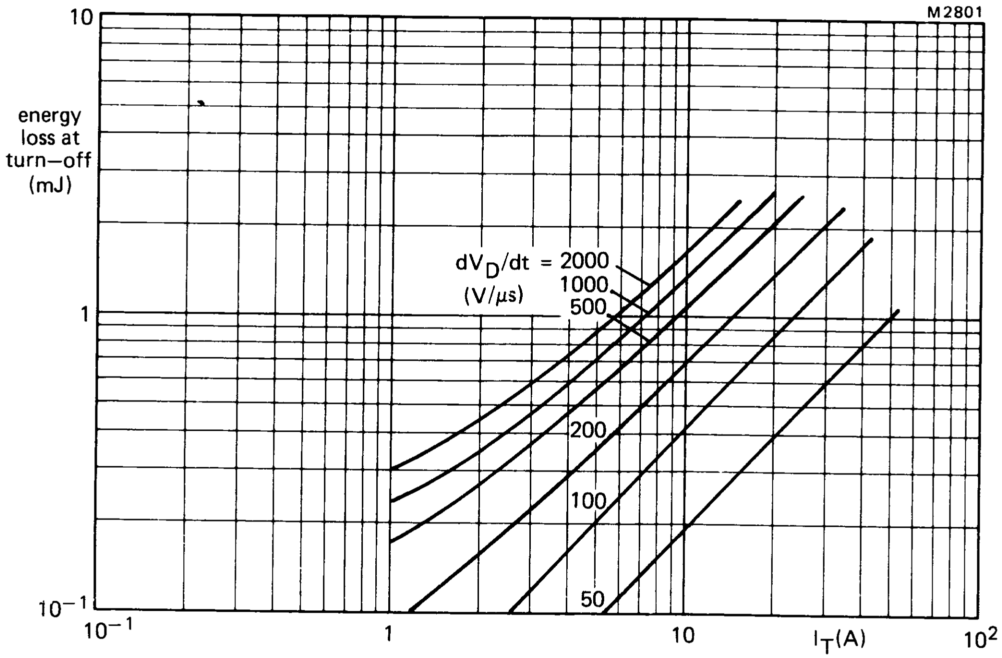


Fig.16 Maximum energy loss at turn-off (per cycle) as a function of anode current and applied dV_D/dt (calculated from I_T/C_S); dV_D/dt linear up to $V_D = V_{DWmax}$; V_{GR} = 10 V; I_G = 0.5 A; $L_G < 0.5$ μH; $L_S < 0.25$ μH; T_j = 120 °C.

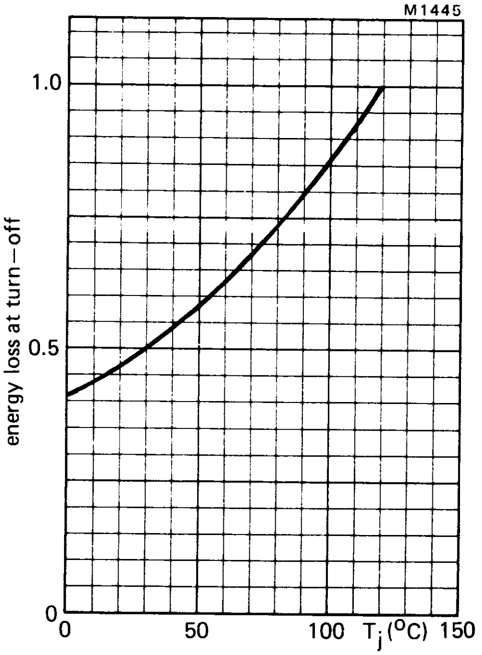


Fig.17 Energy loss at turn-off as a function of junction temperature; I_G = 0.5 A; V_{GR} = 10 V. Normalised to T_j = 120 °C.

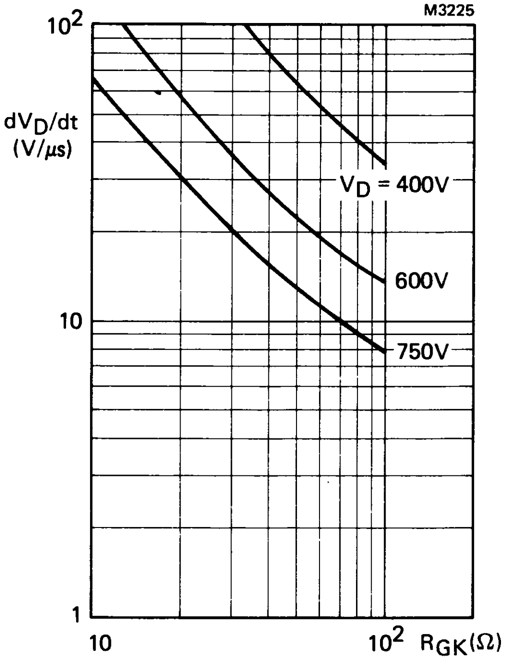


Fig.18 Linear rate of rise of off-state voltage versus gate-cathode resistance; T_j = 25 °C; typical values.

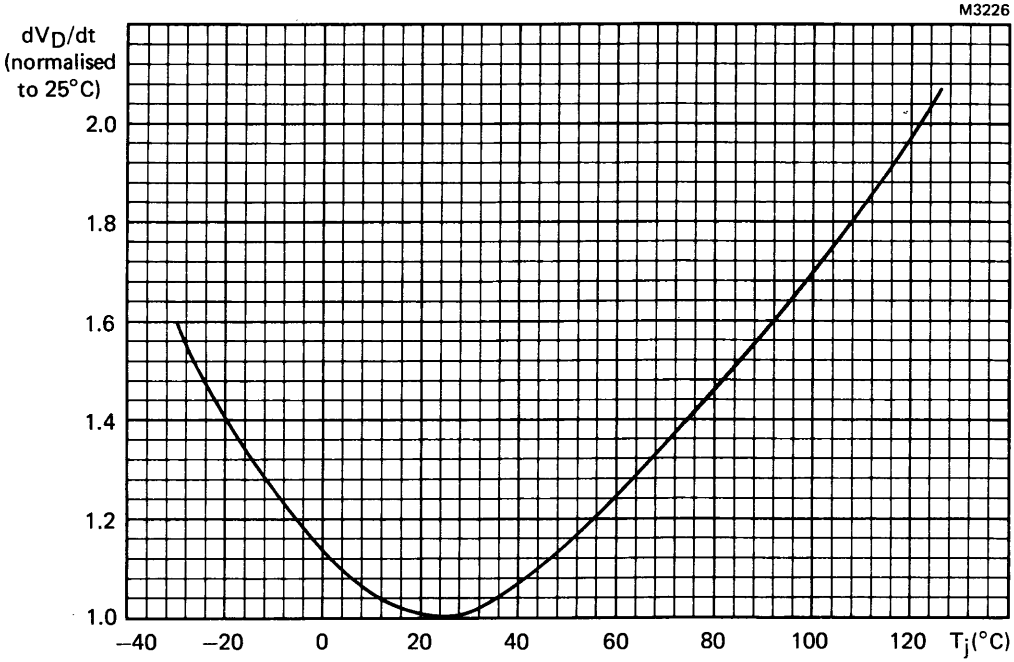


Fig.19 Rate of rise of off-state voltage versus junction temperature, normalised to 25 °C; V_{Dmax} = 750V; R_{GK} = 22 Ω; typical values.

FAST GATE TURN-OFF THYRISTORS

Thyristors in SOT-93 envelopes capable of being turned both on and off via the gate. They are suitable for use in high-frequency inverters, power supplies, motor control etc. The devices have no reverse blocking capability; for reverse blocking operation use with a series diode, for reverse conducting operation use with an anti-parallel diode. The anode is connected to the mounting base.

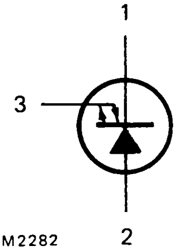
QUICK REFERENCE DATA

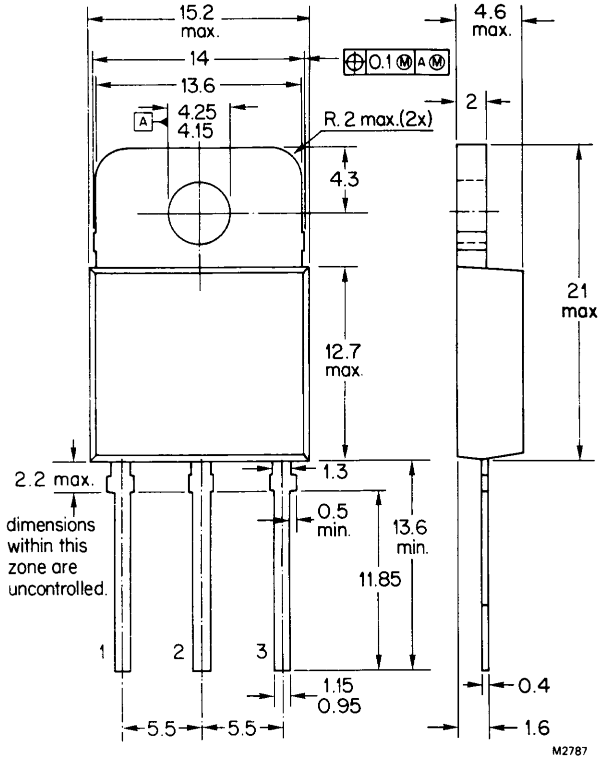
			BTS59-850R	1000R	1200R	
Repetitive peak off-state voltage	V_{DRM}	max.	850	1000	1200	V
Non-repetitive peak on-state current	I_{TSM}	max.		100		A
Controllable anode current	I_{TCRM}	max.		50		A
Average on-state current	$I_{T(AV)}$	max.		15		A
Fall time	t_f	<		250		ns

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-93; anode connected to mounting base





Accessories supplied on request: see data sheets Mounting instructions and accessories for SOT-93 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

Anode to cathode

			BTS59-850R	1000R	1200R	
Transient off-state voltage	V_{DSM}	max.	1000	1100	1300	V*
Repetitive peak off-state voltage	V_{DRM}	max.	850	1000	1200	V*
Working off-state voltage	V_{DW}	max.	600	800	1000	V*
Continuous off-state voltage	V_D	max.	500	650	750	V*
Average on-state current (averaged over any 20 ms period) up to T_{mb} = 85 °C	$I_{T(AV)}$	max.	15			A
Controllable anode current	I_{TCRM}	max.	50			A
Non-repetitive peak on-state current t = 10 ms; half-sinewave; T_j = 120 °C prior to surge	I_{TSM}	max.	100			A
I^2t for fusing; t = 10 ms	I^2t	max.	50			A^2s
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	105			W

Gate to cathode

Repetitive peak current T_j = 120 °C prior to surge gate-cathode forward; t = 10 ms; half-sinewave	I_{GFM}	max.	25	A
gate-cathode reverse; t = 20 µs	I_{GRM}	max.	25	A
Average power dissipation (averaged over any 20 ms period)	$P_{G(AV)}$	max.	5.0	W

Temperatures

Storage temperature	T_{stg}		−40 to +125	°C
Operating junction temperature	T_j	max.	120	°C

THERMAL RESISTANCE

From mounting base to heatsink; with heatsink compound	$R_{th\ mb\text{-}h}$	=	0.2	K/W
From junction to mounting base	$R_{th\ j\text{-}mb}$	=	0.9	K/W

---

* Measured with gate-cathode connected together.

CHARACTERISTICS

Anode to cathode

On-state voltage $I_T = 10$ A; $I_G = 0.5$ A; $T_j = 120$ °C	V_T	$<$	2.3	V*
Rate of rise of off-state voltage that will not trigger any off-state device; exponential method $V_D = 2/3\ V_{Dmax}$; $V_{GR} = 5$ V; $T_j = 120$ °C	dV_D/dt	$<$	10	kV/µs
Rate of rise of off-state voltage that will not trigger any device following conduction, linear method $I_T = 20$ A; $V_D = V_{DRMmax}$; $V_{GR} = 10$ V; $T_j = 120$ °C	dV_D/dt	$<$	1.0	kV/µs
Off-state current $V_D = V_{Dmax}$; $T_j = 120$ °C	I_D	$<$	5.0	mA
Latching current; $T_j = 25$ °C	I_L	typ.	1.5	A**

Gate to cathode

Voltage that will trigger all devices $V_D = 12$ V; $T_j = 25$ °C	V_{GT}	$>$	1.5	V
Current that will trigger all devices $V_D = 12$ V, $T_j = 25$ °C	I_{GT}	$>$	300	mA
Minimum reverse breakdown voltage $I_{GR} = 1.0$ mA	$V_{(BR)GR}$	$>$	10	V

Switching characteristics (resistive load)

Turn-on when switched to $I_T = 10$ A from $V_D = 250$ V with $I_{GF} = 1.5$ A; $T_j = 25$ °C				
delay time	t_d	$<$	0.3	µs
rise time	t_r	$<$	1.5	µs

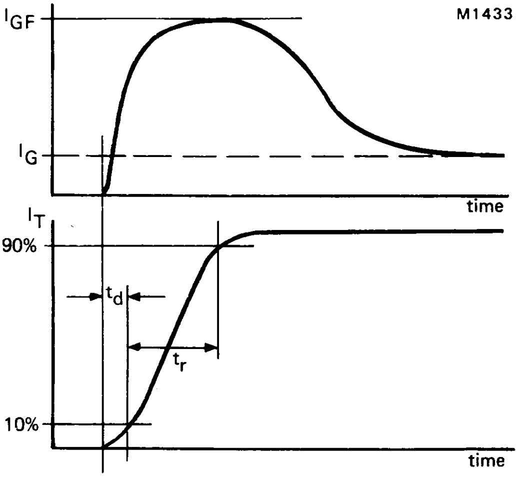


Fig.2 Waveforms

---

* Measured under pulse conditions to avoid excessive dissipation.

** Below latching level the device behaves like a transistor with a gain dependent on current.

Switching characteristics (inductive load)

Turn-off when switched from I_T = 10 A to $V_D = V_{Dmax}$;

V_{GR} = 10 V; $L_G \leqslant 0.5\ \mu H$; $L_S \leqslant 0.25\ \mu H$; $C_S \geqslant 20$ nF; T_j = 25 °C

storage time	t_s	<	0.60	μs
fall time	t_f	<	0.25	μs
peak reverse gate current	I_{GR}	<	10	A

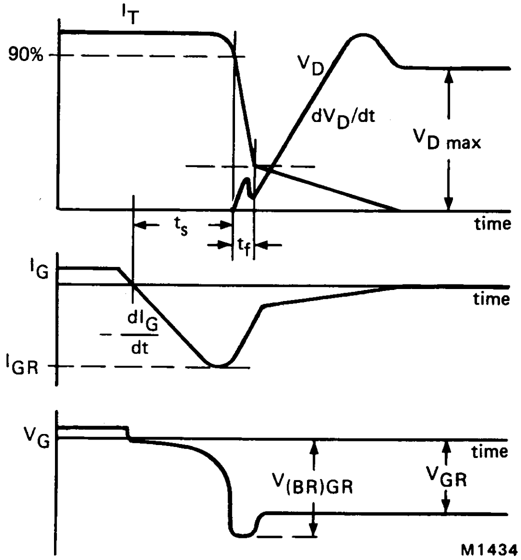


Fig.3 Waveforms.

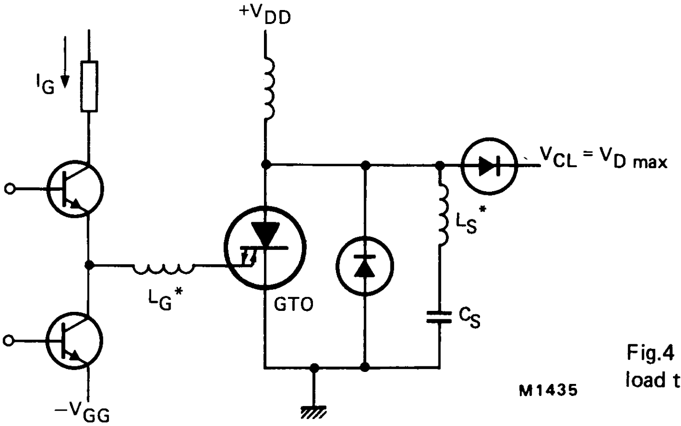


Fig.4 Inductive load test circuit.

*Indicates stray series inductance only

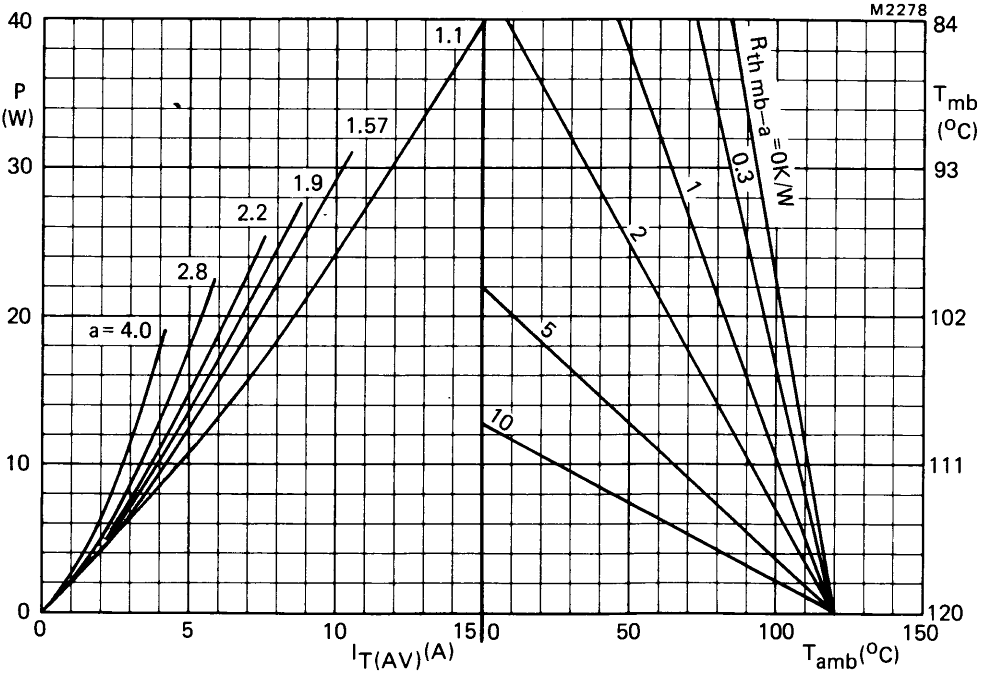


Fig.5 The right hand part shows the interrelationship between the power (derived from the left-hand part) and the maximum permissible temperatures.

a = form factor = $\frac{I_{T(RMS)}}{I_{T(AV)}}$

P = power excluding switching losses.

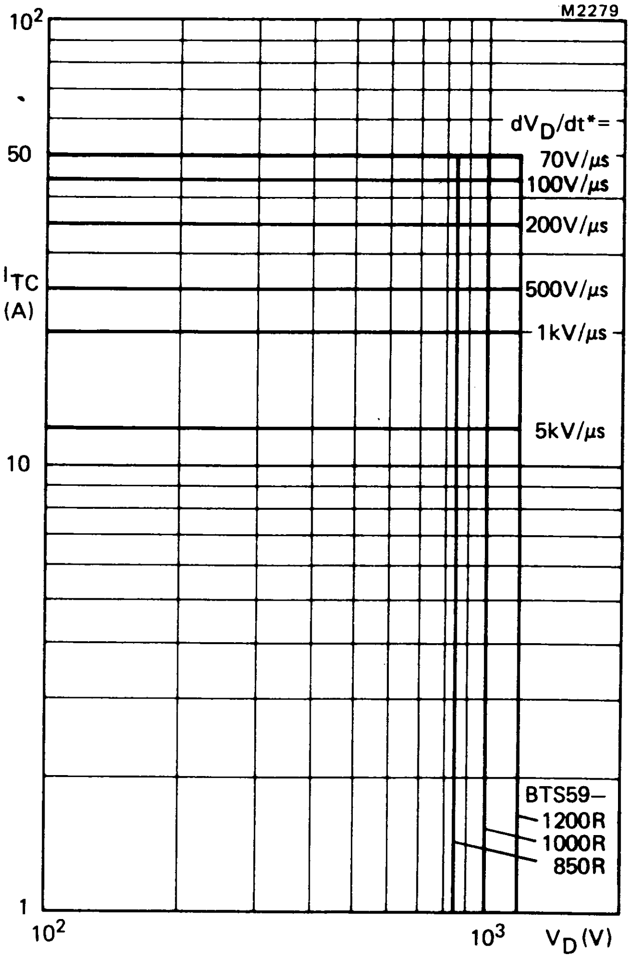


Fig.6 Anode current which can be turned off versus anode voltage; inductive load; V_{GR} = 10 V; $L_G \leqslant 0.5$ µH; $L_S \leqslant 0.25$ µH; T_j = 120 °C.
*dV_D/dt is calculated from I_T/C_S.

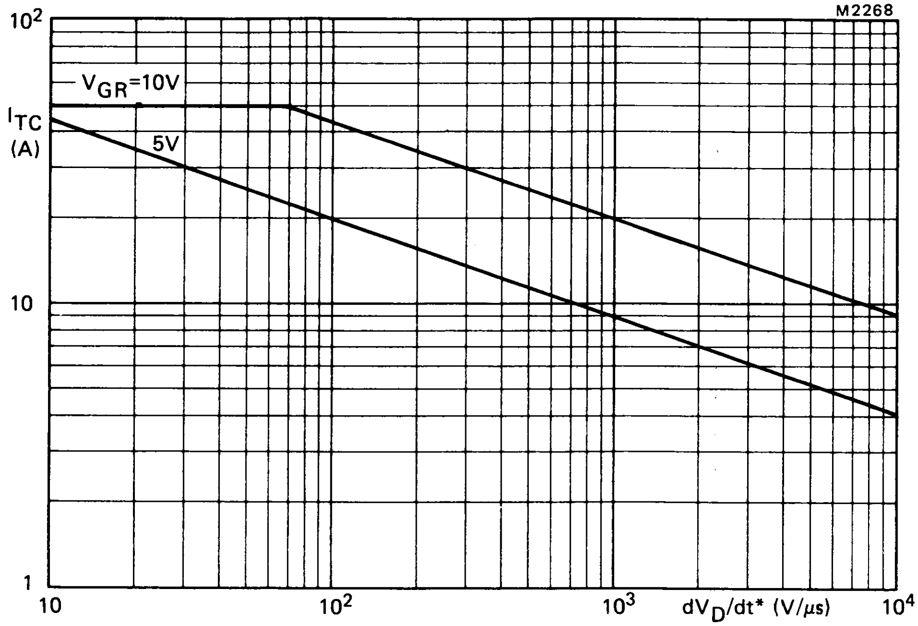


Fig.7 Anode current which can be turned off versus applied dV_D/dt^*; inductive load; $L_G \leqslant 0.5$ µH; $L_S \leqslant 0.25$ µH; T_j = 120 °C. $^*dV_D/dt$ is calculated from I_T/C_S.

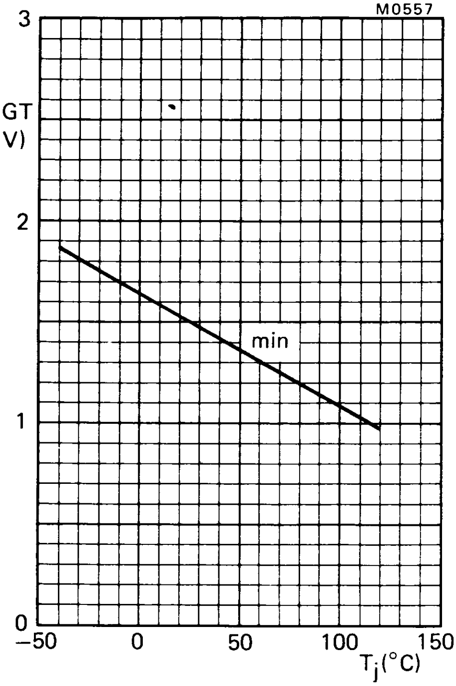


Fig.8 Minimum gate voltage that will trigger all devices as a function of junction temperature; V_D = 12 V.

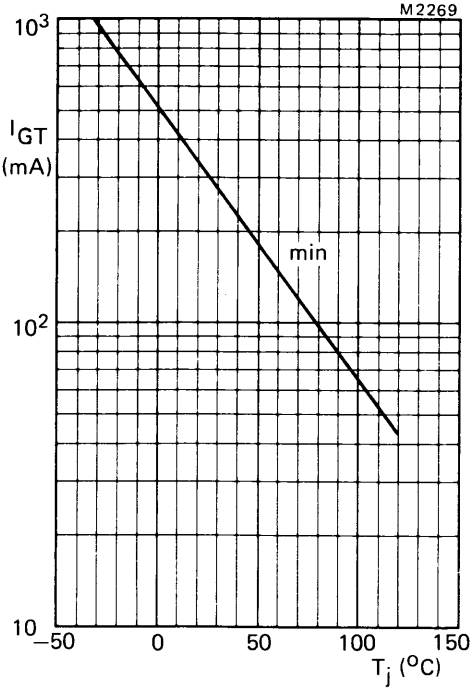


Fig.9 Minimum gate current that will trigger all devices as a function of junction temperature; V_D = 12 V.

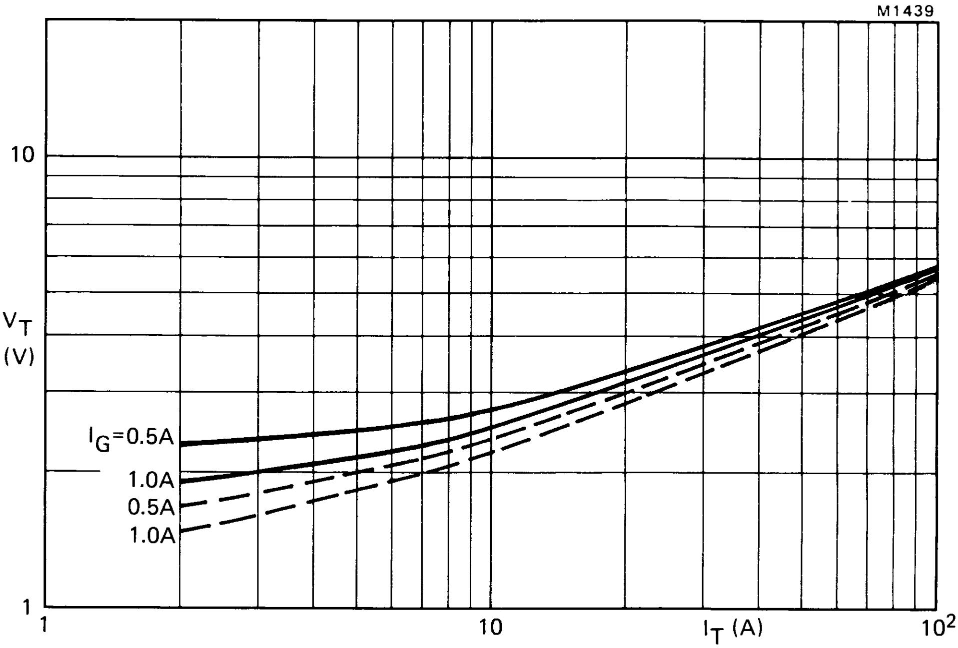


Fig.10 Maximum V_T versus I_T; —— T_j = 25 °C; – – – – T_j = 120 °C.

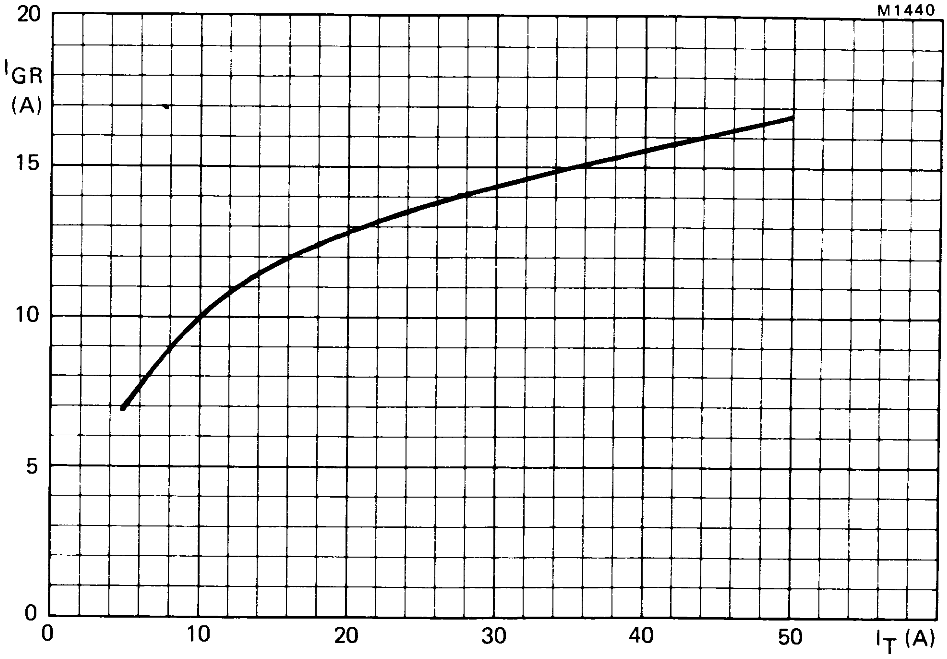


Fig.11 Peak reverse gate current versus anode current at turn-off; inductive load;
V_{GR} = 10 V; I_G = 0.5 A; L_G = 0.4 μH; T_j = 120 °C; maximum values.

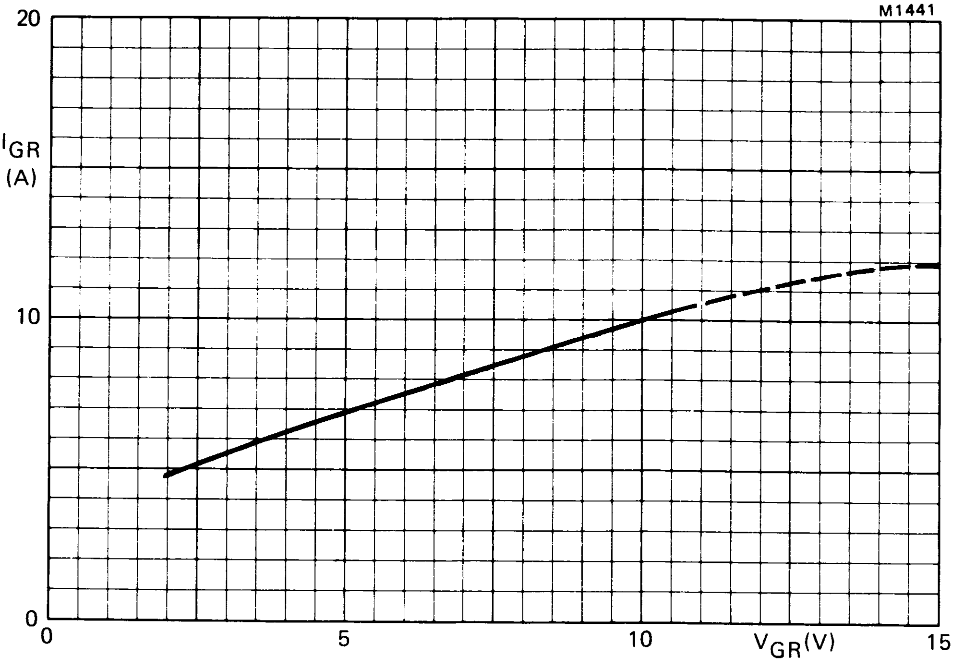


Fig.12 Peak reverse gate current versus applied reverse gate voltage; inductive load;
I_T = 10 A; I_G = 0.5 A, L_G = 0.4 μH; T_j = 120 °C; maximum values.

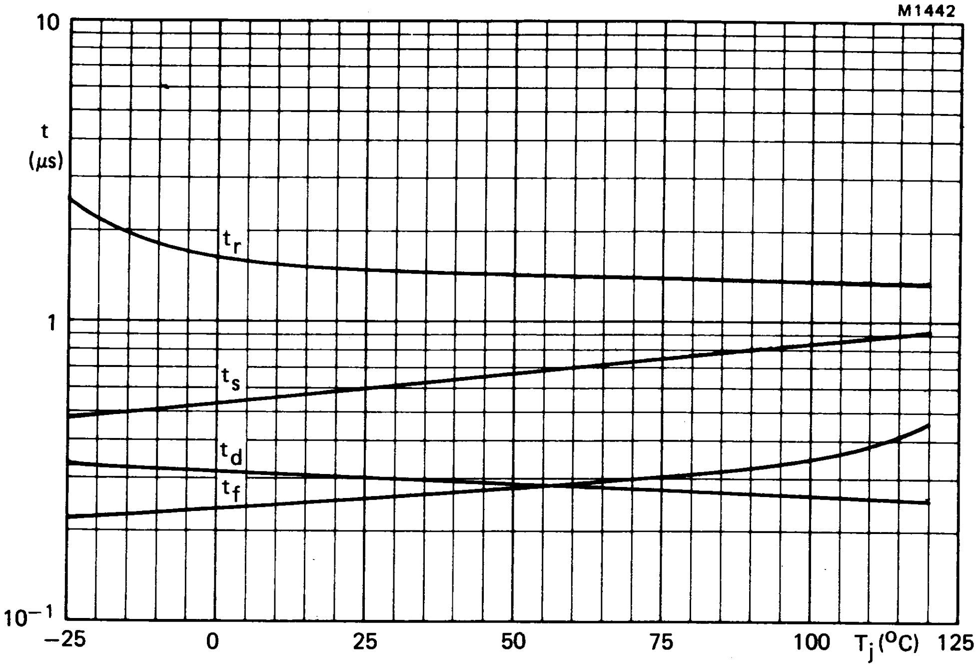


Fig.13 Switching times as a function of junction temperature; $V_D \geqslant 250$ V; $I_T = 10$ A; $I_{GF} = 1.0$ A; $V_{GR} = 10$ V; $I_G = 0.5$ A; $L_G = 0.4$ μH; maximum values.

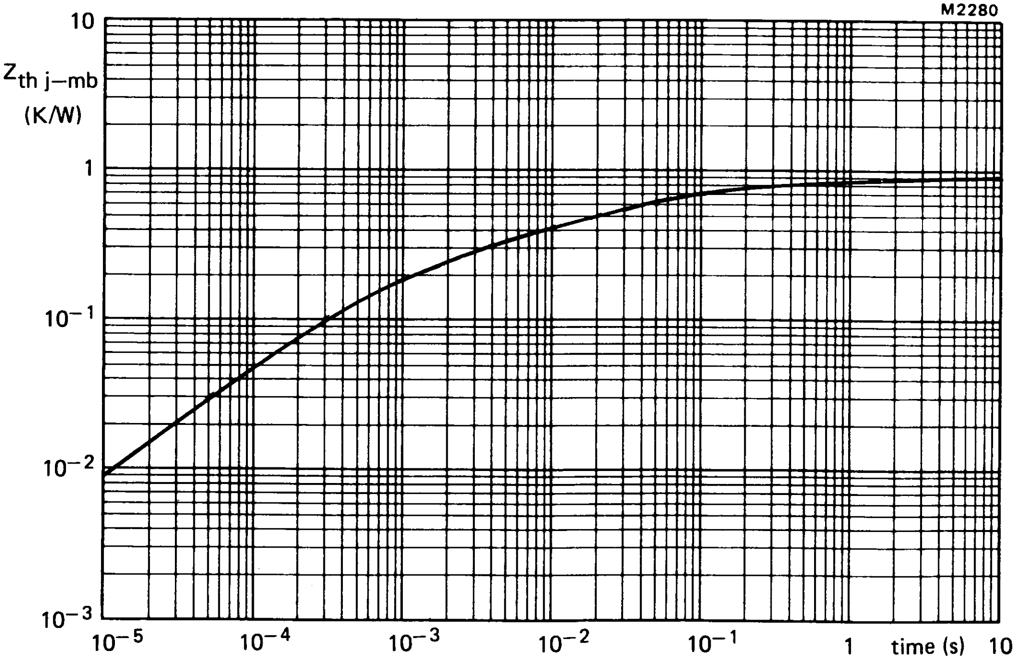


Fig.14 Transient thermal impedance.

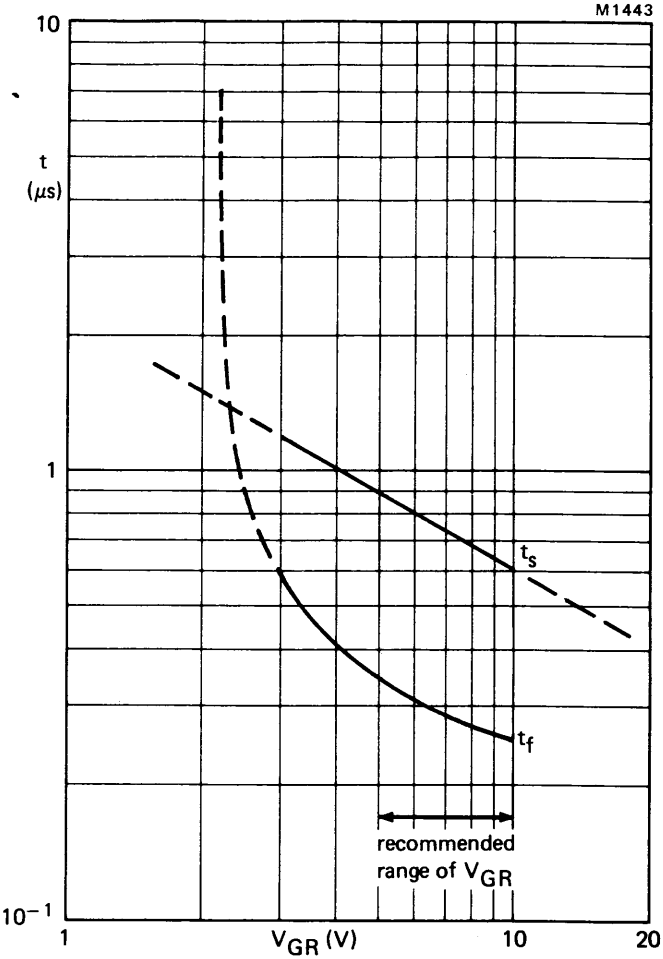


Fig.15 Storage and fall times versus applied reverse gate voltage; inductive load; I_T = 10 A; I_G = 0.5 A; L_G = 0.4 μH; T_j = 25 °C; maximum values.

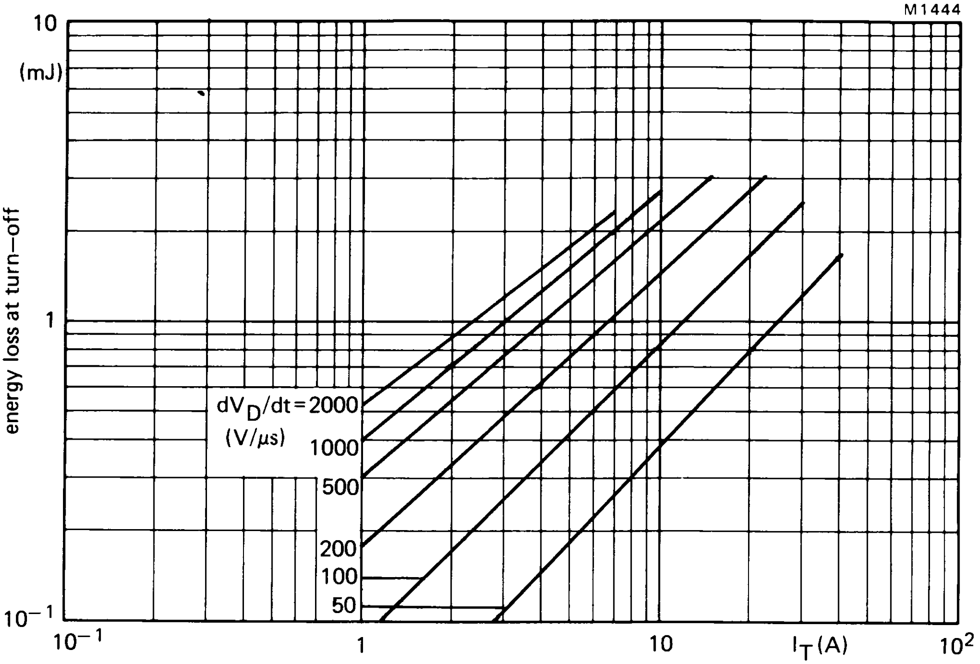


Fig. 16 Maximum energy loss at turn-off (per cycle) as a function of anode current and applied dV_D/dt (calculated from I_T/C_S); dV_D/dt linear up to $V_{Dmax} = 600$ V; $V_{GR} = 10$ V; $I_G = 0.5$ A; $L_G \leqslant 0.5$ µH; $L_S \leqslant 0.25$ µH; $T_j = 120$ °C.

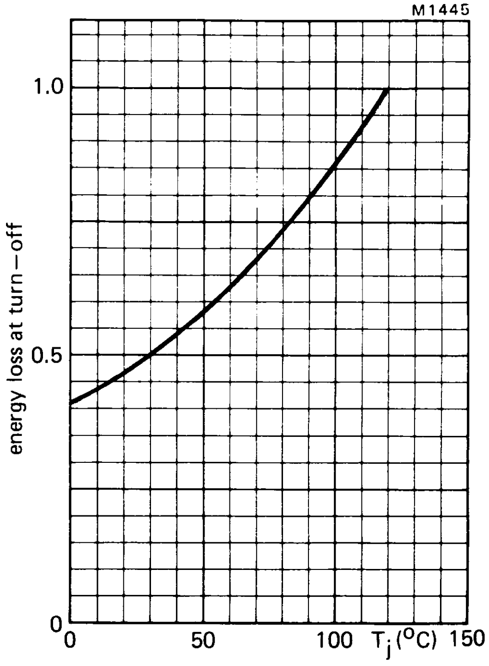


Fig. 17 Energy loss at turn off as a function of junction temperature; $I_G = 0.5$ A; $V_{GR} = 10$ V. Normalised to $T_j = 120$ °C.

Silicon diffused power transistors BUT18F; BUT18AF

DESCRIPTION

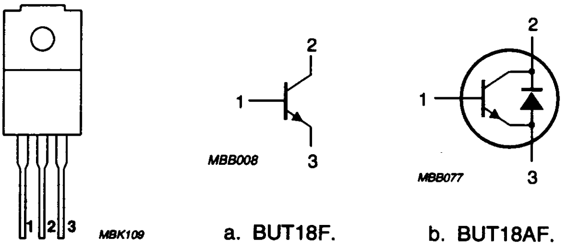
High-voltage, high-speed, glass-passivated NPN power transistor in a SOT186 package with electrically isolated mounting base.

APPLICATIONS

- Converters
- Inverters
- Switching regulators
- Motor control systems.

PINNING

PIN	DESCRIPTION
1	base
2	collector
3	emitter
mb	mounting base; electrically isolated from all pins



a. BUT18F. b. BUT18AF.

Fig.1 Simplified outline (SOT186) and symbols.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{CESM}	collector-emitter peak voltage	$V_{BE} = 0$		
	BUT18F		850	V
	BUT18AF		1 000	V
V_{CEO}	collector-emitter voltage	open base		
	BUT18F		400	V
	BUT18AF		450	V
V_{CEsat}	collector-emitter saturation voltage	see Fig.7	1.5	V
I_{Csat}	collector saturation current		4	A
I_C	collector current (DC)	see Fig.4	6	A
I_{CM}	collector current (peak value)	see Fig.4	12	A
P_{tot}	total power dissipation	$T_h \leq 25$ °C; see Fig.2	33	W
t_f	fall time	resistive load; see Figs 10 and 11	0.8	µs

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}h}$	thermal resistance from junction to external heatsink	note 1	6.15	K/W
		note 2	3.65	K/W

Notes

1. Mounted **without** heatsink compound and 30 ±5 N force on centre of package.
2. Mounted **with** heatsink compound and 30 ±5 N force on centre of package.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CESM}	collector-emitter peak voltage	$V_{BE} = 0$			
	BUT18F		–	850	V
	BUT18AF		–	1000	V
V_{CEO}	collector-emitter voltage	open base			
	BUT18F		–	400	V
	BUT18AF		–	450	V
I_{Csat}	collector saturation current		–	4	A
I_C	collector current (DC)	see Fig.4	–	6	A
I_{CM}	collector current (peak value)	see Fig.4	–	12	A
I_B	base current (DC)		–	3	A
I_{BM}	base current (peak value)		–	6	A
P_{tot}	total power dissipation	$T_h \leq 25$ °C; see Fig.2; note 1	–	20	W
		$T_h \leq 25$ °C; see Fig.2; note 2	–	33	W
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		–	150	°C

Notes

1. **Without** heatsink compound.
2. **With** heatsink compound.

ISOLATION CHARACTERISTICS

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{isolM}	isolation voltage from all terminals to external heatsink (peak value)	–	1500	V
C_{isol}	isolation capacitance from collector to external heatsink	12	–	pF

CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CEOsust}$	collector-emitter sustaining voltage	$I_C = 100$ mA; $I_{Boff} = 0$; L = 25 mH; see Figs 3 and 6				
	BUT18F		400	–	–	V
	BUT18AF		450	–	–	V
V_{CEsat}	collector-emitter saturation voltage	$I_C = 4$ A; $I_B = 800$ mA; see Fig.7	–	–	1.5	V
V_{BEsat}	base-emitter saturation voltage	$I_C = 4$ A; $I_B = 800$ mA; see Fig.8	–	–	1.3	V
I_{CES}	collector-emitter cut-off current	$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$; note 1	–	–	1	mA
		$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$; $T_j = 125$ °C; note 1	–	–	2	mA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 9$ V; $I_C = 0$	–	–	10	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 10 mA; see Fig.9	10	18	35	
		V_{CE} = 5 V; I_C = 1 A; see Fig.9	10	20	35	
Switching times resistive load (see Figs 10 and 11)						
t_{on}	turn-on time	I_{Con} = 4 A; I_{Bon} = $-I_{Boff}$ = 800 mA	–	–	1	µs
t_s	storage time	I_{Con} = 4 A; I_{Bon} = $-I_{Boff}$ = 800 mA	–	–	4	µs
t_f	fall time	I_{Con} = 4 A; I_{Bon} = $-I_{Boff}$ = 800 mA	–	–	0.8	µs
Switching times inductive load (see Figs 10 and 13)						
t_s	storage time	I_{Con} = 4 A; I_{Bon} = 800 mA	–	1.6	2.5	µs
t_f	fall time	I_{Con} = 4 A; I_{Bon} = 800 mA	–	150	400	ns

Note

1. Measured with a half-sinewave voltage (curve tracer).

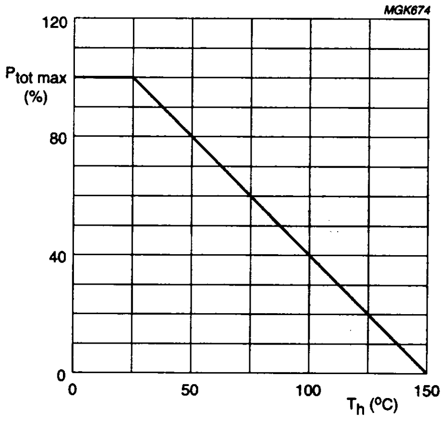


Fig.2 Power derating curve.

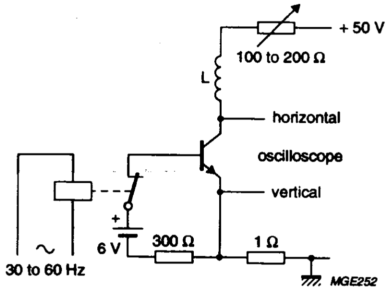
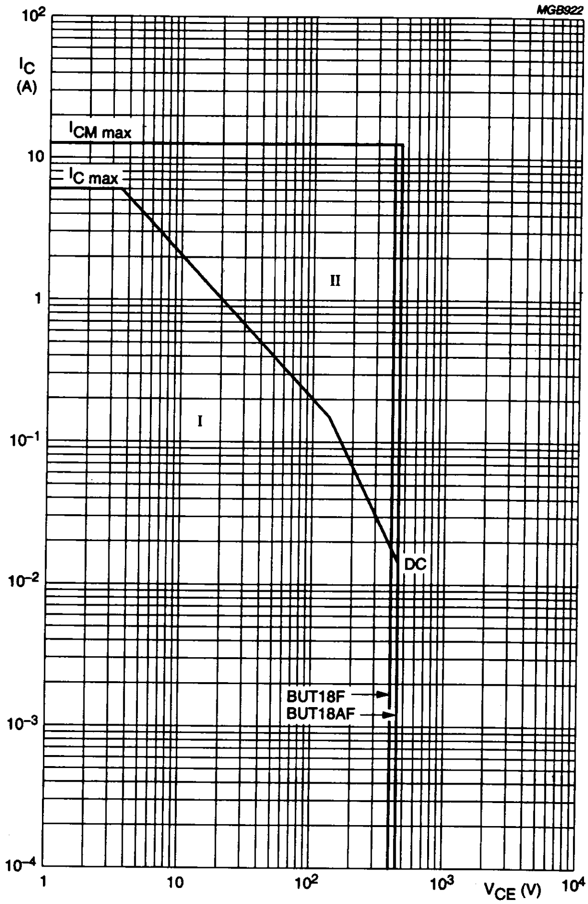


Fig.3 Test circuit for collector-emitter sustaining voltage.



Mounted **without** heatsink compound and 30 ±5 N force on centre of package.

$T_{mb} < 25\ °C$

I - Region of permissible DC operation.

II - Permissible extension for repetitive pulse operation.

Fig.4 Forward bias SOAR.

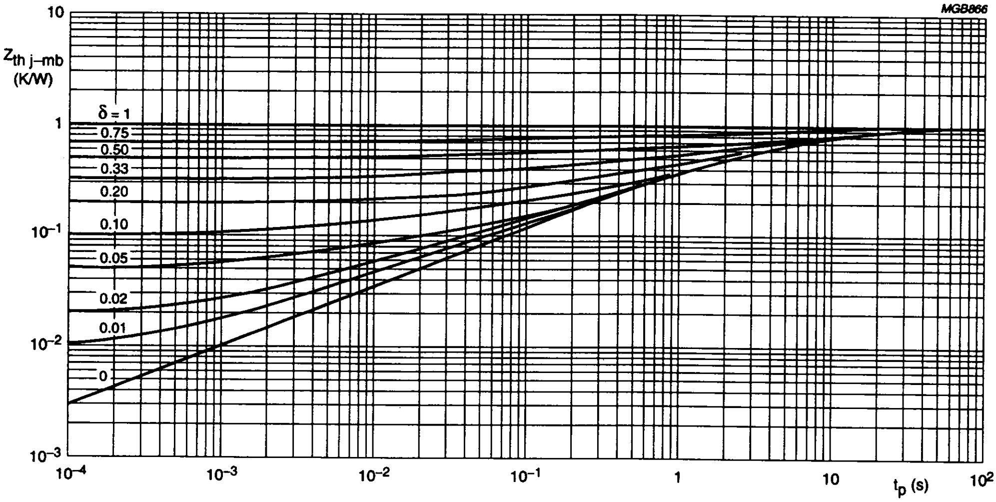


Fig.5 Transient thermal impedance.

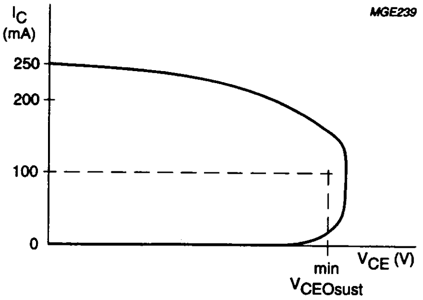
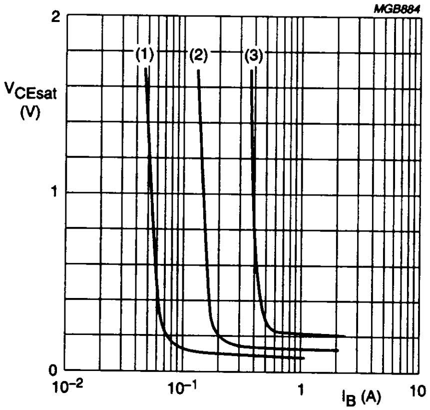
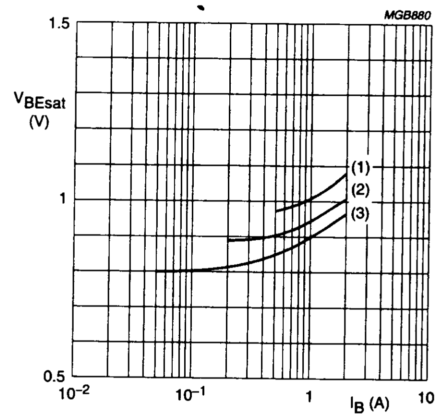


Fig.6 Oscilloscope display for collector-emitter sustaining voltage.



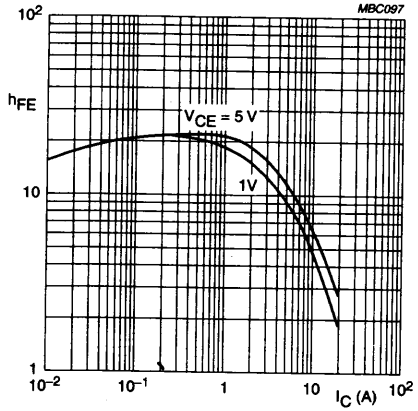
T_j = 25 °C.
(1) I_C = 1 A.
(2) I_C = 2 A.
(3) I_C = 4 A.

Fig.7 Collector-emitter saturation voltage as a function of base current.



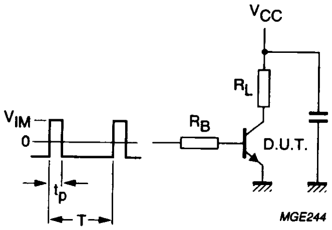
T_j = 25 °C.
(1) I_C = 4 A.
(2) I_C = 2 A.
(3) I_C = 1 A.

Fig.8 Base-emitter saturation voltage as a function of base current.



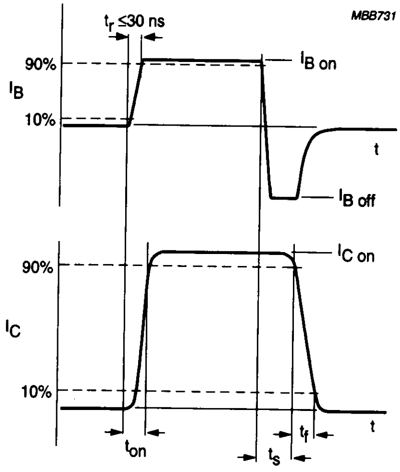
V_{CE} = 5 V; T_j = 25 °C.

Fig.9 DC current gain; typical values.



V_{CC} = 250 V; t_p = 20 µs; V_{IM} = −6 to +8 V; t_p/T = 0.01.
The values of R_B and R_L are selected in accordance with I_{Con} and I_{Bon} requirements.

Fig.10 Test circuit resistive load.



t_r ≤ 20 ns.

Fig.11 Switching times waveforms with resistive load.