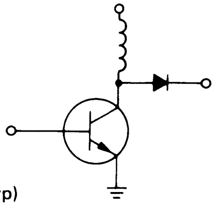
MOTOROLA

BUS 36
BUS 37

SWITCHMODE II▲ SERIES
NPN SILICON POWER TRANSISTORS

The BUS36 and BUS37 transistors are designed for low voltage, high speed, power switching in inductive and resistive circuits where turn-off times are critical. They are particularly suited for battery-operated Switchmode applications and driver applications such as :

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls



Fast Turn-Off Times
60 ns Inductive Fall Time – 25°C (Typ)
110 ns Inductive Crossover Time – 25°C (Typ)

Operating Temperature Range – 65 to + 175°C

100°C Performance Specified for :
Reverse-Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents (125°C)

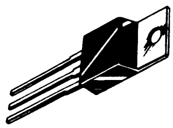
12 AMPERES

NPN SILICON POWER TRANSISTORS

120 & 150 VOLTS
107 WATTS

Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



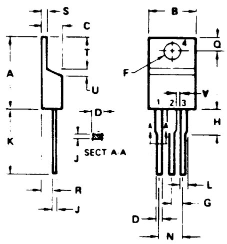
MAXIMUM RATINGS

Rating	Symbol	BUS36	BUS37	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	120	150	Vdc
Collector-Emitter Voltage	V_{CEV}	250	300	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current – Continuous – Peak(1) – Overload	I_C I_{OL}	12 25 40		Adc
Base Current – Continuous – Peak(1)	I_B I_{BM}	7 15		Adc
Total Power Dissipation – T_C = 25°C – T_C = 100°C Derate above 25°C	P_D	107 53 0.71		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	- 65 to + 175		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≦ 10%.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14		0.045	

CASE 221A-02
TO-220

1-83/DSER1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 50$ mA, $I_B = 0$) L = 25 mH BUS36	$V_{CEO(sus)}$	120	–		Vdc
BUS37		150	–	–	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)} = 1.5$ Vdc)	I_{CEV}	–	–	0.1	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)} = 1.5$ Vdc, $T_C = 125°C$)		–	–	1.0	
Collector Cutoff Current BUS36 : $V_{CE} = 60$ V	I_{CEO}	–	–	0.05	mAdc
BUS37 : $V_{CE} = 75$ V		–	–	0.05	
Emitter Cutoff Current ($V_{EB} = 6$ Vdc, $I_C = 0$)	I_{EBO}			0.1	mAdc
Emitter-base breakdown Voltage ($I_E = 50$ mA - $I_C = 0$)	BV_{EBO}	8.0			Vdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$		See Figure 12		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 13		
ON CHARACTERISTICS (1)					
DC Current Gain ($I_C = 10$ Adc, $V_{CE} = 2$ Vdc)	h_{FE}	30	–	–	–
($I_C = 0.5$ Amp, $V_{CE} = 2$ V)		50	–	–	
Collector-Emitter Saturation Voltage ($I_C = 12$ Amp, $I_B = 1.2$ Amp)	$V_{CE(sat)}$	–	–	0.8	Vdc
($I_C = 12$ Amp, $I_B = 1.2$ Amp, $T_c = 100°C$)		–	–	1.0	
Base-Emitter Saturation Voltage ($I_C = 12$ Amp, $I_B = 1.2$ Amp)	$V_{BE(sat)}$	–	–	1.8	Vdc
($I_C = 12$ Amp, $I_B = 1.2$ Amp, $T_c = 100°C$)		–	–	1.8	
DYNAMIC CHARACTERISTICS					
Output Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0$, $f_{test} = 100$ khz)	C_{ob}	–	–	300	pF
Current Gain — Bandwidth Product (2) ($I_C = 1.0$ Adc, $V_{CE} = 10$ Vdc, $f_{test} = 1.0$ MHz	f_T	30	–	–	MHz

SWITCHING CHARACTERISTICS
Resistive Load (Table 1)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Delay Time	(V_{CC} = 100 Vdc, I_C = 12 A, I_{B1} = 1.2 A, t_p = 30 μs, Duty Cycle ≤ 2%, $V_{BE(off)}$ = 5 V)	t_d	–	0.07	0.15	μs
Rise Time		t_r	–	0.15	0.3	
Storage Time		t_s	–	0.5	1.0	
Fall Time		t_f	–	0.12	0.25	

Inductive Load, Clamped (Table 1)

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Storage Time	($I_{C(pk)}$ = 12 A, I_{B1} = 1.2 A, $V_{BE(off)}$ = 5 V, $V_{CE(c1)}$ = 100 V)	($T_C = 25°C$)	t_{sv}	–	0.5	–	μs
Fall Time			t_{fi}	–	0.06	–	
Storage Time		($T_C = 100°C$)	t_{sv}	–	0.6	1.0	
Fall Time			t_{fi}	–	0.15	0.30	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

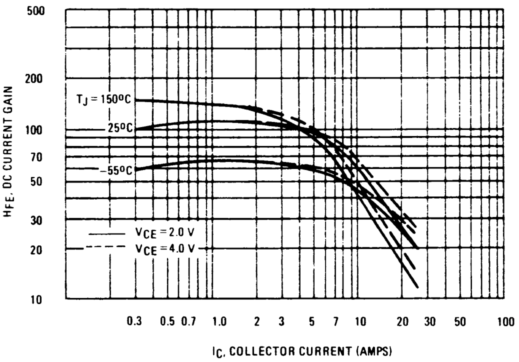


FIGURE 2 – COLLECTOR SATURATION REGION

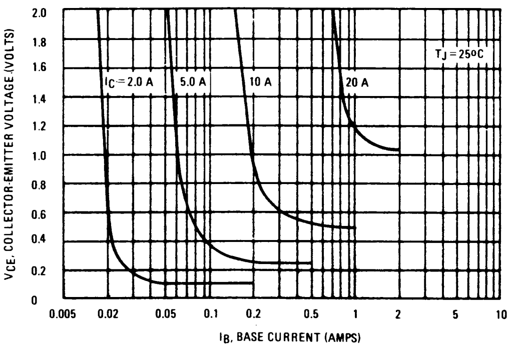


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

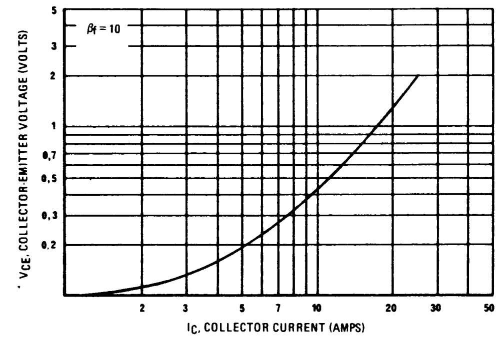


FIGURE 4 – BASE-EMITTER VOLTAGE

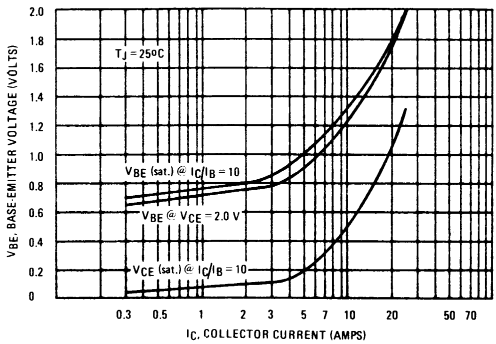


FIGURE 5 – COLLECTOR CUTOFF REGION

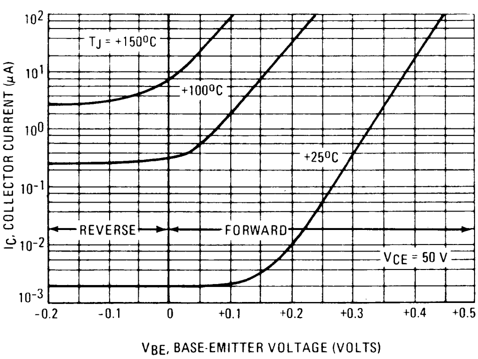


FIGURE 6 – CAPACITANCE

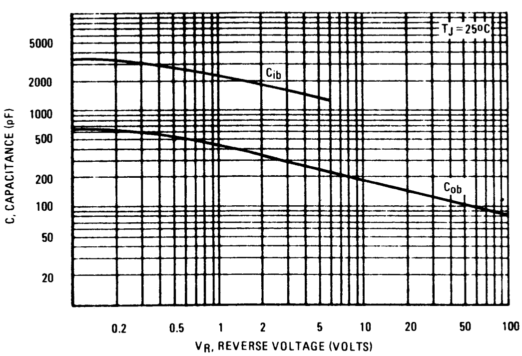


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

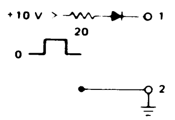
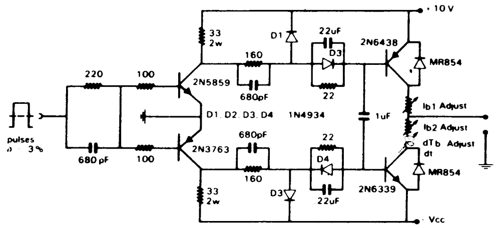
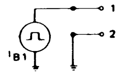
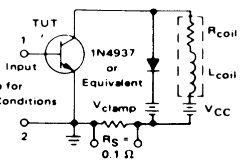
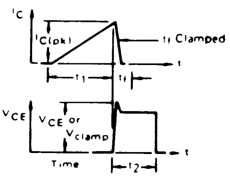
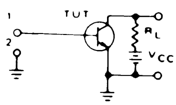
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA		TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 83 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above for Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

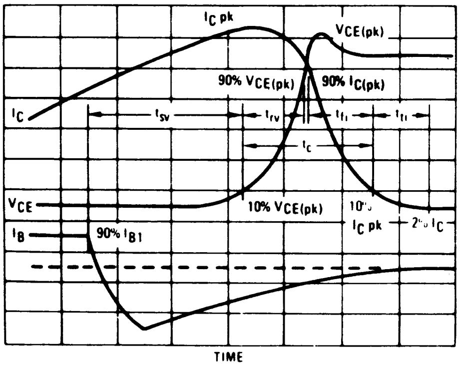
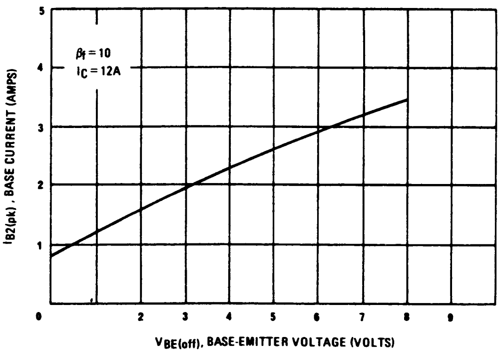


FIGURE 8 — PEAK-REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}

t_{rv} = Voltage Rise Time, 10–90% V_{clamp}

t_{fi} = Current Fall Time, 90–10% I_C

t_{ti} = Current Tail, 10–2% I_C

t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME, Tsv

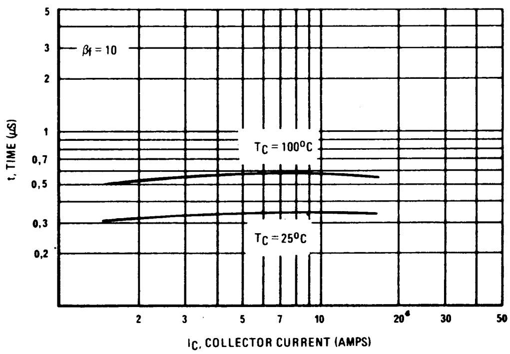


FIGURE 10 — FALL TIMES

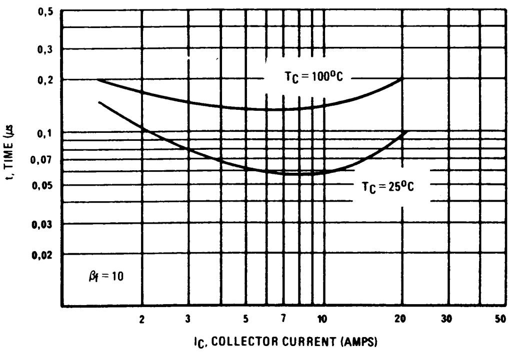


FIGURE 11a — TURN-OFF TIMES vs FORCED GAIN

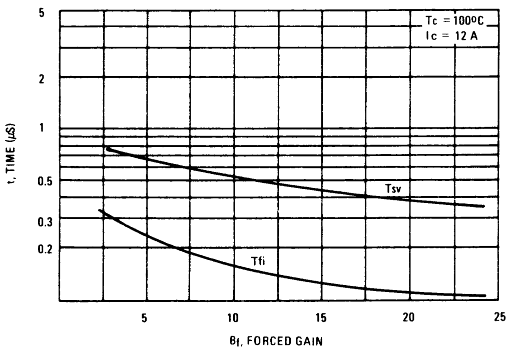
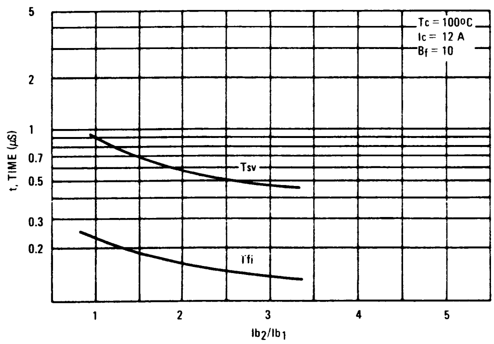


FIGURE 11b — TURN-OFF TIMES vs I_{b2}/I_{b1}



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

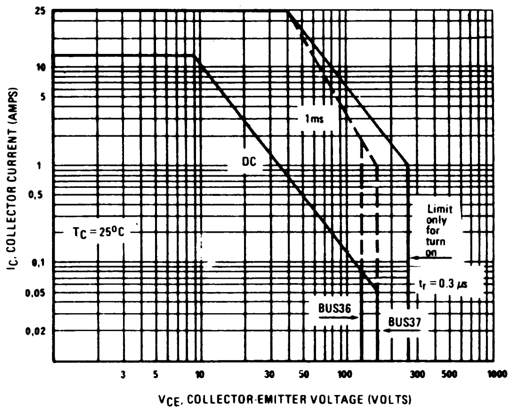


FIGURE 13 – REVERSE BIAS SAFE OPERATING AREA

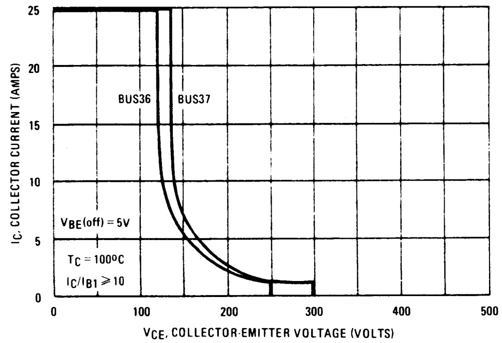
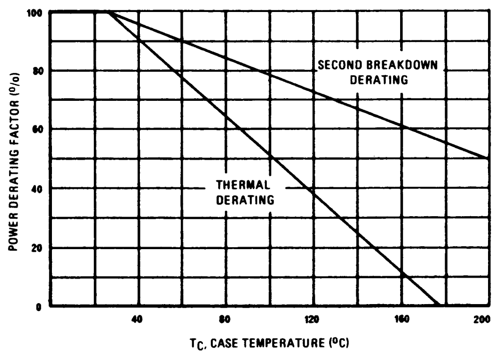


FIGURE 14 – POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

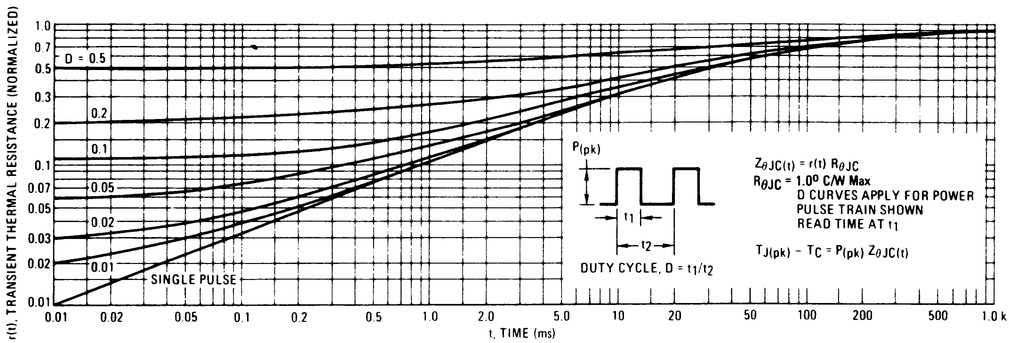
The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

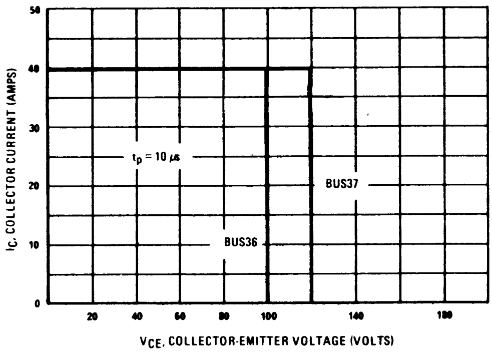
For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

FIGURE 15 — THERMAL RESPONSE



OVERLOAD CHARACTERISTICS

FIGURE 16 — RATED OVERLOAD SAFE OPERATING AREA (OLSOA)



OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

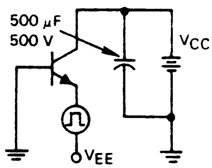
Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 17) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

FIGURE 17 — OVERLOAD SOA TEST CIRCUIT

Notes:

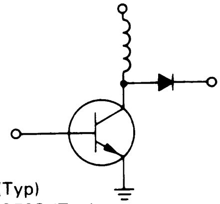
- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p



SWITCHMODE II SERIES
NPN SILICON POWER TRANSISTORS

The BUS 45P transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line-operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times
- 100 ns Inductive Fall Time — 25°C (Typ)
- 150 ns Inductive Crossover Time — 25°C (Typ)
- 400 ns Inductive Storage Time — 25°C (Typ)

Operating Temperature Range −65 to +150°C

100°C Performance Specified for:
- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

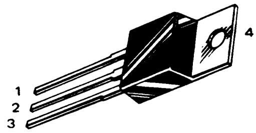
3 AMPERES

NPN SILICON POWER TRANSISTORS

450 VOLTS
75 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



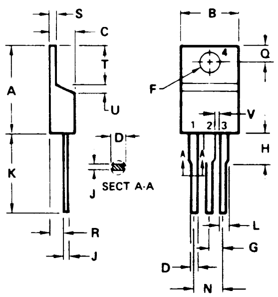
MAXIMUM RATINGS

Rating	Symbol	BUS 45P	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6	Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	3 5	Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	1.5 3	Adc
Total Power Dissipation – T_C = 25°C – T_C = 100°C Derate above 25°C	P_D	75	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	·	0.045	·

CASE 221A-02
TO 220

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

OFF CHARACTERISTICS (1)

Characteristic	Symbol	Min	Typ	Max	Unit
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450	–	–	Vdc
Collector Cutoff Current (V_{CEV} = 850 V, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	–	0.5	mAdc
(V_{CEV} = 850 V, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		–	–	2.5	
Collector Cutoff Current (V_{CE} = 850 V, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	–	–	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	–	1.0	mAdc

ON CHARACTERISTICS (1)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Current Gain (I_C = 2 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	6	–	–	–
Collector-Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.5 Adc)	$V_{CE(sat)}$	–	–	1.0	Vdc
(I_C = 3 Adc, I_B = 0.75 Adc)		–	–	3.0	
(I_C = 2 Adc, I_B = 0.5 Adc, T_C = 100°C)		–	–	2.0	
Base-Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.5 Adc)	$V_{BE(sat)}$	–	–	1.5	Vdc
(I_C = 2 Adc, I_B = 0.5 Adc, T_C = 100°C)		–	–	1.5	

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Delay Time	(V_{CC} = 250 Adc, I_C = 2 A, I_{B1} = 0.5 Adc, t_p = 30 μs, Duty Cycle ≦ 2%, $V_{BE(off)}$ = 5.0 Vdc)	t_d	–	0.03	0.05	μs
Rise Time		t_r	–	0.10	0.40	
Storage Time		t_s	–	0.40	1.50	
Fall Time		t_f	–	0.175	0.50	

Inductive Load, Clamped (Table 1)

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Storage Time	($I_{C(pk)}$ = 2 A, I_{B1} = 0.5 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 250 V)	(T_J = 100°C)	t_{sv}	–	0.70	2.0	μs
Crossover Time			t_c	–	0.28	0.50	
Fall Time			t_{fi}	–	0.15	0.35	
Storage Time		(T_J = 25°C)	t_{sv}	–	0.40	–	
Crossover Time			t_c	–	0.15	–	
Fall Time			t_{fi}	–	0.10	–	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≦ 2%.

$$\beta_f = \frac{I_C}{I_B}$$

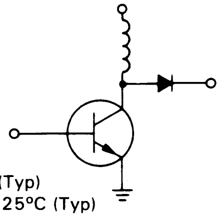
MOTOROLA

BUS 46P

SWITCHMODE II SERIES
NPN SILICON POWER TRANSISTORS

The BUS 46P transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line-operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times
 100 ns Inductive Fall Time—25°C (Typ)
 150 ns Inductive Crossover Time—25°C (Typ)
 400 ns Inductive Storage Time—25°C (Typ)

Operating Temperature Range −65 to +150°C

100°C Performance Specified for:
 Reverse-Biased SOA with Inductive Loads
 Switching Times with Inductive Loads
 Saturation Voltages
 Leakage Currents

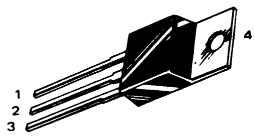
5 AMPERES

NPN SILICON POWER TRANSISTORS

450 VOLTS
80 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



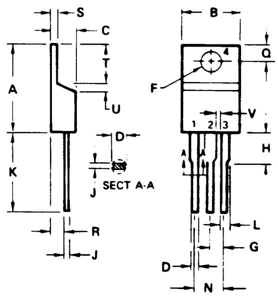
MAXIMUM RATINGS

Rating	Symbol	BUS 46P	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6	Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	5 8	Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	2 4	Adc
Total Power Dissipation – T_C = 25°C – T_C = 100°C Derate above 25°C	P_D	80	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

CASE 221A-02
TO 220

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450	–	–	Vdc
Collector Cutoff Current (V_{CEV} = 850 V, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	–	0.5	mAdc
(V_{CEV} = 850 V, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		–	–	2.5	
Collector Cutoff Current (V_{CE} = 850 V, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	–	–	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	–	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$		See Figure 12		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 13		
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	7.0	–	–	–
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc)	$V_{CE(sat)}$	–	–	1.0	Vdc
(I_C = 5.0 Adc, I_B = 1.0 Adc)		–	–	3.0	
(I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C)		–	–	2.0	
Base-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc)	$V_{BE(sat)}$	–	–	1.5	Vdc
(I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C)		–	–	1.5	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 Khz)	C_{ob}	–	–	250	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Delay Time	(V_{CC} = 250 Adc, I_C = 3.0 Adc, I_{B1} = 0.4 Adc, t_p = 30 μs, Duty Cycle ≦ 2%, $V_{BE(off)}$ = 5.0 Vdc)	t_d	–	0.03	0.05	μs
Rise Time		t_r	–	0.10	0.40	
Storage Time		t_s	–	0.40	1.50	
Fall Time		t_f	–	0.175	0.50	

Inductive Load, Clamped (Table 1)

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Storage Time	($I_{C(pk)}$ = 3.0 A, I_{B1} = 0.4 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 250 V)	(T_J = 100°C)	t_{sv}	–	0.70	2.0	μs
Crossover Time			t_c	–	0.28	0.50	
Fall Time			t_{fi}	–	0.15	0.30	
Storage Time		(T_J = 25°C)	t_{sv}	–	0.40	–	
Crossover Time			t_c	–	0.15	–	
Fall Time			t_{fi}	–	0.10	–	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≦ 2%.

$$\beta_f = \frac{I_C}{I_B}$$

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

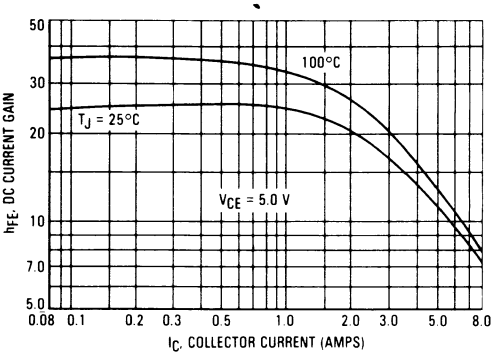


FIGURE 2 — COLLECTOR SATURATION REGION

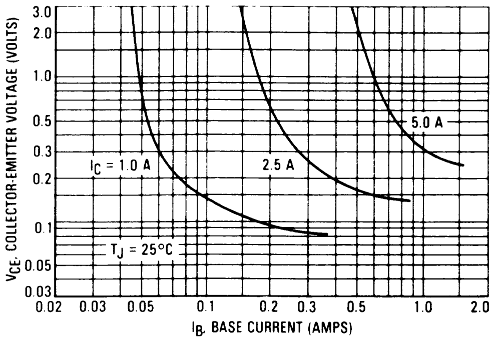


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

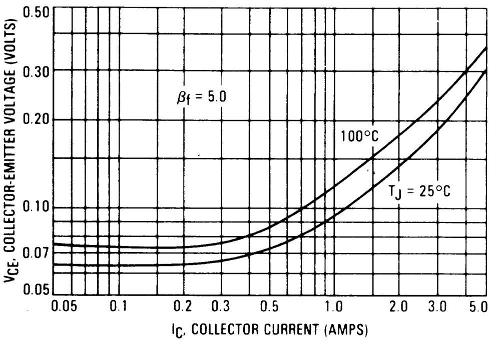


FIGURE 4 — BASE-EMITTER VOLTAGE

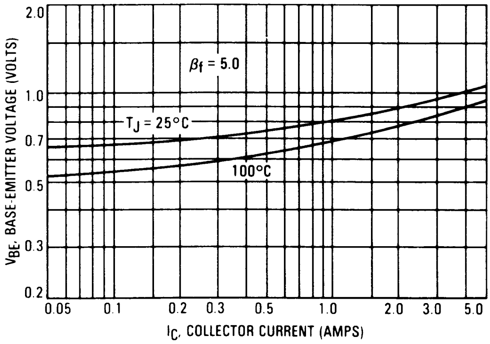


FIGURE 5 — COLLECTOR CUTOFF REGION

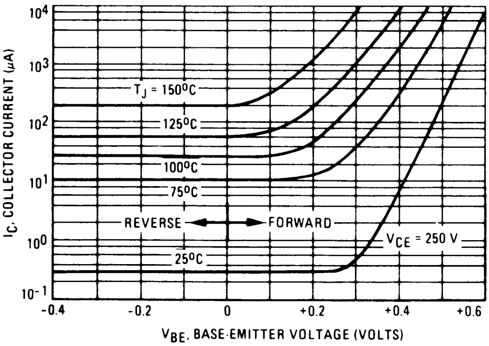


FIGURE 6 — CAPACITANCE

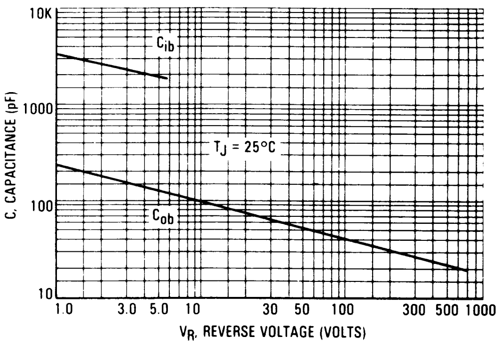


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

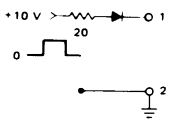
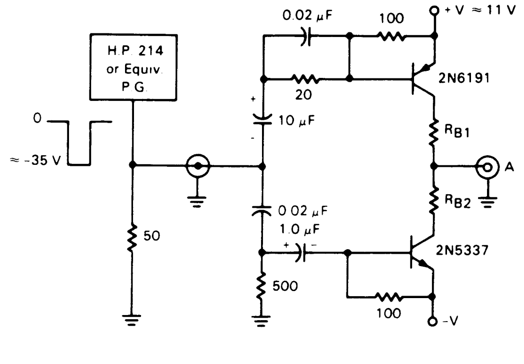
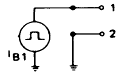
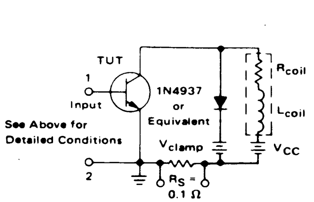
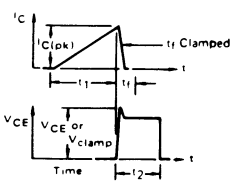
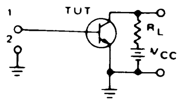
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $BV_{CEO(sus)}$, R2 = ∞	TURN-ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN-OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 83 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above for Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

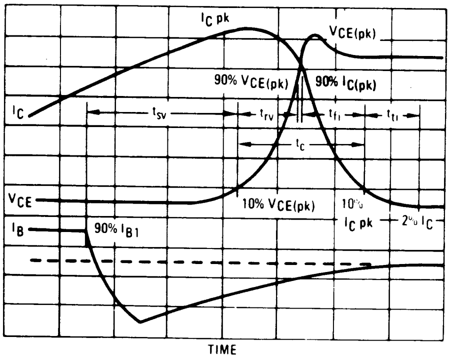
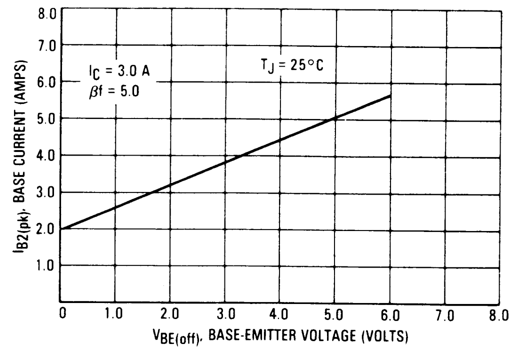


FIGURE 8 — PEAK REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME

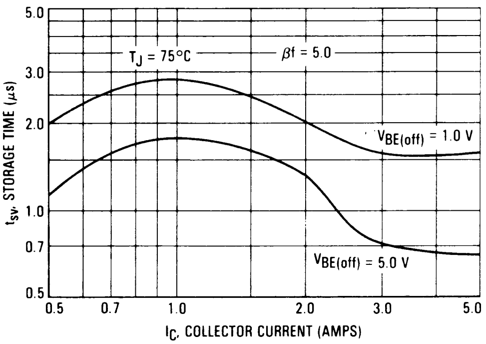


FIGURE 10 — CROSSOVER AND FALL TIMES

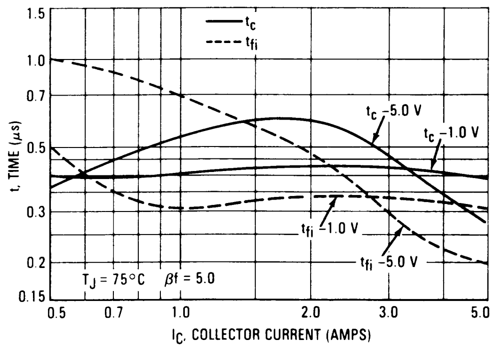
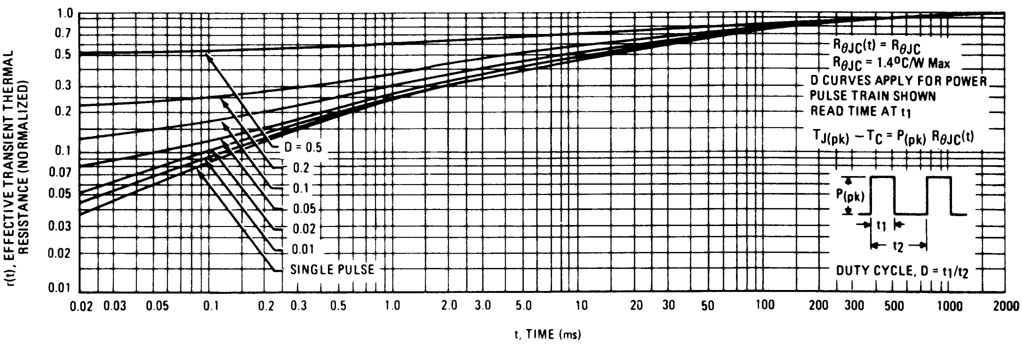


FIGURE 11 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

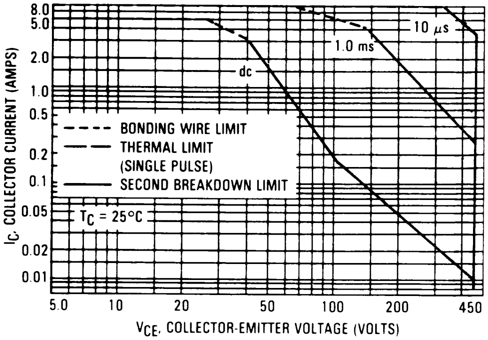


FIGURE 13 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA

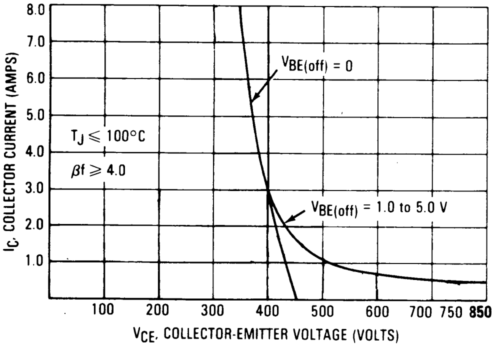
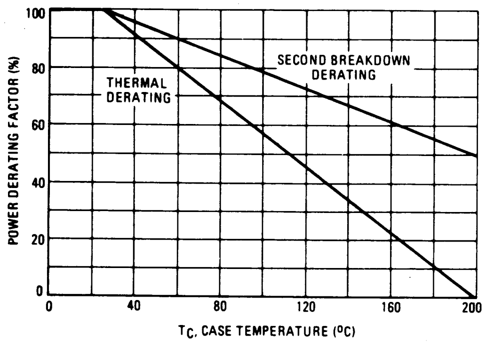


FIGURE 14 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq$ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

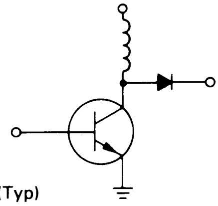
MOTOROLA

BUS 47
BUS 47A

SWITCHMODE II▲ SERIES
NPN SILICON POWER TRANSISTORS

The BUS 47 and BUS 47A transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



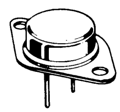
Fast Turn-Off Times
60 ns Inductive Fall Time—25°C (Typ)
120 ns Inductive Crossover Time—25°C (Typ)

Operating Temperature Range −65 to +200°C
100°C Performance Specified for:
Reverse-Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents (125°C)

9 AMPERES
NPN SILICON POWER TRANSISTORS
400 AND 450 VOLTS (BVCEO)
150 WATTS
850 – 1000 V (BVCES)

Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



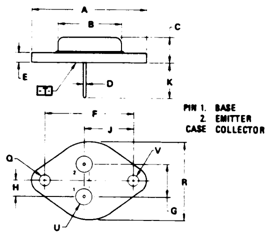
MAXIMUM RATINGS

Rating	Symbol	BUS 47	BUS 47A	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	1000	Vdc
Emitter Base Voltage	V_{EB}	7		Vdc
Collector Current – Continuous – Peak (1) – Overload	I_C I_{CM} I_{OI}	9 18 36		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	5 10		Adc
Total Power Dissipation – T_C = 25°C – T_C = 100°C Derate above 25°C	P_D	150 85.5 0.86		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
⊕ | ∅ 0.13 (0.005) Ⓜ | T | V Ⓜ
FOR LEADS:
⊕ | ∅ 0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3 TYPE

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 200$ mA, $I_B = 0$) L = 25 mH	BUS47 BUS47A	$V_{CEO(sus)}$	400 450	–	–	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)} = 1.5$ Vdc) (V_{CEV} = Rated Value, $V_{BE(off)} = 1.5$ Vdc, $T_C = 125°C$)		I_{CEV}	– –	– –	0.15 1.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, $R_{BE} = 10\ \Omega$)	$T_C = 25°C$ $T_C = 125°C$	I_{CER}	–	–	0.4 3.0	mAdc
Emitter Cutoff Current ($V_{EB} = 5$ Vdc, $I_C = 0$)		I_{EBO}	–	–	0.1	mAdc
Emitter-base breakdown Voltage ($I_E = 50$ mA - $I_C = 0$)		B_{VEBO}	7.0	–	–	Vdc

SECOND BREAKDOWN

Characteristic	Symbol		Unit
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 12	
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13	

ON CHARACTERISTICS (1)

Characteristic		Symbol	Min	Typ	Max	Unit
DC Current Gain ($I_C = 6$ Adc, $V_{CE} = 5$ Vdc) ($I_C = 5$ Adc, $V_{CE} = 5$ V)	BUS47 BUS47A	h_{FE}	7	–	–	
Collector-Emitter Saturation Voltage ($I_C = 6$ Adc, $I_B = 1.2$ Adc) ($I_C = 9$ Adc, $I_B = 1.8$ Adc) ($I_C = 6$ Adc, $I_B = 1.2$ Adc, $T_C = 100°C$) ($I_C = 5$ Adc, $I_B = 1$ Adc) ($I_C = 8$ Adc, $I_B = 1.6$ Adc) ($I_C = 5$ Adc, $I_B = 1$ Adc, $T_C = 100°C$)	BUS47 BUS47A	$V_{CE(sat)}$	– – – – – –	– – – – – –	1.5 5.0 2.5 1.5 5.0 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 6$ Adc, $I_B = 1.2$ Adc) ($I_C = 6$ Adc, $I_B = 1.2$ Adc, $T_C = 100°C$) ($I_C = 5$ Adc, $I_B = 1$ Adc) ($I_C = 5$ Adc, $I_B = 1$ Adc, $T_C = 100°C$)	BUS47 BUS47A	$V_{BE(sat)}$	– – – –	– – – –	1.6 1.6 1.6 1.6	Vdc

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Output Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0$, $f_{test} = 100$ Khz)	C_{ob}	–	–	300	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Delay Time	($V_{CC} = 250$ Vdc, $I_C = 6$ A, $I_{B1} = 1.2$ A, $t_p = 30\ \mu s$, Duty Cycle 2 , $V_{BE(off)} = 5$ V)	t_d	–	0.05	0.2	μs
Rise Time		t_r	–	0.5	0.8	
Storage Time		t_s	–	1	2.0	
Fall Time		t_f	–	0.2	0.4	

Inductive Load, Clamped (Table 1)

Characteristic	Conditions	Device	Temperature	Symbol	Min	Typ	Max	Unit
Storage Time	($I_{C(pk)} = 6$ A, $I_{B1} = 1.2$ A, $V_{BE(off)} = 5$ V, $V_{CE(c1)} = 250$ V) $I_{C(pk)} = 5$ A $I_{B1} = 1$ A	BUS47	($T_C = 25°C$)	t_{sv}	–	0.9	–	μs
Fall Time				t_{fi}	–	0.06	–	
Storage Time		BUS47A	($T_C = 100°C$)	t_{sv}	–	1.0	2.5	
Crossover Time				t_c	–	0.2	0.5	
Fall Time				t_{fi}	–	0.1	0.3	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≦ 2%.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

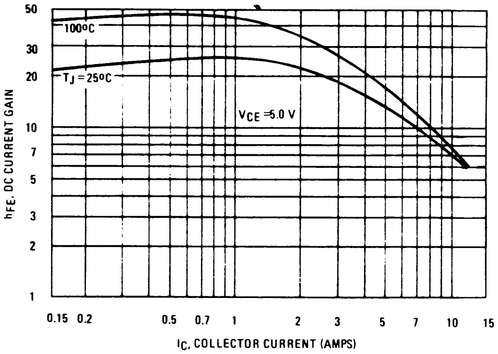


FIGURE 2 – COLLECTOR SATURATION REGION

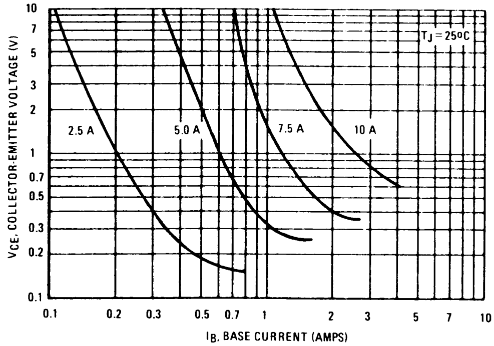


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

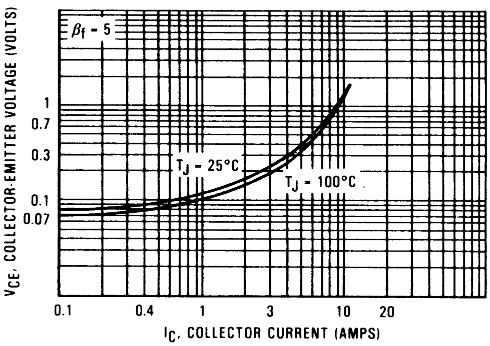


FIGURE 4 – BASE-EMITTER VOLTAGE

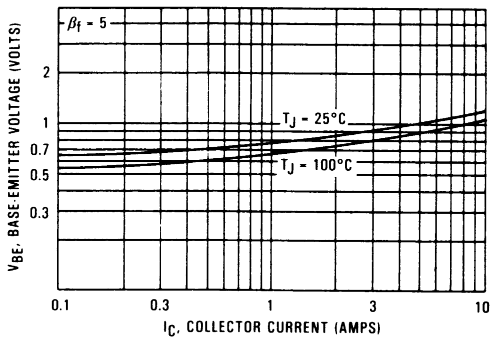


FIGURE 5 – COLLECTOR CUTOFF REGION

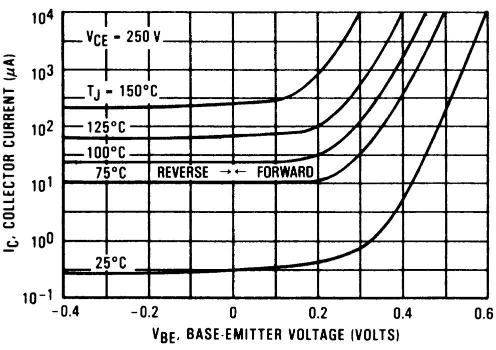


FIGURE 6 – CAPACITANCE

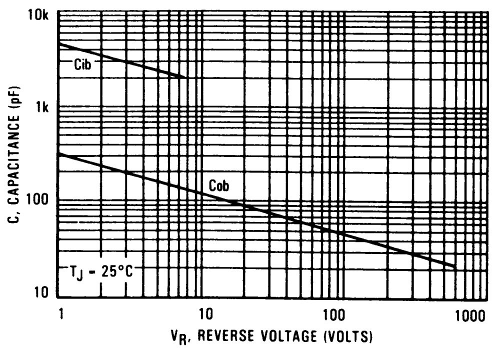


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

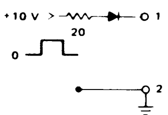
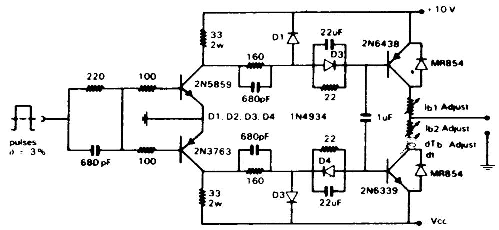
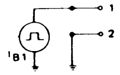
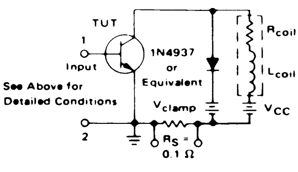
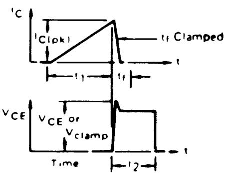
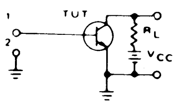
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA		TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 83 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above for Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

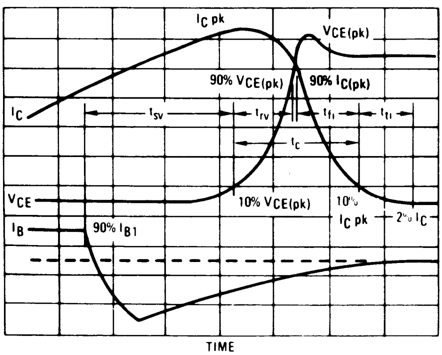
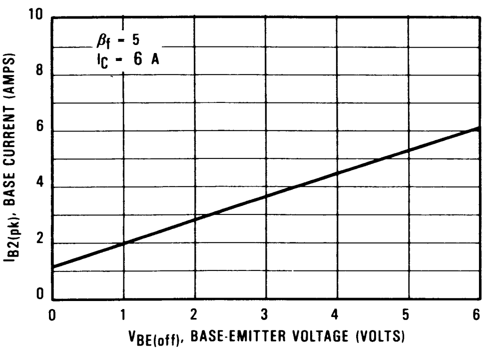


FIGURE 8 – PEAK-REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 – STORAGE TIME

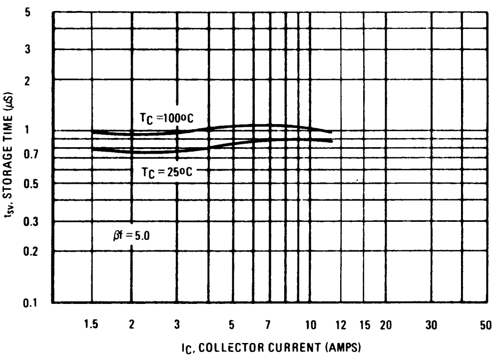


FIGURE 10 – CROSSOVER AND FALL TIMES

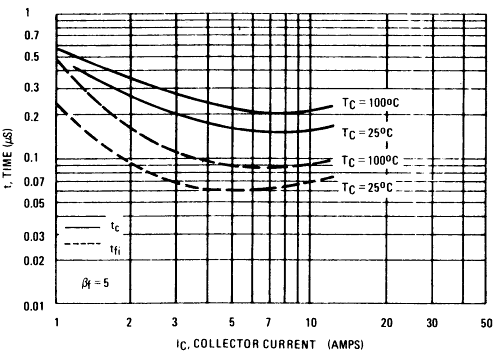


FIGURE 11a – TURN-OFF TIMES vs FORCED GAIN

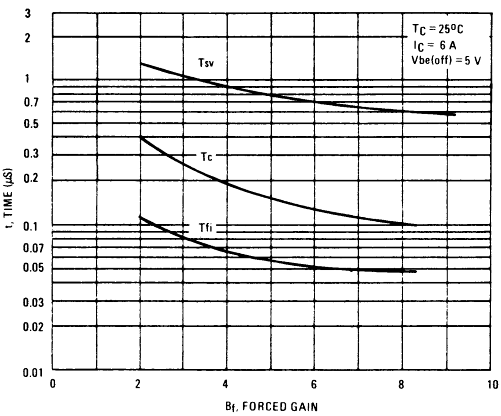
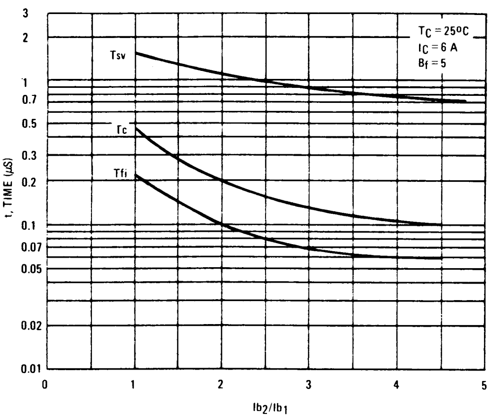


FIGURE 11b – TURN-OFF TIMES vs I_{b2}/I_{b1}



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

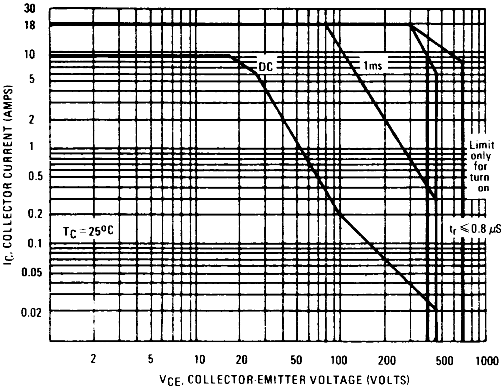


FIGURE 13 – REVERSE BIAS SAFE OPERATING AREA

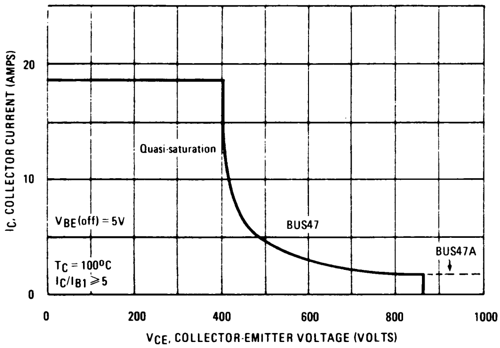
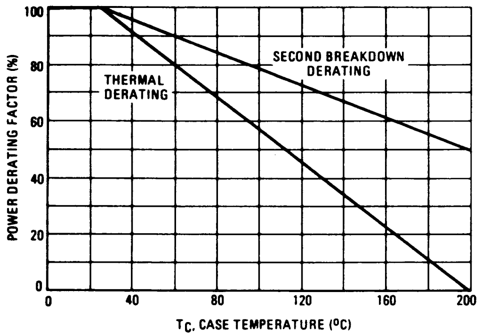


FIGURE 14 – POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

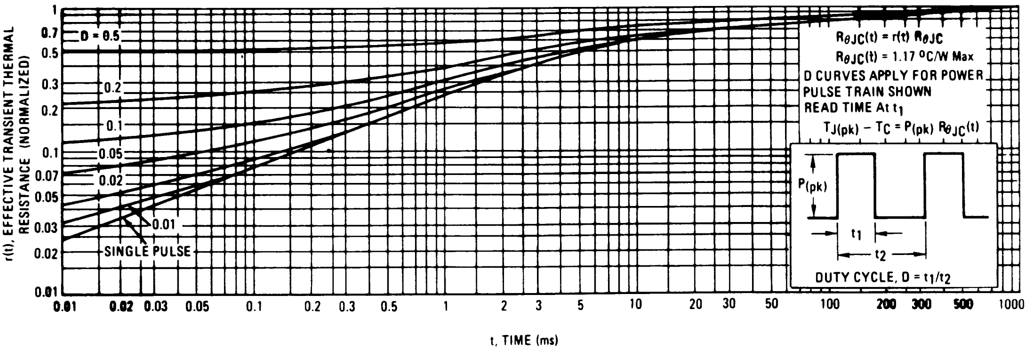
The data of Figure 12 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

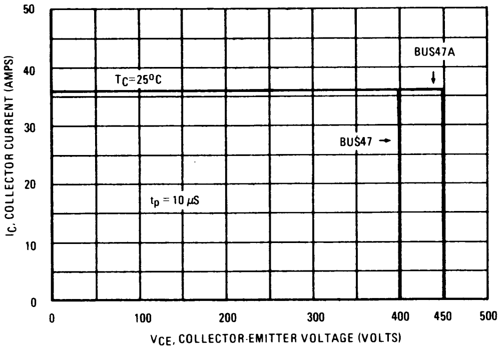
For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

FIGURE 15 – THERMAL RESPONSE



OVERLOAD CHARACTERISTICS

FIGURE 16 – RATED OVERLOAD SAFE OPERATING AREA (OLSOA)



OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

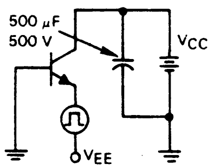
Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 17) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

FIGURE 17 -- OVERLOAD SOA TEST CIRCUIT

Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p

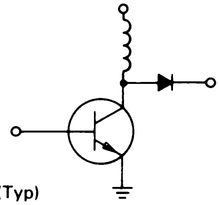


MOTOROLA

BUS 47P
BUS 47AP

SWITCHMODE II▲ SERIES
NPN SILICON POWER TRANSISTORS

The BUS 47P/BUS 47AP transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:

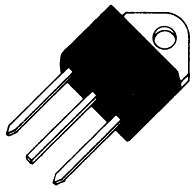


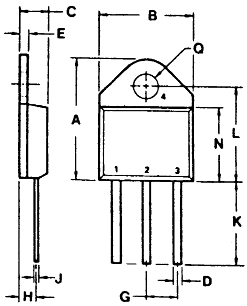
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times
60 ns Inductive Fall Time — 25°C (Typ)
120 ns Inductive Crossover Time — 25°C (Typ)

Operating Temperature Range −65 to +175°C
100°C Performance Specified for:
Reverse-Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents (125°C)

9 AMPERES
NPN SILICON POWER TRANSISTORS
400 AND 450 VOLTS (BV_{CEO})
128 WATTS
850 – 1000 V (BV_{CES})





STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	3.94	4.19	0.155	0.165

CASE 340-01
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	BUS 47P	BUS 47AP	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	1000	Vdc
Emitter Base Voltage	V_{EB}	7		Vdc
Collector Current — Continuous — Peak (1) — Overload	I_C I_{CM}	9 18 36		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	5 10		Adc
Total Power Dissipation — T_C = 25°C — T_C = 100°C Derate above 25°C	P_D	128 64.5 0.86		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +175		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

1-83/DSE R1

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 200$ mA, $I_B = 0$) L = 25 mH	BUS47P BUS47AP	$V_{CEO(sus)}$	400 450	–	–	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)} = 1.5$ Vdc) (V_{CEV} = Rated Value, $V_{BE(off)} = 1.5$ Vdc, $T_C = 125°C$)		I_{CEV}	– –	– –	0.15 1.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, $R_{BE} = 10\ \Omega$)	$T_C = 25°C$ $T_C = 125°C$	I_{CER}	–	–	0.4 3.0	mAdc
Emitter Cutoff Current ($V_{EB} = 5$ Vdc, $I_C = 0$)		I_{EBO}	–	–	0.1	mAdc
Emitter-base breakdown Voltage ($I_E = 50$ mA - $I_C = 0$)		B_{VEBO}	7.0	–	–	Vdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain ($I_C = 6$ Adc, $V_{CE} = 5$ Vdc) ($I_C = 5$ Adc, $V_{CE} = 5$ V)	BUS47P BUS47AP	h_{FE}	7	–	–	
Collector-Emitter Saturation Voltage ($I_C = 6$ Adc, $I_B = 1.2$ Adc) ($I_C = 9$ Adc, $I_B = 1.8$ Adc) ($I_C = 6$ Adc, $I_B = 1.2$ Adc, $T_C = 100°C$)	BUS47P	$V_{CE(sat)}$	– – –	– – –	1.5 5.0 2.5	Vdc
($I_C = 5$ Adc, $I_B = 1$ Adc) ($I_C = 8$ Adc, $I_B = 1.6$ Adc) ($I_C = 5$ Adc, $I_B = 1$ Adc, $T_C = 100°C$)	BUS47AP		– – –	– – –	1.5 5.0 2.5	
Base-Emitter Saturation Voltage ($I_C = 6$ Adc, $I_B = 1.2$ Adc) ($I_C = 6$ Adc, $I_B = 1.2$ Adc, $T_C = 100°C$)	BUS47P	$V_{BE(sat)}$	– –	– –	1.6 1.6	Vdc
($I_C = 5$ Adc, $I_B = 1$ Adc) ($I_C = 5$ Adc, $I_B = 1$ Adc, $T_C = 100°C$)	BUS47AP		– –	– –	1.6 1.6	
DYNAMIC CHARACTERISTICS						
Output Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0$, $f_{test} = 100$ Khz)		C_{ob}	–	–	300	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Delay Time	($V_{CC} = 250$ Vdc, $I_C = 6$ A, $I_{B1} = 1.2$ A, $t_p = 30\ \mu s$, Duty Cycle ≤ 2%, $V_{BE(off)} = 5$ V)	t_d	–	0.05	0.2	µs
Rise Time		t_r	–	0.5	0.8	
Storage Time		t_s	–	1	2.0	
Fall Time		t_f	–	0.2	0.4	

Inductive Load, Clamped (Table 1)

Characteristic	Conditions	Device	Temperature	Symbol	Min	Typ	Max	Unit
Storage Time	($I_{C(pk)} = 6$ A, $I_{B1} = 1.2$ A, $V_{BE(off)} = 5$ V, $V_{CE(c1)} = 250$ V)	BUS47P	($T_C = 25°C$)	t_{sv}	–	0.9	–	µs
Fall Time				t_{fi}	–	0.06	–	
Storage Time	$I_{C(pk)} = 5$ A, $I_{B1} = 1$ A	BUS47AP	($T_C = 100°C$)	t_{sv}	–	1.0	2.5	
Crossover Time				t_c	–	0.2	0.5	
Fall Time				t_{fi}	–	0.1	0.3	

(1) Pulse Test: PW = 300 µs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

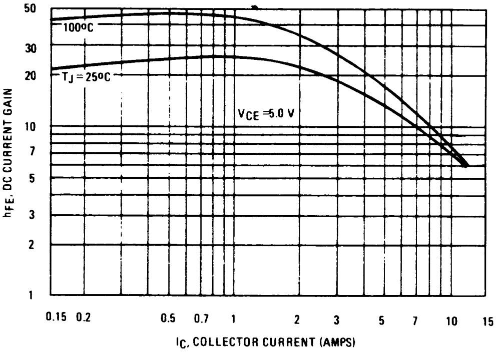


FIGURE 2 – COLLECTOR SATURATION REGION

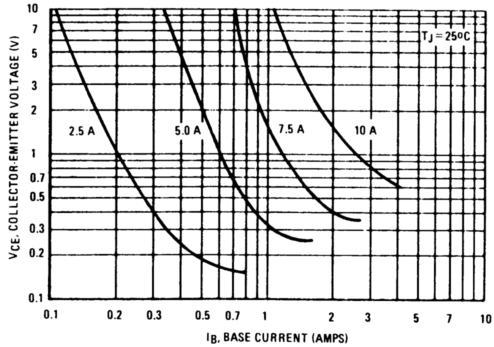


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

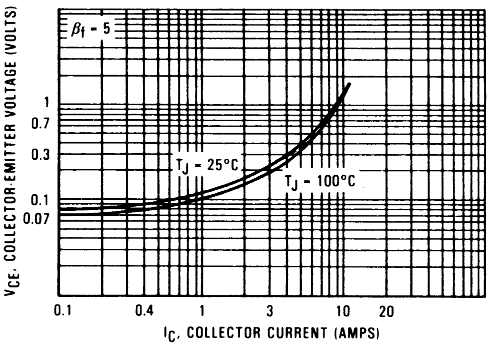


FIGURE 4 – BASE-EMITTER VOLTAGE

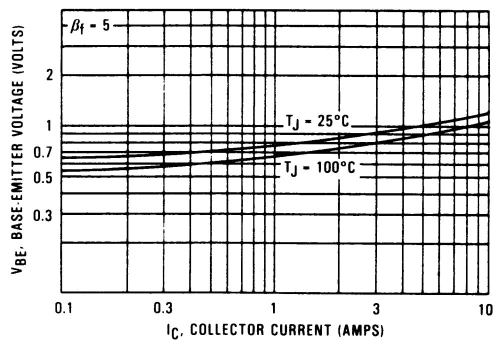


FIGURE 5 – COLLECTOR CUTOFF REGION

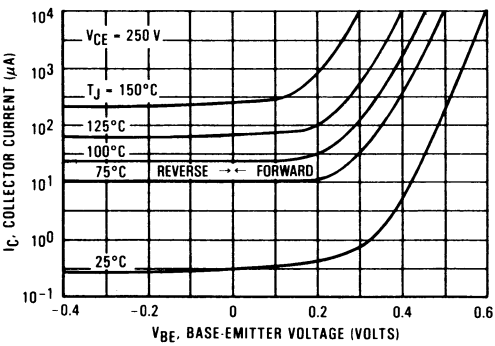


FIGURE 6 – CAPACITANCE

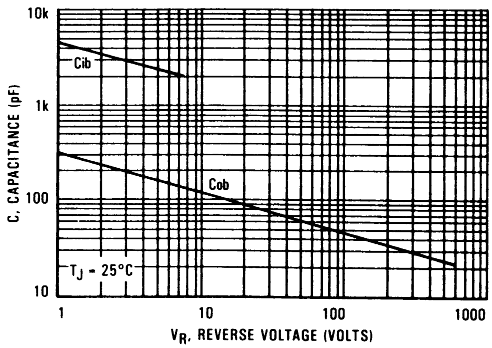


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

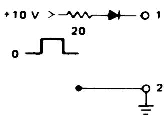
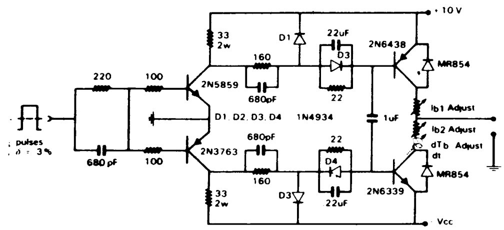
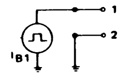
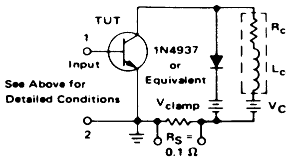
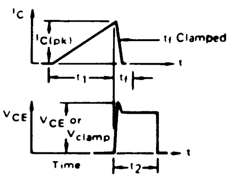
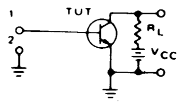
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA		TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 83 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

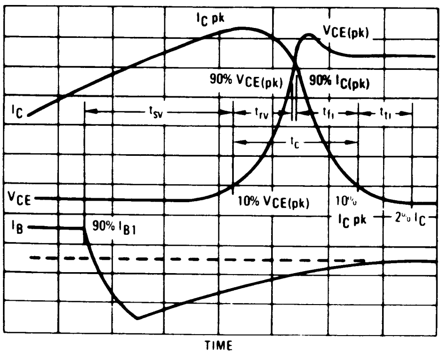
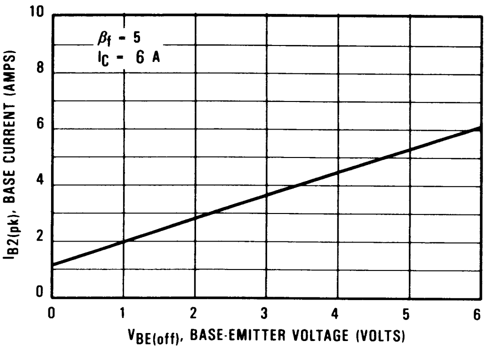


FIGURE 8 – PEAK-REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 – STORAGE TIME

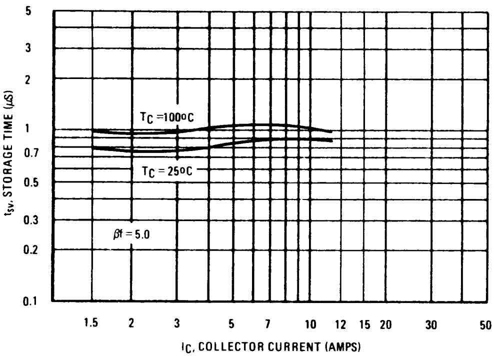


FIGURE 10 – CROSSOVER AND FALL TIMES

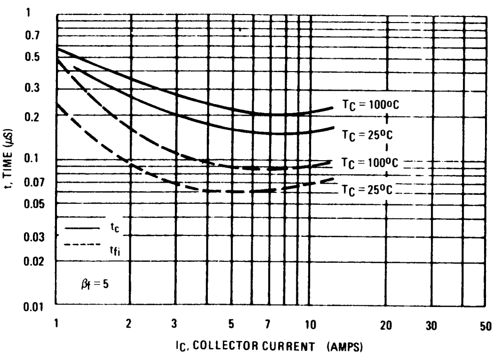


FIGURE 11a – TURN-OFF TIMES vs FORCED GAIN

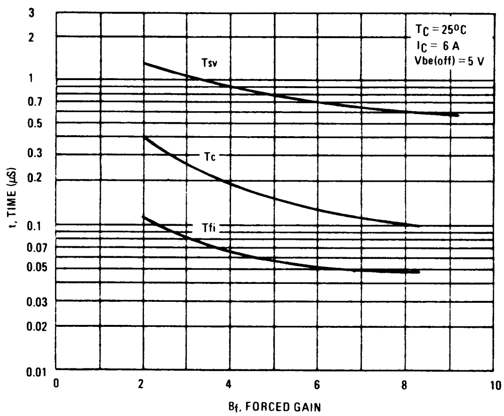
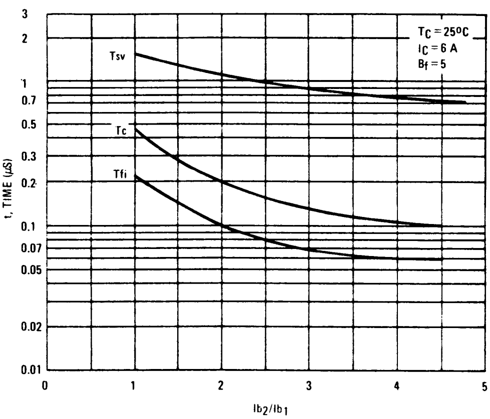


FIGURE 11b – TURN-OFF TIMES vs Ib2/Ib1



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

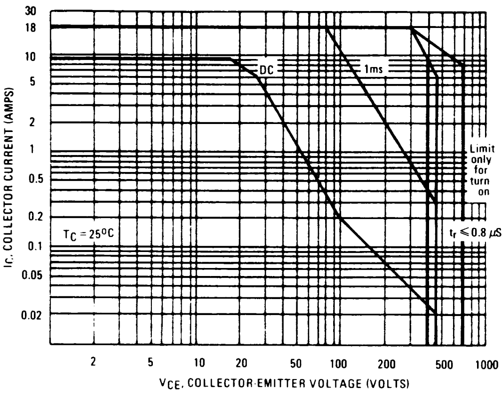


FIGURE 13 – REVERSE BIAS SAFE OPERATING AREA

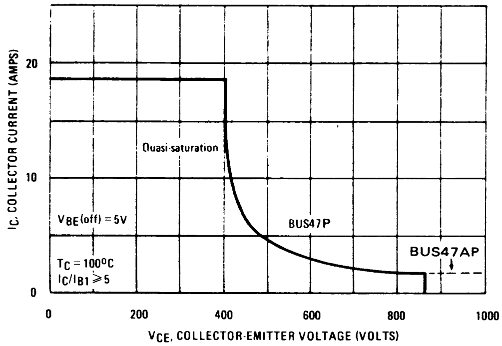
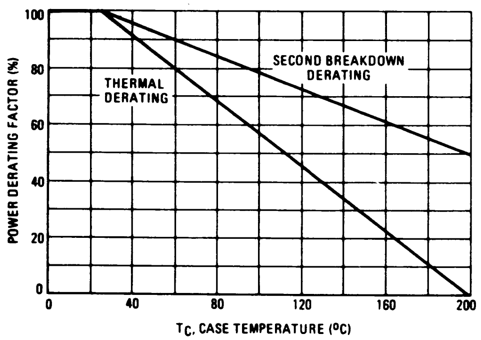


FIGURE 14 – POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

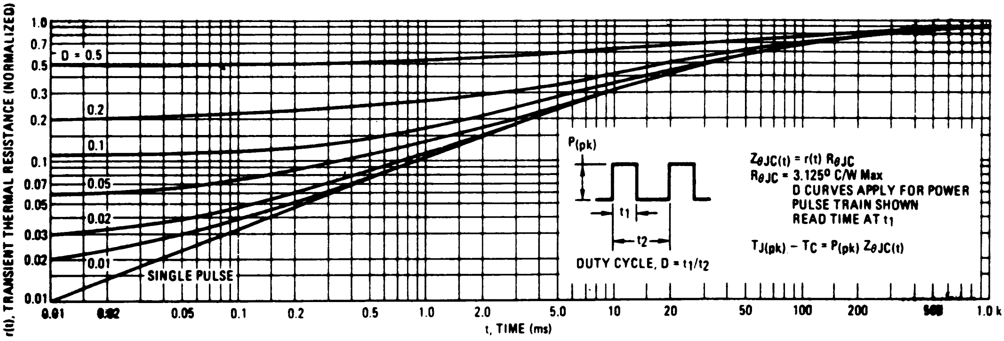
The data of Figure 12 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

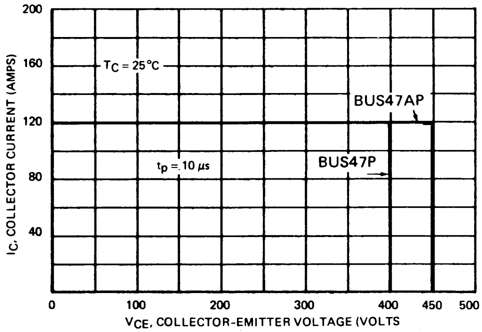
For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

FIGURE 15 – THERMAL RESPONSE



OVERLOAD CHARACTERISTICS

FIGURE 16 – RATED OVERLOAD SAFE OPERATING AREA (OLSOA)



OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

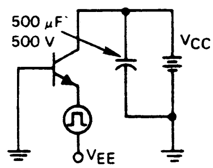
Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 17) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

FIGURE 17 – OVERLOAD SOA TEST CIRCUIT

Notes:

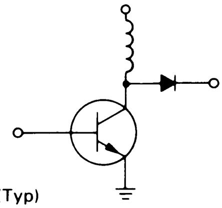
- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p



BUS 48
BUS 48A

SWITCHMODE II▲ SERIES
NPN SILICON POWER TRANSISTORS

The BUS 48 and BUS 48A transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:



- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

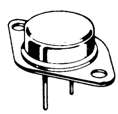
Fast Turn-Off Times
60 ns Inductive Fall Time — 25°C (Typ)
120 ns Inductive Crossover Time — 25°C (Typ)

Operating Temperature Range −65 to +200°C
100°C Performance Specified for:
Reverse-Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents (125°C)

15 AMPERES
NPN SILICON
POWER TRANSISTORS
400 and 450 VOLTS (BVCEO)
850 — 1000 VOLTS (BVCES)
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



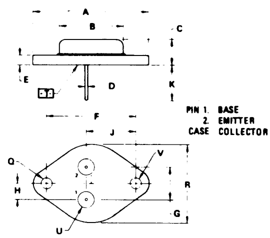
MAXIMUM RATINGS

Rating	Symbol	BUS 48	BUS 48A	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	1000	Vdc
Emitter Base Voltage	V_{EB}	7		Vdc
Collector Current — Continuous — Peak(1) — Overload	I_C I_{CM} I_{OL}	15 30 60		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	5 20		Adc
Total Power Dissipation — T_C = 25°C — T_C = 100°C Derate above 25°C	P_D	175 100 1.0		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES
1. DIMENSIONS Q AND V ARE DATUMS.
2. [T] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
| ⌖ | ∅ 0.13 (0.005) Ⓜ | T | V Ⓜ |

FOR LEADS:
| ⌖ | ∅ 0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 200 mA, I_B = 0) L = 25 mH — BUS48 BUS48A	$V_{CEO(sus)}$	400 450	–	–	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	I_{CEV}	– –	– –	0.2 2.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 10 Ω) — T_C = 25°C T_C = 125°C	I_{CER}	–	–	0.5 3.0	mAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	–	–	0.1	mAdc
Emitter-base breakdown Voltage (I_E = 50 mA - I_C = 0)	BV_{EBO}	7.0	–	–	Vdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 5 Vdc) — BUS48 (I_C = 8 Adc, V_{CE} = 5 V) — BUS48A	h_{FE}	8	–	–	
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2 Adc) (I_C = 15 Adc, I_B = 3 Adc) — BUS48 (I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C) (I_C = 8 Adc, I_B = 1.6 Adc) (I_C = 12 Adc, I_B = 2.4 Adc) — BUS48A (I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)	$V_{CE(sat)}$	– – – – – –	– – – – – –	1.5 5.0 2.0 1.5 5.0 2.0	Vdc
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2 Adc) — BUS48 (I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C) (I_C = 8 Adc, I_B = 1.6 Adc) — BUS48A (I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)	$V_{BE(sat)}$	– – – –	– – – –	1.6 1.6 1.6 1.6	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 Khz)	C_{ob}	–	–	350	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Delay Time	(V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 2.0 A, t_p = 30 μs, Duty Cycle ⩽ 2%, $V_{BE(off)}$ = 5 V)	t_d	–	0.1	0.2	μs
Rise Time		t_r	–	0.4	0.7	
Storage Time		t_s	–	1.3	2.0	
Fall Time		t_f	–	0.2	0.4	

Inductive Load, Clamped (Table 1)

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Storage Time	($I_{C(pk)}$ = 10 A, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5 V, $V_{CE(c1)}$ = 250 V)	(T_C = 25°C)	t_{sv}	–	1.3	–	μs
Fall Time			t_{fi}	–	0.06	–	
Storage Time		(T_C = 100°C)	t_{sv}	–	1.5	2.5	
Crossover Time			t_c	–	0.3	0.6	
Fall Time			t_{fi}	–	0.17	0.35	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

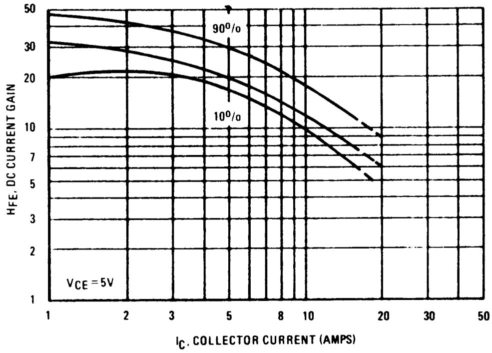


FIGURE 2 – COLLECTOR SATURATION REGION

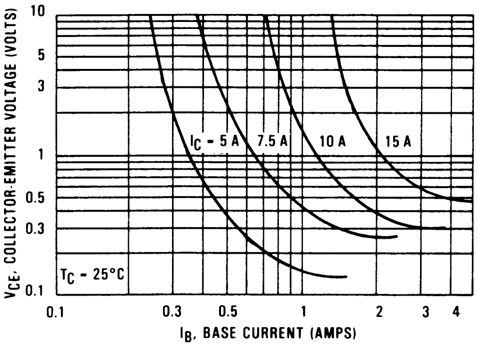


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

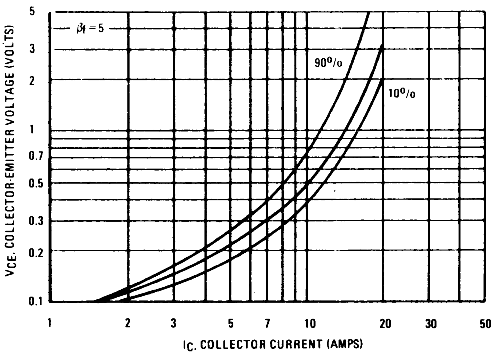


FIGURE 4 – BASE-EMITTER VOLTAGE

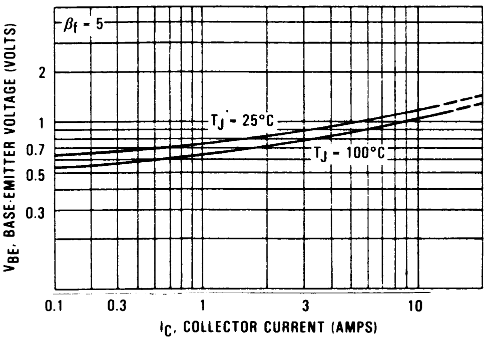


FIGURE 5 – COLLECTOR CUTOFF REGION

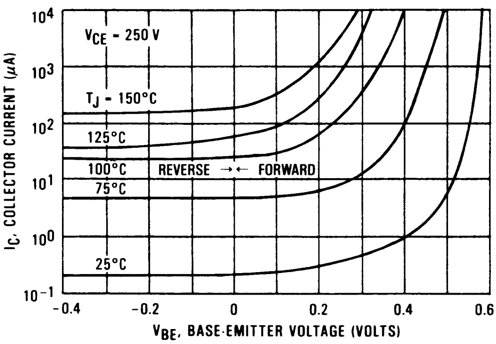


FIGURE 6 – CAPACITANCE

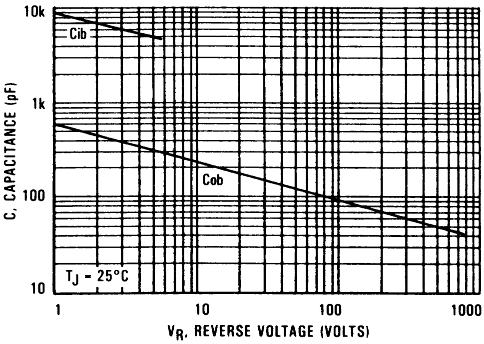


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

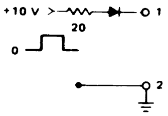
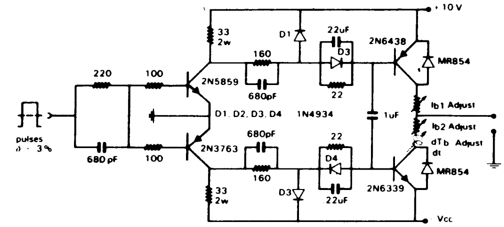
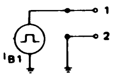
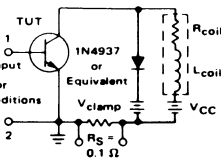
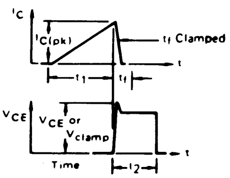
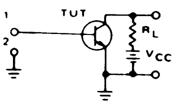
	VCEO(sus)	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA		TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 83 Ω Pulse Width = 10 μs
TEST CIRCUITS	**INDUCTIVE TEST CIRCUIT**  See Above for Detailed Conditions	**OUTPUT WAVEFORMS**  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	**RESISTIVE TEST CIRCUIT** 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

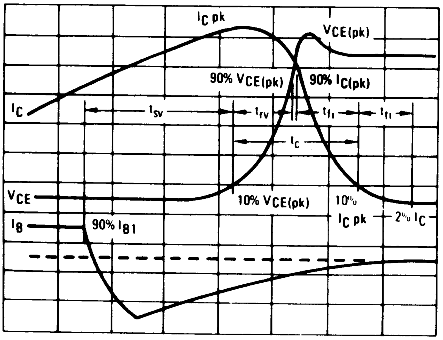
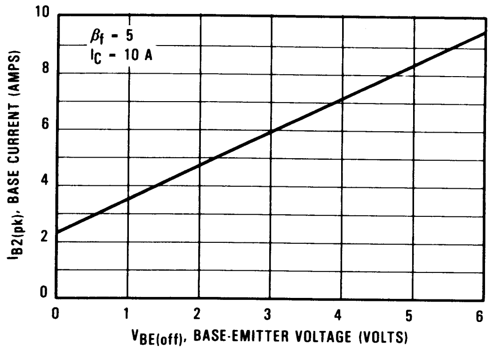


FIGURE 8 – PEAK-REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 – STORAGE TIME, Tsv

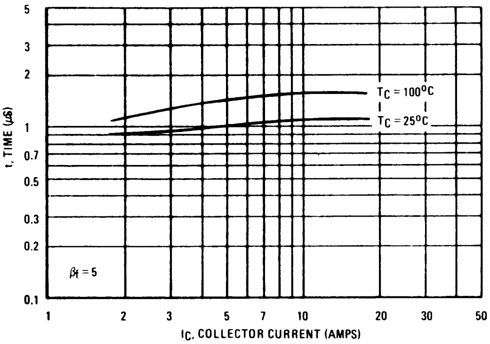


FIGURE 10 – CROSSOVER AND FALL TIMES

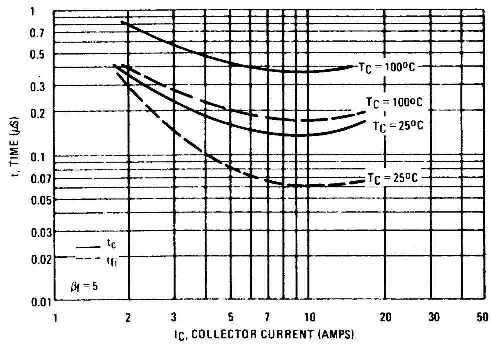


FIGURE 11a – TURN-OFF TIMES vs FORCED GAIN

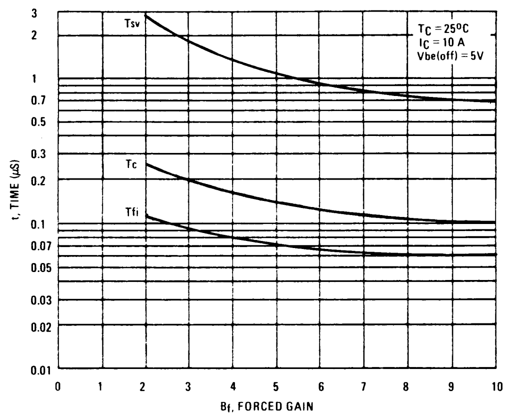
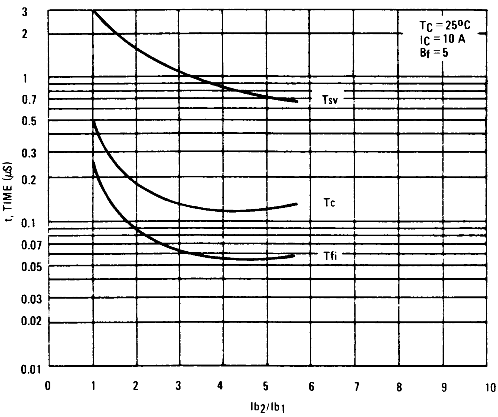


FIGURE 11b – TURN-OFF TIMES vs Ib2/Ib1



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

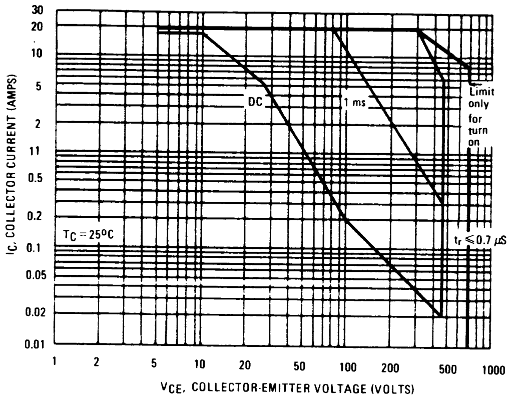


FIGURE 13 — REVERSE BIAS SAFE OPERATING AREA

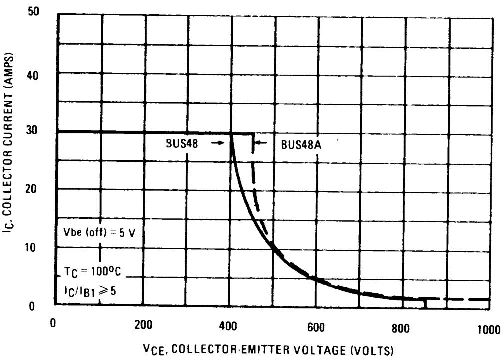
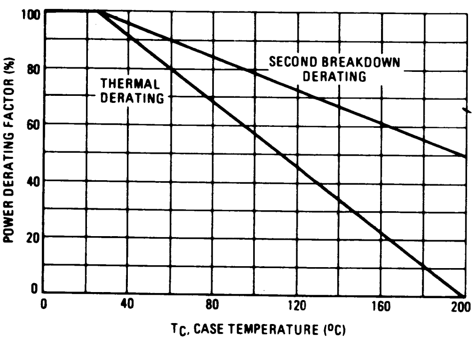


FIGURE 14 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

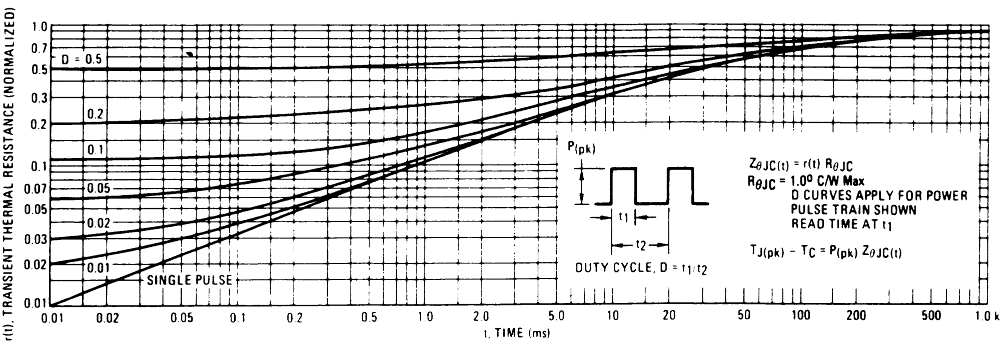
The data of Figure 12 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

FIGURE 15 — THERMAL RESPONSE



OVERLOAD CHARACTERISTICS

FIGURE 16 — RATED OVERLOAD SAFE OPERATING AREA (OLSOA)

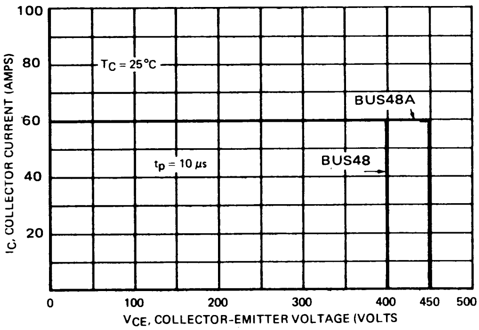
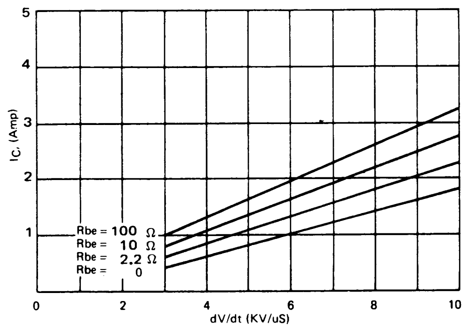


FIGURE 17 — $I_C = f(dV/dt)$



OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

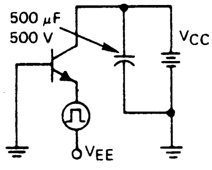
Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

FIGURE 18 — OVERLOAD SOA TEST CIRCUIT

Notes:

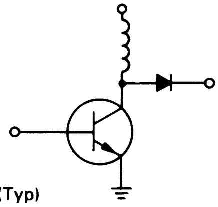
- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p



BUS 48P
BUS 48AP

SWITCHMODE II▲ SERIES NPN SILICON POWER TRANSISTORS

The BUS 48P/BUS 48AP transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:



- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

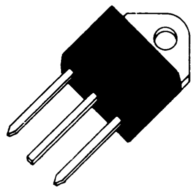
Fast Turn-Off Times
60 ns Inductive Fall Time—25°C (Typ)
120 ns Inductive Crossover Time—25°C (Typ)

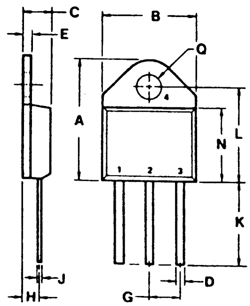
Operating Temperature Range −65 to +175°C
100°C Performance Specified for:
Reverse-Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents (125°C)

15 AMPERES

NPN SILICON POWER TRANSISTORS

400 and 450 VOLTS (BVCEO)
850 – 1000 VOLTS (BVCES)
150 WATTS





STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	3.94	4.19	0.155	0.165

CASE 340-01
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	BUS 48P	BUS 48AP	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	1000	Vdc
Emitter Base Voltage	V_{EB}	7		Vdc
Collector Current — Continuous — Peak(1) — Overload	I_C I_{CM} I_{OI}	15 30 60		Adc
Base Current – Continuous – Peak(1)	I_B I_{BM}	5 20		Adc
Total Power Dissipation – T_C = 25°C – T_C = 100°C Derate above 25°C	P_D	150 75 1.0		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +175		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≦ 10%.

1-83/DSER1

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 200$ mA, $I_B = 0$) L = 25 mH	BUS48P BUS48AP	$V_{CEO(sus)}$	400 450	–	–	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)} = 1.5$ Vdc) (V_{CEV} = Rated Value, $V_{BE(off)} = 1.5$ Vdc, $T_C = 125°C$)		I_{CEV}	– –	– –	0.2 2.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, $R_{BE} = 10\ \Omega$)	$T_C = 25°C$ $T_C = 125°C$	I_{CER}	–	–	0.5 3.0	mAdc
Emitter Cutoff Current ($V_{EB} = 5$ Vdc, $I_C = 0$)		I_{EBO}	–	–	0.1	mAdc
Emitter-base breakdown Voltage ($I_E = 50$ mA - $I_C = 0$)		B_{VEBO}	7.0	–	–	Vdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain ($I_C = 10$ Adc, $V_{CE} = 5$ Vdc) ($I_C = 8$ Adc, $V_{CE} = 5$ V)	BUS48 BUS48A	h_{FE}	8	–	–	
Collector-Emitter Saturation Voltage ($I_C = 10$ Adc, $I_B = 2$ Adc) ($I_C = 15$ Adc, $I_B = 3$ Adc) ($I_C = 10$ Adc, $I_B = 2$ Adc, $T_C = 100°C$)	BUS48P	$V_{CE(sat)}$	– – –	– – –	1.5 5.0 2.0	Vdc
($I_C = 8$ Adc, $I_B = 1.6$ Adc) ($I_C = 12$ Adc, $I_B = 2.4$ Adc) ($I_C = 8$ Adc, $I_B = 1.6$ Adc, $T_C = 100°C$)	BUS48AP		– – –	– – –	1.5 5.0 2.0	
Base-Emitter Saturation Voltage ($I_C = 10$ Adc, $I_B = 2$ Adc) ($I_C = 10$ Adc, $I_B = 2$ Adc, $T_C = 100°C$)	BUS48P	$V_{BE(sat)}$	– –	– –	1.6 1.6	Vdc
($I_C = 8$ Adc, $I_B = 1.6$ Adc) ($I_C = 8$ Adc, $I_B = 1.6$ Adc, $T_C = 100°C$)	BUS48AP		– –	– –	1.6 1.6	
DYNAMIC CHARACTERISTICS						
Output Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0$, $f_{test} = 100$ Khz)		C_{ob}	–	–	350	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Delay Time	($V_{CC} = 250$ Vdc, $I_C = 10$ A, $I_{B1} = 2.0$ A, $t_p = 30\ \mu s$, Duty Cycle 2 , $V_{BE(off)} = 5$ V)	t_d	–	0.1	0.2	μs
Rise Time		t_r	–	0.4	0.7	
Storage Time		t_s	–	1.3	2.0	
Fall Time		t_f	–	0.2	0.4	

Inductive Load, Clamped (Table 1)

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Storage Time	($I_{C(pk)} = 10$ A, $I_{B1} = 2.0$ A, $V_{BE(off)} = 5$ V, $V_{CE(c1)} = 250$ V)	($T_C = 25°C$)	t_{sv}	–	1.3	–	μs
Fall Time			t_{fi}	–	0.06	–	
Storage Time		($T_C = 100°C$)	t_{sv}	–	1.5	2.5	
Crossover Time			t_c	–	0.3	0.6	
Fall Time			t_{fi}	–	0.17	0.35	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≦ 2%.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

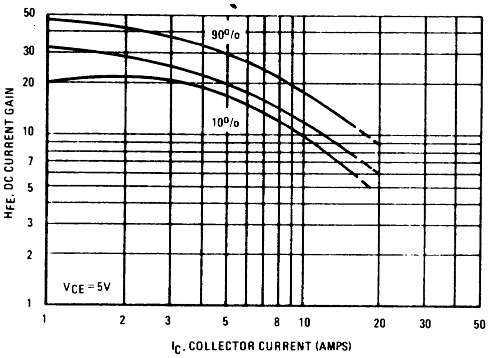


FIGURE 2 – COLLECTOR SATURATION REGION

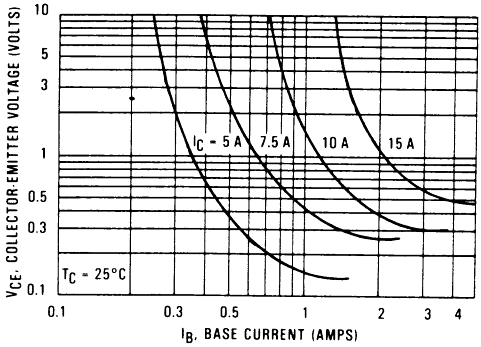


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

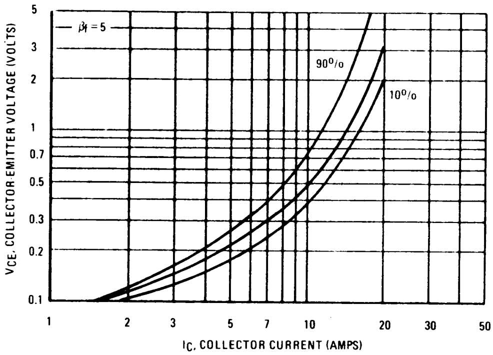


FIGURE 4 – BASE-EMITTER VOLTAGE

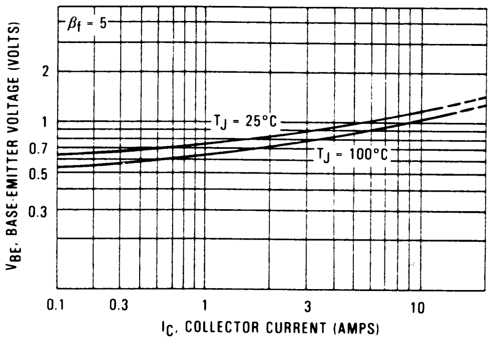


FIGURE 5 – COLLECTOR CUTOFF REGION

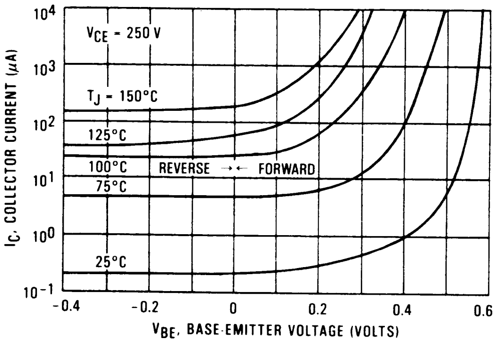


FIGURE 6 – CAPACITANCE

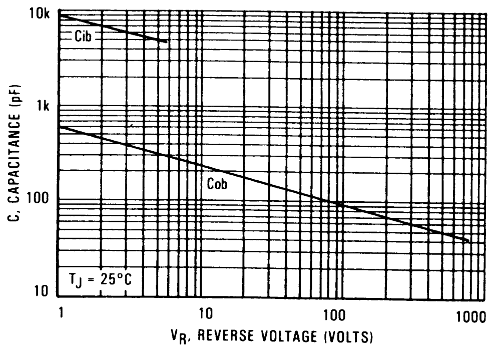


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

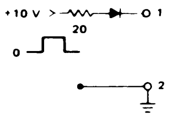
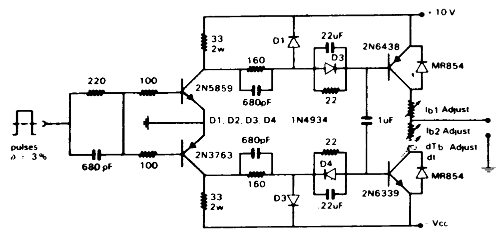
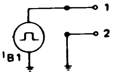
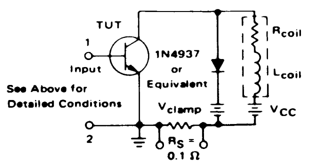
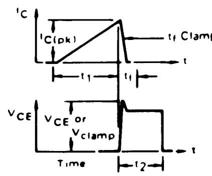
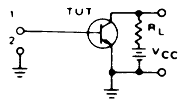
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA		TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 83 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above for Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

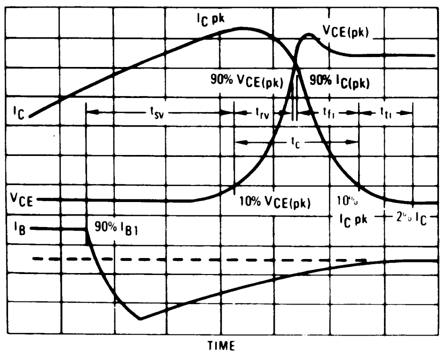
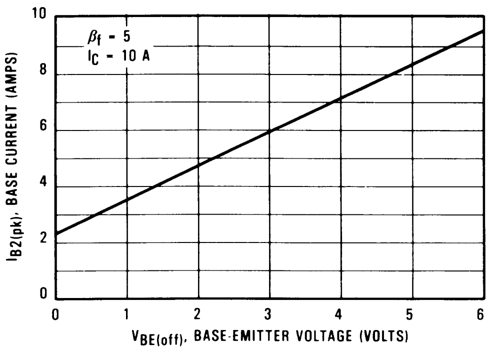


FIGURE 8 – PEAK-REVERSE CURRENT



SWITCHING TIMES NOTE

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t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 – STORAGE TIME, Tsv

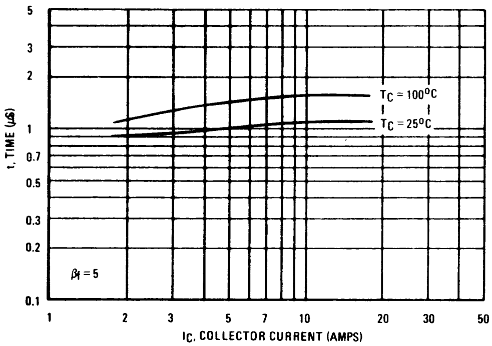


FIGURE 10 – CROSSOVER AND FALL TIMES

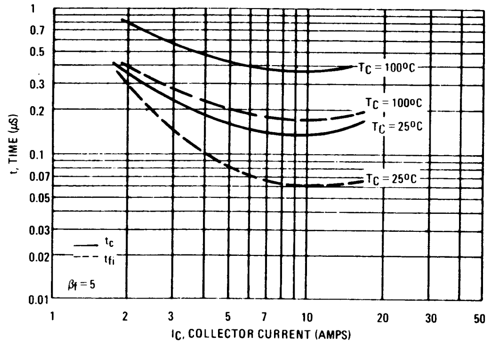


FIGURE 11a – TURN-OFF TIMES vs FORCED GAIN

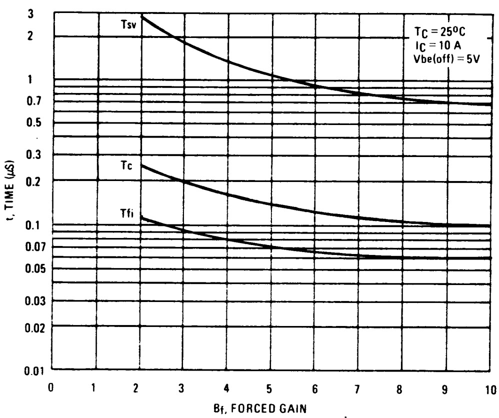
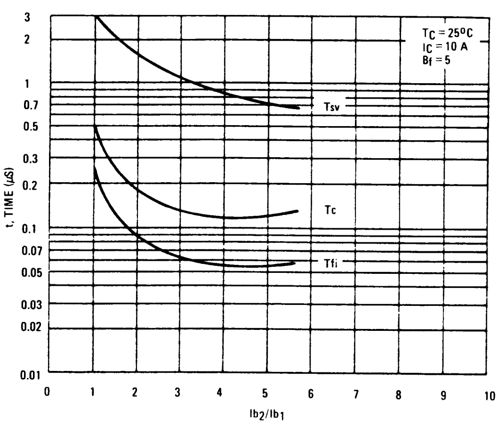


FIGURE 11b – TURN-OFF TIMES vs I_{b2}/I_{b1}



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

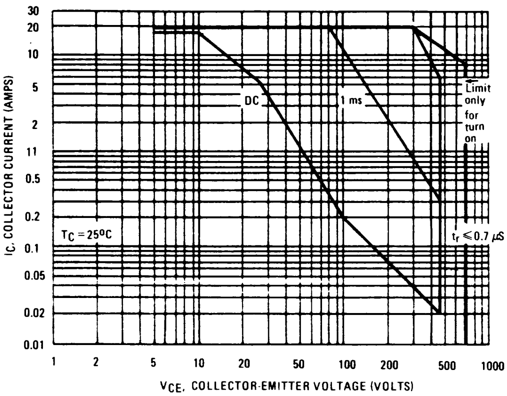


FIGURE 13 – REVERSE BIAS SAFE OPERATING AREA

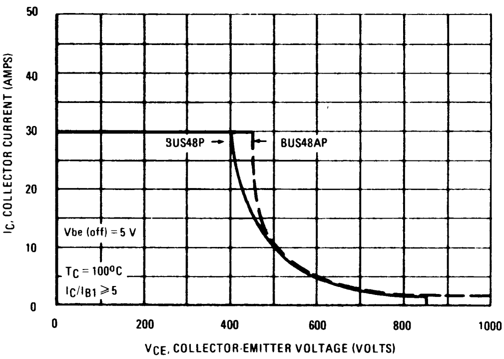
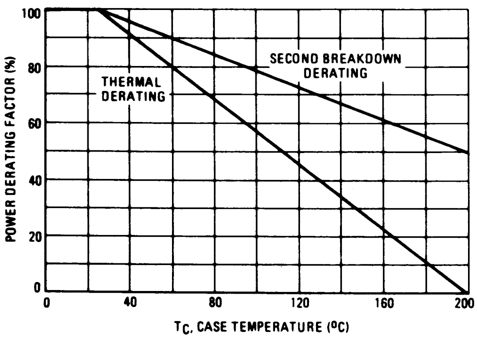


FIGURE 14 – POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

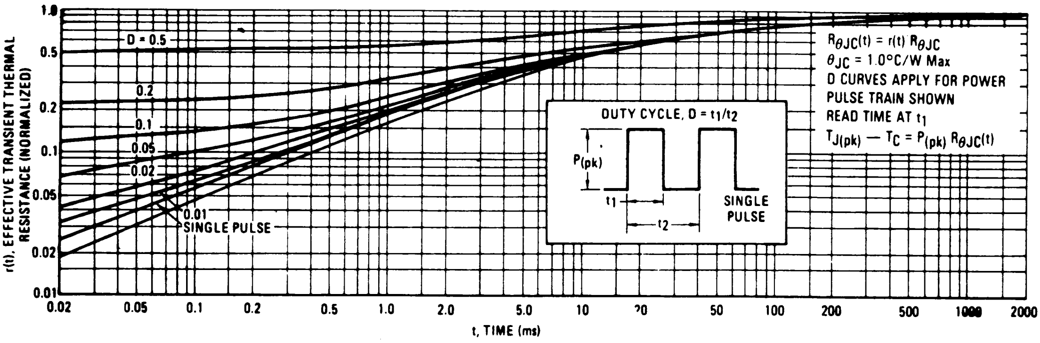
The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

FIGURE 15 – THERMAL RESPONSE



OVERLOAD CHARACTERISTICS

FIGURE 16 – RATED OVERLOAD SAFE OPERATING AREA (OLSOA)

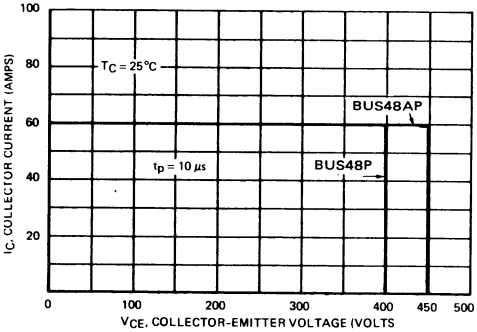
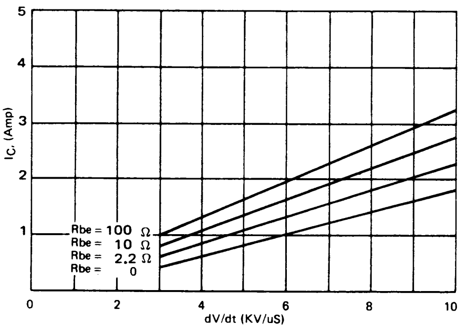


FIGURE 17 – $I_C = f(dV/dt)$



OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

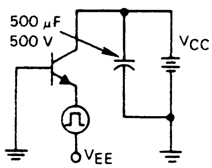
Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

FIGURE 18 – OVERLOAD SOA TEST CIRCUIT

Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p

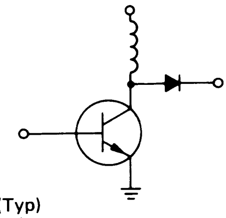


BUS 98
BUS 98A

SWITCHMODE II SERIES
NPN SILICON POWER TRANSISTORS

The BUS 98 and BUS 98A transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times
- 60 ns Inductive Fall Time – 25°C (Typ)
- 120 ns Inductive Crossover Time – 25°C (Typ)

Operating Temperature Range – 65 to + 200°C

100°C Performance Specified for :
- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents (125°C)

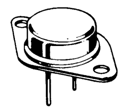
30 AMPERES

NPN SILICON POWER TRANSISTORS

400 AND 450 VOLTS (BVCEO)
250 WATTS
850 – 1000 V (BVCES)

Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



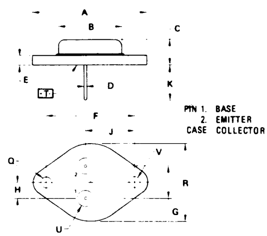
MAXIMUM RATINGS

Rating	Symbol	BUS 98	BUS98A	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	1000	Vdc
Emitter Base Voltage	V_{EB}	7		Vdc
Collector Current – Continuous – Peak (1) – Overload	I_C I_{CM} I_{ol}	30 60 120		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	10 30		Adc
Total Power Dissipation – T_C = 25°C – T_C = 100°C Derate above 25°C	P_D	250 142 1.42		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	– 65 to + 200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{θJC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES
1. DIMENSIONS Q AND V ARE DATUMS.
2. [T] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ∅ 0.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | ∅ 0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R		26.67		1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05

1-83/DSE R1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 200 mA, I_B = 0) L = 25 mH BUS98 BUS98A	$V_{CEO(sus)}$	400 450	– –	– –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	I_{CEV}	– –	– –	0.4 4.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 10 Ω) T_C = 25°C T_C = 125°C	I_{CER}	– –	– –	1.0 6.0	mAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}			0.2	mAdc
Emitter-base breakdown Voltage (I_E = 100 mA - I_C = 0)	V_{EBO}	7.0			Vdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$		See Figure 12		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 13		
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 20 Adc, V_{CE} = 5 Vdc) BUS98 (I_C = 16 Adc, V_{CE} = 5 V) BUS98A	h_{FE}	8	–	–	–
Collector-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 4 Adc) (I_C = 30 Adc, I_B = 8 Adc) BUS98 (I_C = 20 Adc, I_B = 4 Adc, T_c = 100°C) (I_C = 16 Adc, I_B = 3.2 Adc) (I_C = 24 Adc, I_B = 5 Adc) BUS98A (I_C = 16 Adc, I_B = 3.2 Adc, T_c = 100°C)	$V_{CE(sat)}$	– – – – – –	– – – – – –	1.5 3.5 2.0 1.5 5.0 2.0	Vdc
Base-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 4 Adc) (I_C = 20 Adc, I_B = 4 Adc, T_c = 100°C) BUS98 (I_C = 16 Adc, I_B = 3.2 Adc) (I_C = 16 Adc, I_B = 3.2 Adc, T_c = 100°C) BUS98A	$V_{BE(sat)}$	– – – –	– – – –	1.6 1.6 1.6 1.6	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 khz)	C_{ob}	–	–	700	pF

SWITCHING CHARACTERISTICS
Resistive Load (Table 1)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Delay Time	(V_{CC} = 250 Vdc, I_C = 20A, I_{B1} = 4.0 A, tp = 30 μs, Duty Cycle ≤ 2%, $V_{BE(off)}$ = 5 V) (for BUS98A : I_C = 16A, I_{b1} = 3.2A)	t_d	–	0.1	0.2	μs
Rise Time		t_r	–	0.4	0.7	
Storage Time		t_s	–	1.55	2.3	
Fall Time		t_f	–	0.2	0.4	

Inductive Load, Clamped (Table 1)

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Storage Time	$I_{C(pk)}$ = 20A, I_{b1} = 4A (BUS98)	(T_C = 25°C)	t_{sv}	–	1.55	–	μs
Fall Time			t_{fi}	–	0.06	–	
Storage Time	$V_{BE(off)}$ = 5 V, $V_{CE(c1)}$ = 250 V)	(T_C = 100°C)	t_{sv}	–	1.8	2.8	
Crossover Time	$I_{C(pk)}$ = 16A, I_{B1} = 3.2A (BUS98A)		t_c	–	0.3	0.6	
Fall Time			t_{fi}	–	0.17	0.35	

(1) Pulse Test : PW = 300 μs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

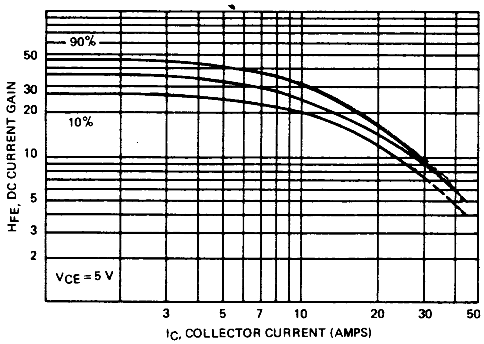


FIGURE 2 — COLLECTOR SATURATION REGION

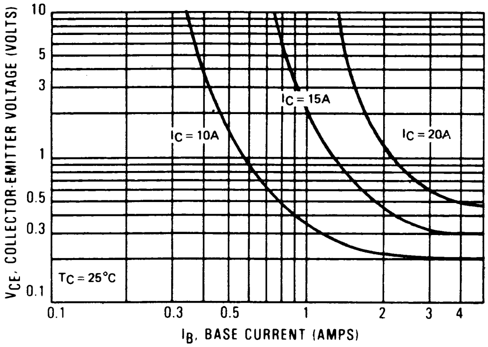


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

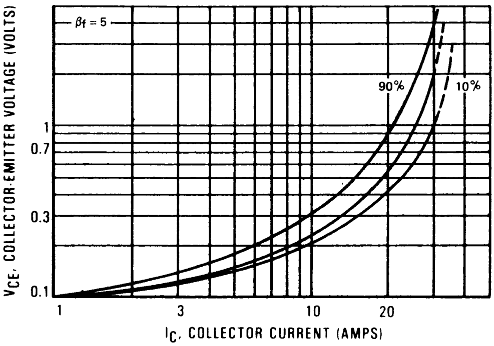


FIGURE 4 — BASE-EMITTER VOLTAGE

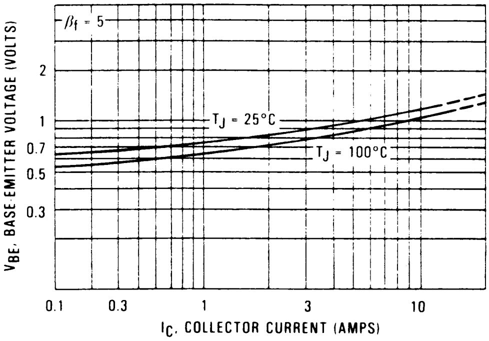


FIGURE 5 — COLLECTOR CUTOFF REGION

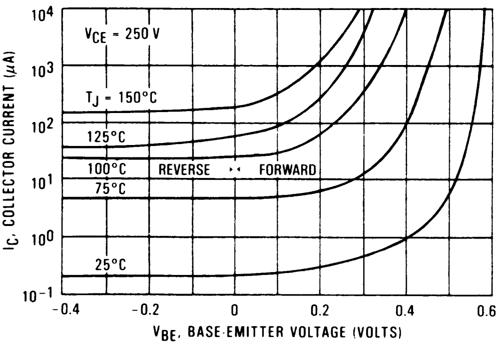


FIGURE 6 — CAPACITANCE

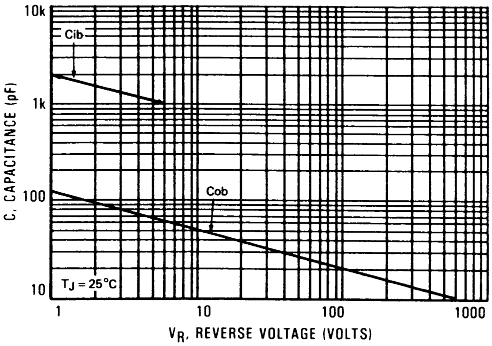


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

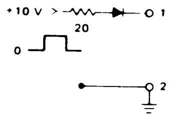
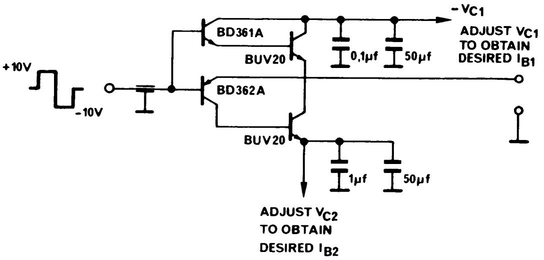
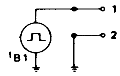
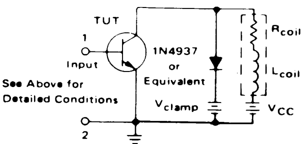
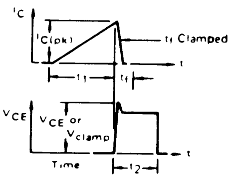
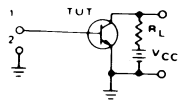
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA		TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 25 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V	V_{CC} = 250 V Pulse Width = 10 µs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above for Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

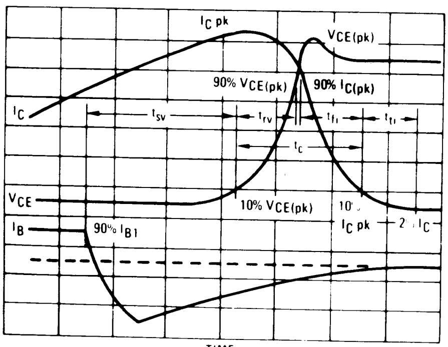
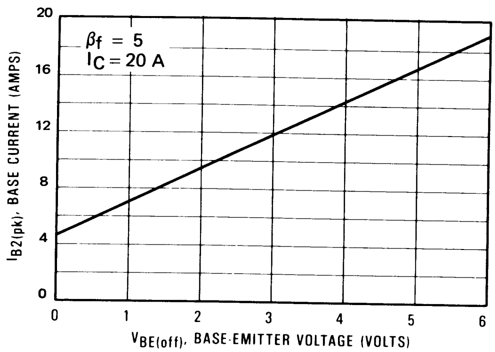


FIGURE 8 – PEAK-REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME, Tsv

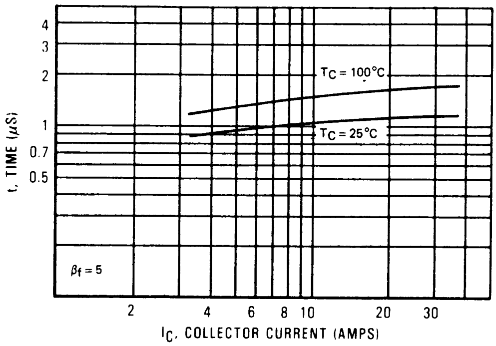


FIGURE 10 — CROSSOVER AND FALL TIMES

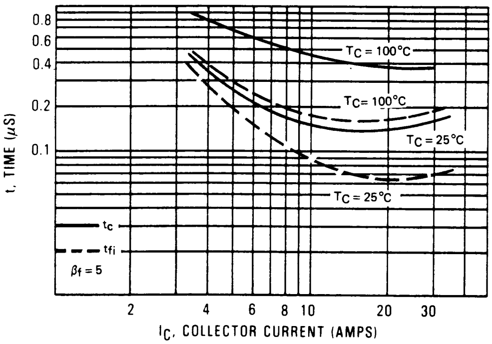


FIGURE 11a — TURN-OFF TIMES vs FORCED GAIN

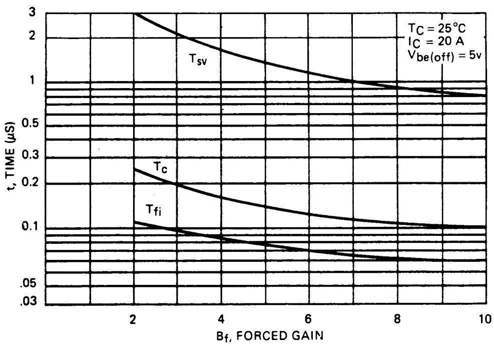
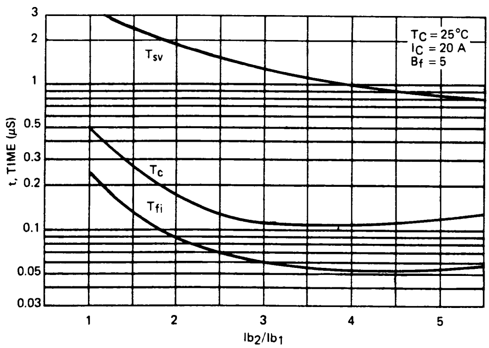


FIGURE 11b — TURN-OFF TM TIMES vs I_{b2}/I_{b1}



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

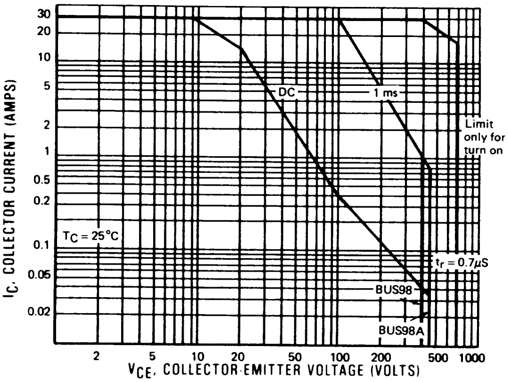


FIGURE 13 — REVERSE BIAS SAFE OPERATING AREA

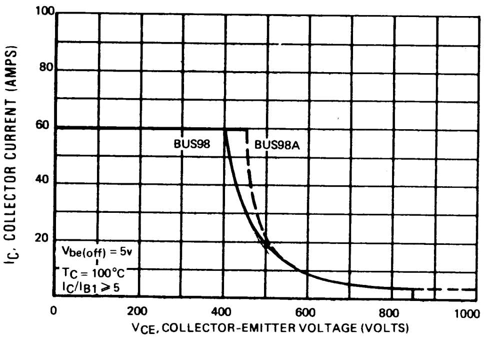
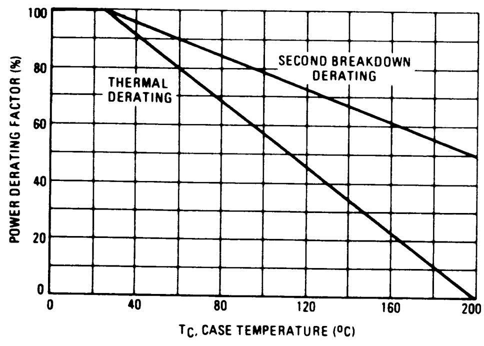


FIGURE 14 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

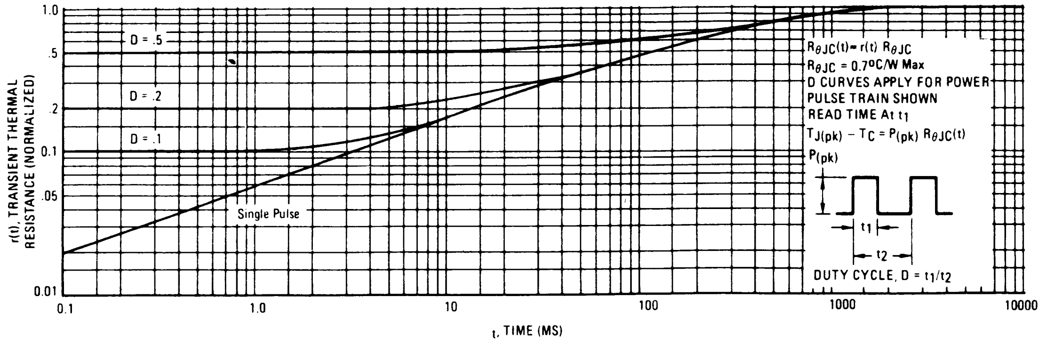
The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

FIGURE 15 — THERMAL RESPONSE



OVERLOAD CHARACTERISTICS

FIGURE 16 — RATED OVERLOAD SAFE OPERATING AREA (OLSOA)

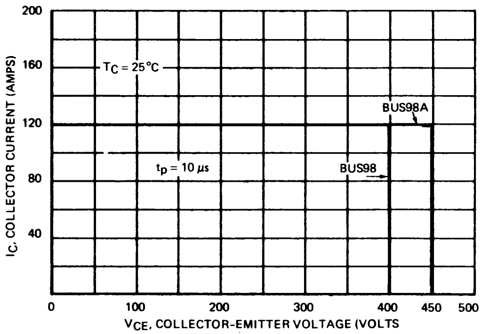
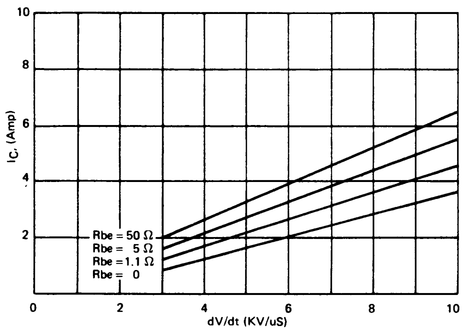


FIGURE 17 — $I_C = f$ (dV/dt)



OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

FIGURE 18 - OVERLOAD SOA TEST CIRCUIT

Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p