BUV 10N

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTOR

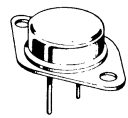
. . . designed for high current, high speed, high power applications.

- HFe min.: 20 at Ic = 10 A
- T_F max. = 0.45 μs at Ic = 15 A
- Equivalent to Bdy 58

25 AMPERES

NPN SILICON POWER METAL TRANSISTOR

125 VOLTS
175 WATTS



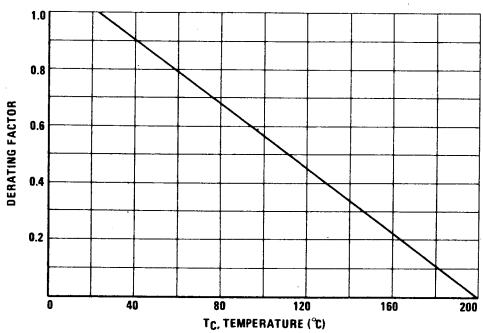
MAXIMUM RATINGS

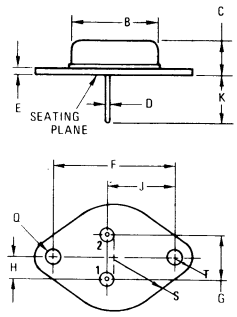
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	125	Vdc
Collector-Base Voltage	V_{CBO}	160	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage (V_{BE} = –1.5 V)	V_{CEX}	160	Vdc
Collector-Emitter Voltage (R_{BE} = 100Ω)	V_{CER}	140	Vdc
Collector-Current – continuous – peak (pw ≤ 10 ms)	I_C I_{CM}	25 30	Adc Apk
Base-Current continuous	I_B	6	Adc
Total Power Dissipation @ T_C = 25°C	P_D	175	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.0	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	–	0.312	–
Q	3.84	4.09	0.151	0.161
S	–	13.34	–	0.525
T	–	4.78	–	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

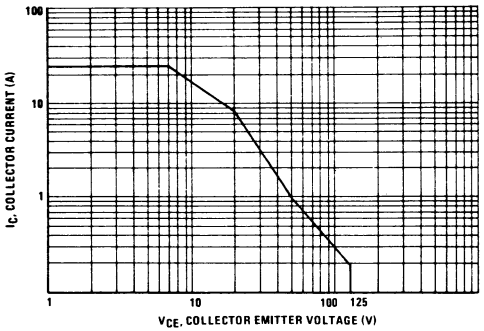
Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage ($I_C = 200$ mA, $I_B = 0$, L = 25 mH)	$V_{CEO(sus)}$	125		Vdc
Collector Cutoff Current at Reverse Biais: ($V_{CE} = 160$ V, $V_{BE} = -1.5$ V) ($V_{CE} = 160$ V, $V_{BE} = -1.5$ V, $T_C = 125°C$)	I_{CEX}		1.5 6	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 100$ V)	I_{CEO}		1.5	mAdc
Emitter-Base Reverse Voltage ($I_E = 50$ mA)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5$ V)	I_{EBO}		0.5	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased ($V_{CE} = 20$ V, t = 0.5 s) ($V_{CE} = 48$ V, t = 0.5 s)	$I_{S/b}$	8.75 1.0		Adc
ON CHARACTERISTICS[1]				
DC Current Gain ($I_C = 10$ A, $V_{CE} = 4$ V) ($I_C = 20$ A, $V_{CE} = 4$ V)	h_{FE}	20 10	60	
Collector-Emitter Saturation Voltage ($I_C = 10$ A, $I_B = 1$ A) ($I_C = 20$ A, $I_B = 2$ A)	$V_{CE(sat)}$		1 2.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 10$ A, $I_B = 1$ A)	$V_{BE(sat)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product ($V_{CE} = 15$ V, $I_C = 1$ A, f = 4 MHz)	f_T	10.0		MHz

SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 15$ A, $I_{B1} = I_{B2} = 1.5$ A, ($V_{CC} = 75$ V, RC = 5 Ω)	t_{on}		1.0	μs
Storage Time		t_s		1.55	
Fall Time		t_f		0.45	

[1] Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 – "ON" VOLTAGES

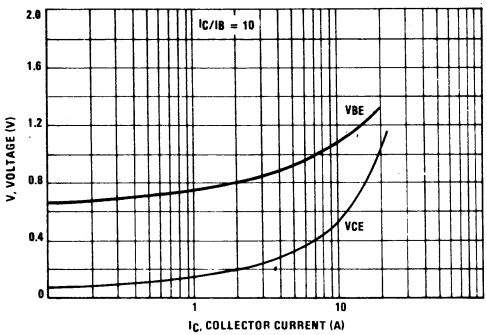


FIGURE 4 – DC CURRENT GAIN

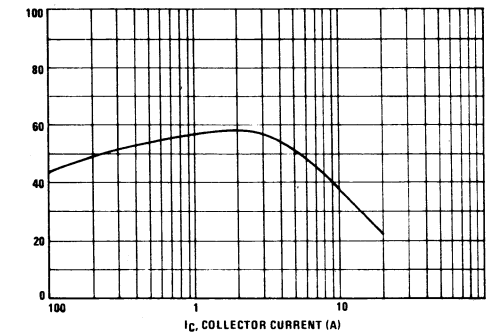


FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

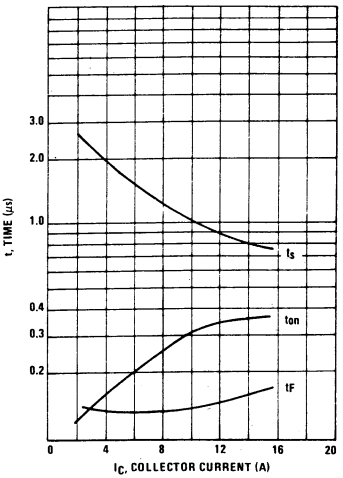
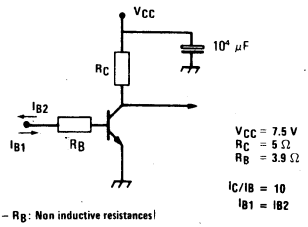


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



BUV 11

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTOR

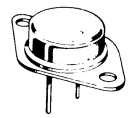
. . . designed for high current, high speed, high power applications.

- High DC current gain: HFE min. = 20 at Ic = 6 A
- Low $V_{CE(sat)}$, $V_{CE(sat)}$ max. = 0.6 V at Ic = 6 A
- Very fast switching times:
  T_F max. = 0.8 μs at Ic = 12 A

20 AMPERES

NPN SILICON POWER METAL TRANSISTOR

200 VOLTS
150 WATTS



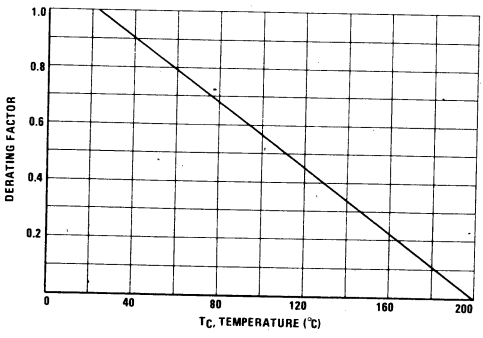
MAXIMUM RATINGS

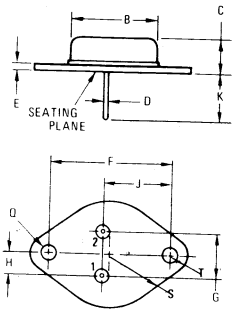
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	200	Vdc
Collector-Base Voltage	V_{CBO}	250	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage (V_{BE} = –1.5 V)	V_{CEX}	250	Vdc
Collector-Emitter Voltage (R_{BE} = 100Ω)	V_{CER}	240	Vdc
Collector-Current – continuous – peak (pw ≤ 10 ms)	I_C I_{CM}	20 25	Adc Apk
Base-Current continuous	I_B	4	Adc
Total Power Dissipation @ T_C = 25°C	P_D	150	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR
STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE-EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	–	0.312	–
Q	3.84	4.09	0.151	0.161
S	–	13.34	–	0.525
T	–	4.78	–	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

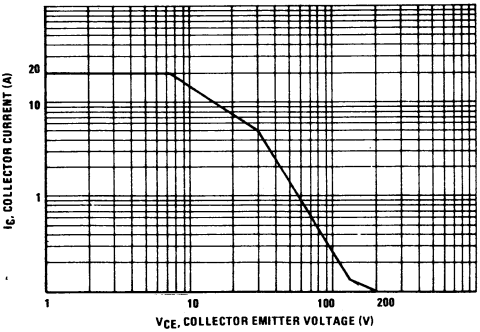
Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage ($I_C = 200$ mA, $I_B = 0$, L = 25 mH)	$V_{CEO(sus)}$	200		Vdc
Collector Cutoff Current at Reverse Biais: ($V_{CE} = 250$ V, $V_{BE} = -1.5$ V) ($V_{CE} = 250$ V, $V_{BE} = -1.5$ V, $T_C = 125°C$)	I_{CEX}		1.5 6	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 160$ V)	I_{CEO}		1.5	mAdc
Emitter-Base Reverse Voltage ($I_E = 50$ mA)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5$ V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased ($V_{CE} = 30$ V, t = 1 s) ($V_{CE} = 140$ V, t = 1 s)	$I_{S/b}$	5.0 0.15		Adc
ON CHARACTERISTICS[1]				
DC Current Gain ($I_C = 6$ A, $V_{CE} = 2$ V) ($I_C = 12$ A, $V_{CE} = 4$ V)	h_{FE}	20 10	60	
Collector-Emitter Saturation Voltage ($I_C = 6$ A, $I_B = 0.6$ A) ($I_C = 12$ A, $I_B = 1.5$ A)	$V_{CE(sat)}$		0.6 1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 12$ A, $I_B = 1.5$ A)	$V_{BE(sat)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product ($V_{CE} = 15$ V, $I_C = 1$ A, f = 4 MHz)	f_T	8.0		MHz

SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 12$ A, $I_{B1} = I_{B2} = 1.5$ A, ($V_{CC} = 150$ V, RC = 12.5 Ω)	t_{on}		0.8	μs
Storage Time		t_s		1.8	
Fall Time		t_f		0.4	

[1] Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 – "ON" VOLTAGES

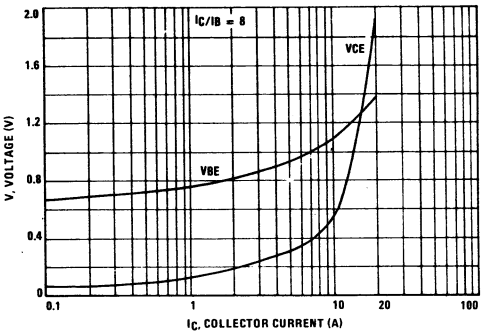


FIGURE 4 – DC CURRENT GAIN

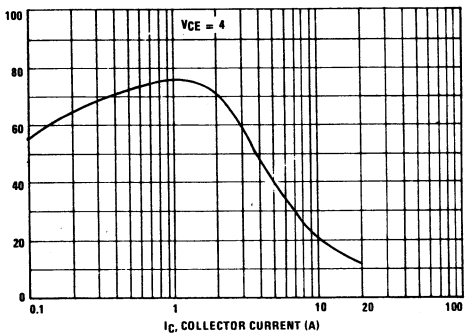


FIGURE 5 – SWITCHING TIMES VERSUS COLLECTOR CURRENT

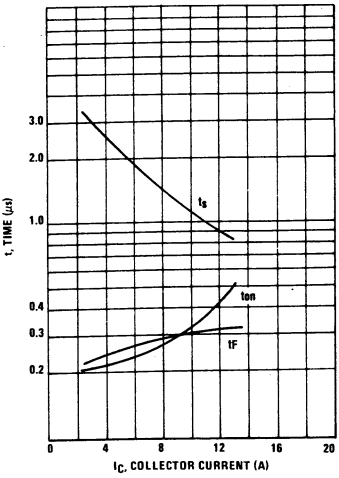
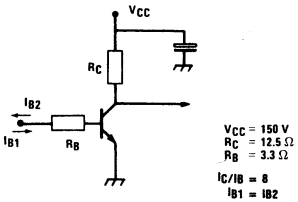


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



RC – RB: Non inductives resistances

BUV11N

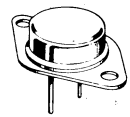
NPN SILICON POWER METAL TRANSISTOR

. . . designed for high speed, high current, high power applications.

- High DC Current gain – H_{FE} min 20 @ I_C = 8 A
- Very fast switching times
  t_F max. = 0.25 μs @ I_C = 15 A
- Low $V_{CE(sat)}$: $V_{CE(sat)}$ max. = 0.6 V, @ I_C = 8A
- High V_{CEO}: 160 V.

NPN SILICON
POWER
METAL TRANSISTOR

20 AMPERES



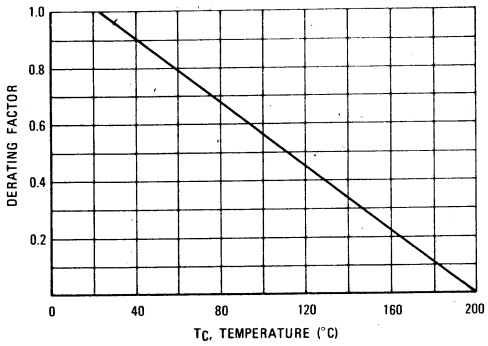
MAXIMUM RATINGS

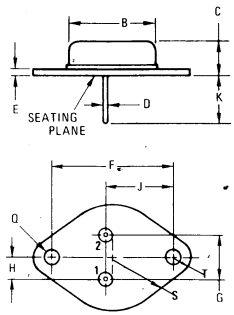
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	160	Vdc
Collector-Base Voltage	V_{CBO}	220	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage (V_{BE} = -1.5 V)	V_{CEX}	220	Vdc
Collector-Emitter Voltage (R_{BE} = 100Ω)	V_{CER}	200	Vdc
Collector-Current – continuous – peak (pw ≤ 10 ms)	I_C I_{CM}	20 25	Adc Apk
Base-Current continuous	I_B	5	Adc
Total Power Dissipation @ T_C = 25 °C	P_D	150	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR

STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE-EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
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K	7.92	–	0.312	–
Q	3.84	4.09	0.151	0.161
S	–	13.34	–	0.525
T	–	4.78	–	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

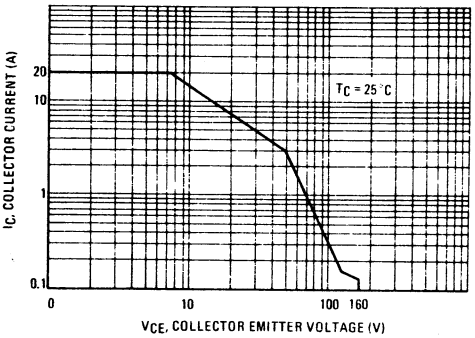
Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)	$V_{CEO(sus)}$	160		Vdc
Collector Cutoff Current at Reverse Bias: (V_{CE} = 220 V, V_{BE} = −1.5 V) (V_{CE} = 220 V, V_{BE} = −1.5 V, T_C = 125 °C)	I_{CEX}		1.5	mAdc
Collector-Emitter Cutoff Current (V_{CE} = 130 V)	I_{CEO}		1.5	
Emitter-Base Reverse Voltage (I_E = 50 mA)	V_{EBO}	7		V
Emitter-Cutoff Current (V_{EB} = 5 V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased (V_{CE} = 30 V, t = 1 s) (V_{CE} = 140 V, t = 1 s)	$I_{S/b}$	5 0.15		Adc
ON CHARACTERISTICS[1]				
DC Current Gain (I_C = 8 A, V_{CE} = 2 V) (I_C = 15 A, V_{CE} = 4 V)	h_{FE}	20 10	60	
Collector-Emitter Saturation Voltage (I_C = 8 A, I_B = 0.8 A) (I_C = 15 A, I_B = 1.88 A)	$V_{CE(sat)}$		0.6 1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 15 A, I_B = 1.88 A)	$V_{BE(sat)}$		1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (V_{CE} = 15 V, I_C = 1 A, f = 4 MHz)	f_T	8		MHz

SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	(I_C = 15 A, I_{B1} = I_{B2} = 1.88 A, V_{CC} = 30 V, RL ≈ 2Ω)	t_{on}		1.2	μs
Storage Time		t_s		1.2	
Fall Time		t_f		0.25	

[1] Pulse Test: Pulse Width ⩽ 300 μs, Duty Cycle ⩽2%.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



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The data of figure 2 is based on T_C = 25 °C; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 – "ON" VOLTAGES

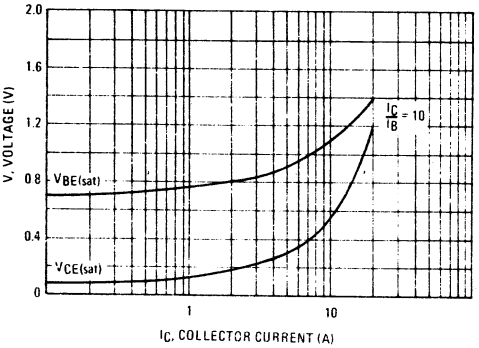
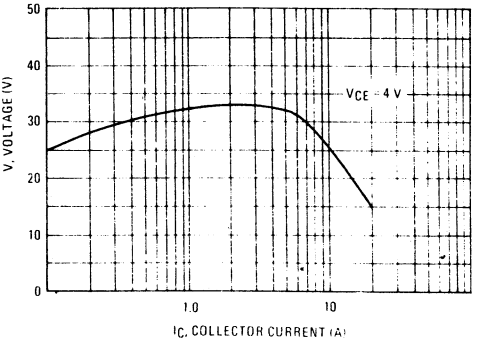


FIGURE 4 – DC CURRENT GAIN



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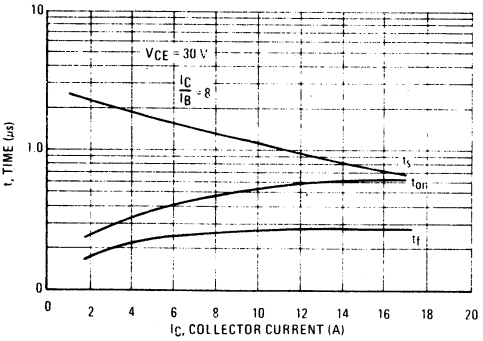

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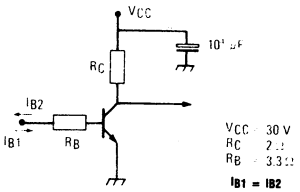


R_C - R_B: Non inductive resistances

BUV 12

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTOR

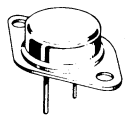
. . . designed for high speed, high voltage, high power applications.

- High DC current gain:
  HFE min. = 20 at Ic = 5 A
- Very fast switching times:
  T_S max. = 1.5 μs at Ic = 10 A
  T_F max. = 0.5 μs at Ic = 10 A

20 AMPERES

NPN SILICON POWER METAL TRANSISTOR

250 VOLTS
150 WATTS



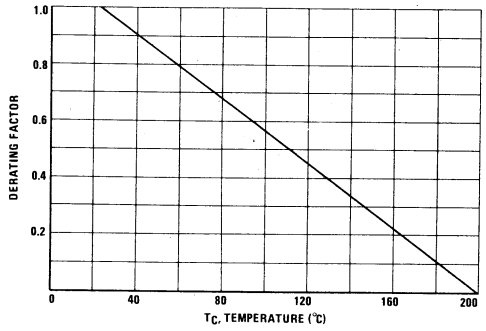
MAXIMUM RATINGS

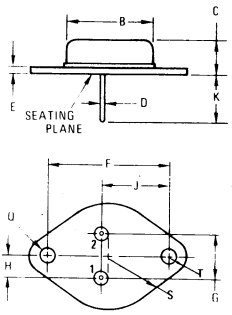
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	250	Vdc
Collector-Base Voltage	V_{CBO}	300	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage (V_{BE} = −1.5 V)	V_{CEX}	300	Vdc
Collector-Emitter Voltage (R_{BE} = 100Ω)	V_{CER}	290	Vdc
Collector-Current — continuous — peak (pw ≤ 10 ms)	I_C I_{CM}	20 25	Adc Apk
Base-Current continuous	I_B	4	Adc
Total Power Dissipation @ T_C = 25°C	P_D	150	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR

STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE-EMITTER

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	–	0.312	–
Q	3.84	4.09	0.151	0.161
S	–	13.34	–	0.525
T	–	4.78	–	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

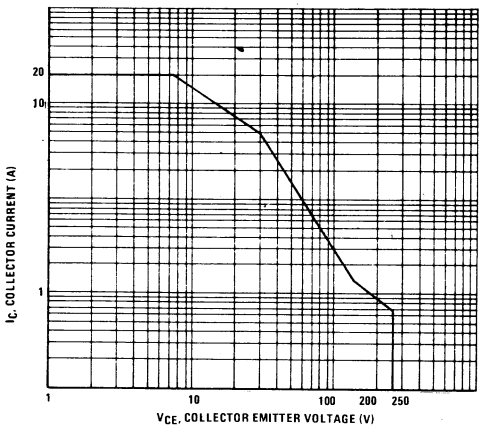
Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage ($I_C = 200$ mA, $I_B = 0$, L = 25 mH)	$V_{CEO(sus)}$	250		Vdc
Collector Cutoff Current at Reverse Biais: ($V_{CE} = 300$ V, $V_{BE} = -1.5$ V) ($V_{CE} = 300$ V, $V_{BE} = -1.5$ V, $T_C = 125°C$)	I_{CEX}		1.5 6	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 200$ V)	I_{CEO}		1.5	mAdc
Emitter-Base Reverse Voltage ($I_E = 50$ mA)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5$ V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased ($V_{CE} = 30$ V, t = 1 s) ($V_{CE} = 140$ V, t = 1 s)	$I_{S/b}$	5.0 0.15		Adc
ON CHARACTERISTICS[1]				
DC Current Gain ($I_C = 5$ A, $V_{CE} = 4$ V) ($I_C = 10$ A, $V_{CE} = 4$ V)	h_{FE}	20 10	60	
Collector-Emitter Saturation Voltage ($I_C = 5$ A, $I_B = 0.5$ A) ($I_C = 10$ A, $I_B = 1.25$ A)	$V_{CE(sat)}$		1.0 1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 10$ A, $I_B = 1.25$ A)	$V_{BE(sat)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product ($V_{CE} = 15$ V, $I_C = 1$ A, f = 4 MHz)	f_T	8.0		MHz

SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 10$ A, $I_{B1} = I_{B2} = 1.25$ A, ($V_{CC} = 150$ V, RC = 15 Ω)	t_{on}		0.7	μs
Storage Time		t_s		1.5	
Fall Time		t_f		0.5	

[1] Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.
The data of figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.
At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 – "ON" VOLTAGES

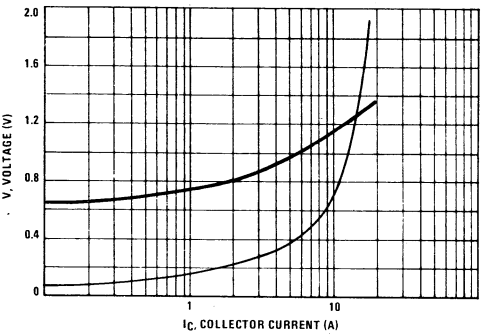


FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

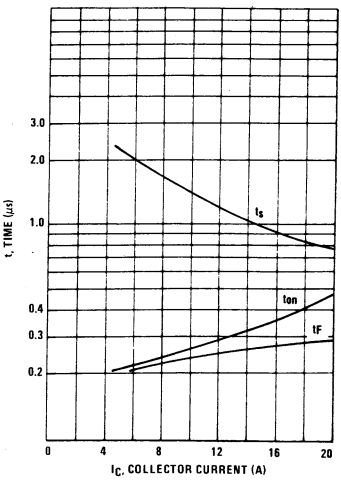


FIGURE 4 – DC CURRENT GAIN

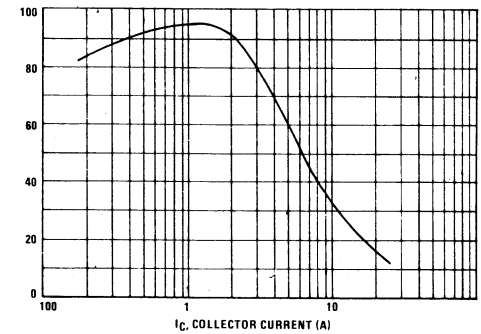
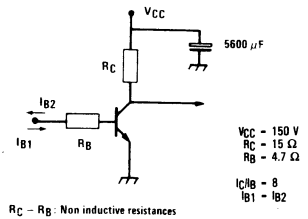


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



R_C – R_B: Non inductive resistances