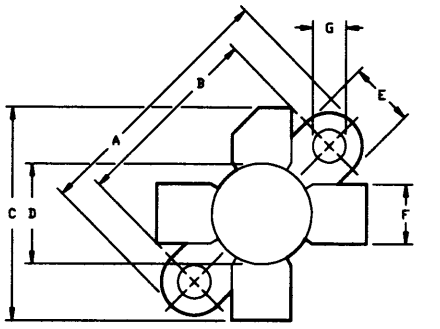
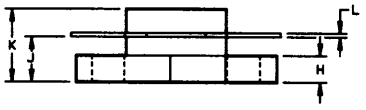
15 Watts, 30-175 MHz, 12 V

Features

- DMOS Structure
- Lower Capacitances for Broadband Operation
- High Saturated Output Power
- Lower Noise Figure Than Bipolar Devices
- Specifically Designed for 12 Volt Applications





LETTER DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.64	24.89	.970	.980
B	18.29	18.54	.720	.730
C	20.07	20.83	.790	.820
D	9.47	9.73	.373	.383
E	6.22	6.48	.245	.255
F	5.64	5.79	.222	.228
G	2.92	3.30	.115	.130
H	2.29	2.67	.090	.105
J	4.04	4.55	.159	.179
K	6.58	7.39	.259	.291
L	.10	.15	.004	.006

Package Outline

Absolute Maximum Ratings at 25°C

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	20	V
Drain-Source Current	I_{DS}	4	A
Power Dissipation	P_D	87.5	W
Junction Temperature	T_J	200	°C
Storage Temperature	T_{STG}	-55 to +150	°C
Thermal Resistance	θ_{JC}	2	°C/W

Electrical Characteristics at 25°C

Parameter	Symbol	Min	Max	Units	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	40	-	V	V_{GS}=0.0 V, I_{DS}=5.0 mA
Drain-Source Leakage Current	I_{DSS}	-	1.0	mA	V_{DS}=15.0 V, V_{GS}=0.0 V
Gate-Source Leakage Current	I_{GSS}	-	1.0	µA	V_{GS}=20.0 V, V_{DS}=0.0 V
Gate Threshold Voltage	$V_{GS(TH)}$	2.0	6.0	V	V_{DS}=10.0 V, I_{DS}=100 mA
Forward Transconductance	G_M	0.5	-	S	V_{DS}=10.0 V, I_{DS}=1000 mA, ΔV_{GS}=1.0 V
Input Capacitance	C_{ISS}		50	pF	V_{DS}=12.0 V, F=1.0 MHz
Output Capacitance	C_{OSS}		60	pF	V_{DS}=12.0 V, F=1.0 MHz
Reverse Capacitance	C_{RSS}		12	pF	V_{DS}=12.0 V, F=1.0 MHz
Power Gain	G_P	9.5	-	dB	V_{DD}=12.0 V, I_{DQ}=100 mA, P_{OUT}=15 W, F=175 MHz
Drain Efficiency	η_D	60	-	%	V_{DD}=12.0 V, I_{DQ}=100 mA, P_{OUT}=15 W, F=175 MHz
Load Mismatch Tolerance	VSWR-T	-	30:1	-	V_{DD}=12.0 V, I_{DQ}=100 mA, P_{OUT}=15 W, F=175 MHz

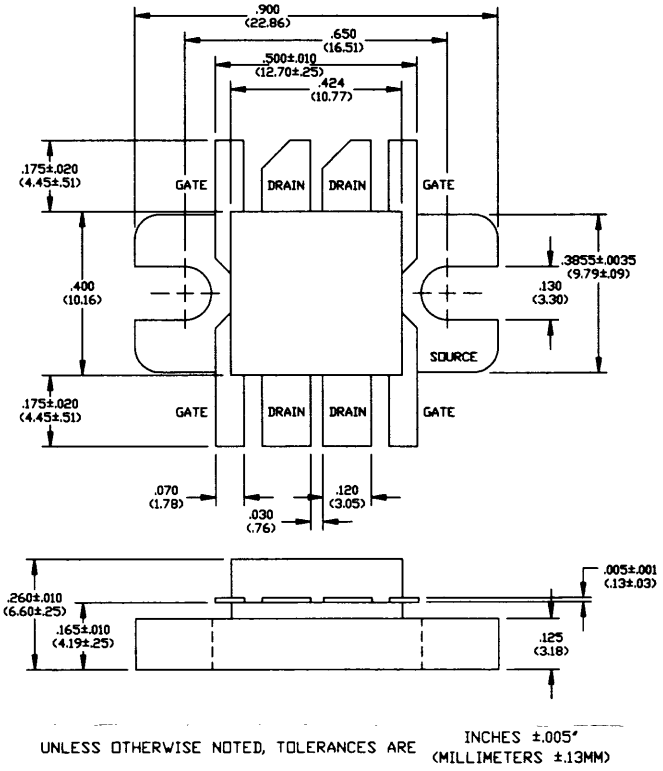
Preliminary

30 Watts, 30 - 175 MHz, 12 V

Features

- N-Channel Enhancement Mode Device
- HF to VHF Applications
- 30 Watts CW
- Common Source Push-Pull Configuration
- DMOS Structure
- Aluminum Metallization

Outline Drawing



UNLESS OTHERWISE NOTED, TOLERANCES ARE INCHES ±.005" (MILLIMETERS ±.13MM)

Absolute Maximum Ratings at 25°C

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	20	V
Drain-Source Current	I_{DS}	8	A
Power Dissipation	P_D	125	W
Junction Temperature	T_J	200	°C
Storage Temperature	T_{STG}	-55 to +150	°C
Thermal Resistance	θ_{JC}	1.4	°C/W

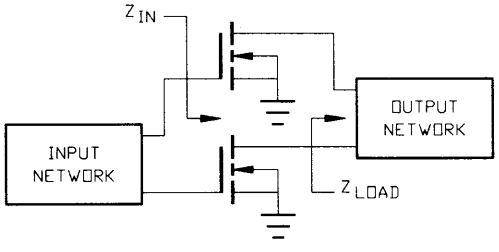
Electrical Characteristics at 25°C (* per side)

Parameter	Symbol	Min	Max	Units	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	40	-	V	I_D=5.0 mA, V_{GS}=0.0 V*
Drain-Source Leakage Current	I_{DSS}	-	1.0	mA	V_{DS}=28.0 V, V_{GS}=0.0 V*
Gate-Source Leakage Current	I_{GSS}	-	1.0	µA	V_{GS}=20 V, V_{DS}=0.0 V*
Gate Threshold Voltage	$V_{GS(TH)}$	2.0	6.0	V	V_{DS}=10.0 V, I_{DS}=100 mA*
Forward Transconductance	G_M	500	-	mS	V_{DS}=10.0 V, I_{DS}=1000 mA (pulsed)*
Input Capacitance	C_{ISS}		50	pF	V_{DS}=12.0 V, F=1.0 MHz*
Output Capacitance	C_{OSS}		60	pF	V_{DS}=12.0 V, F=1.0 MHz*
Reverse Capacitance	C_{RSS}		12	pF	V_{DS}=12.0 V, F=1.0 MHz*
Power Gain	G_P	10	-	dB	V_{DD}=12.0 V, I_{DQ}=200 mA, P_{OUT}=30 W, F=175 MHz
Drain Efficiency	η_D	55	-	%	V_{DD}=12.0 V, I_{DQ}=200 mA, P_{OUT}=30 W, F=175 MHz
Load Mismatch Tolerance	VSWR-T	-	30:1	-	V_{DD}=12.0 V, I_{DQ}=200 mA, P_{OUT}=30 W, F=175 MHz

Typical Optimum Device Impedances

F(MHz)	Z_{IN}(Ω)	Z_{LOAD}(Ω)
30	40 - j40	5.5 + j5.5
100	20 - j30	5.0 + j4.0
175	7.5 - j22	4.6 + j3.5

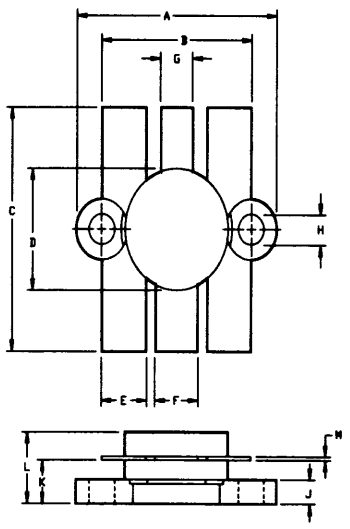
V_{DD}=12 V, I_{DQ}=200 mA, P_{OUT}=30 W



60 Watts, 30-175 MHz, 12 V

Features

- DMOS Structure
- Lower Capacitances for Broadband Operation
- High Saturated Output Power
- Lower Noise Figure Than Bipolar Devices
- Specifically Designed for 12 Volt Applications



LETTER	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	24.38	25.15	.960	.990
B	18.29	18.54	.720	.730
C	21.36	21.74	.841	.856
D	12.60	12.85	.496	.506
E	5.33	5.59	.210	.220
F	5.08	5.33	.200	.210
G	3.81	4.06	.150	.160
H	3.10	3.15	.122	.124
J	2.51	2.67	.099	.105
K	4.06	4.57	.160	.180
L	6.68	7.49	.263	.295
M	.10	.15	.004	.006

Package Outline

Absolute Maximum Ratings at 25°C

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	20	V
Drain-Source Current	I_{DS}	24	A
Power Dissipation	P_D	250	W
Junction Temperature	T_J	200	°C
Storage Temperature	T_{STG}	-55 to +150	°C
Thermal Resistance	θ_{JC}	0.7	°C/W

Electrical Characteristics at 25°C

Parameter	Symbol	Min	Max	Units	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	40	-	V	V_{GS}=0.0 V, I_{DS}=30.0 mA
Drain-Source Leakage Current	I_{DSS}	-	6.0	mA	V_{DS}=15.0 V, V_{GS}=0.0 V
Gate-Source Leakage Current	I_{GSS}	-	6.0	µA	V_{GS}=20 V, V_{DS}=0.0 V
Gate Threshold Voltage	$V_{GS(TH)}$	2.0	6.0	V	V_{DS}=10.0 V, I_{DS}=600 mA
Forward Transconductance	G_M	3.0	-	S	V_{DS}=10.0 V, I_{DS}=6000 mA, ΔV_{GS}=1.0 V
Input Capacitance	C_{ISS}		200	pF	V_{DS}=12.0 V, F=1.0 MHz
Output Capacitance	C_{OSS}		240	pF	V_{DS}=12.0 V, F=1.0 MHz
Reverse Capacitance	C_{RSS}		48	pF	V_{DS}=12.0 V, F=1.0 MHz
Power Gain	G_P	8.0	-	dB	V_{DD}=12.0 V, I_{DQ}=600 mA, P_{OUT}=60 W, F=175 MHz
Drain Efficiency	η_D	60	-	%	V_{DD}=12.0 V, I_{DQ}=600 mA, P_{OUT}=60 W, F=175 MHz
Load Mismatch Tolerance	VSWR-T	-	30:1	-	V_{DD}=12.0 V, I_{DQ}=600 mA, P_{OUT}=60 W, F=175 MHz