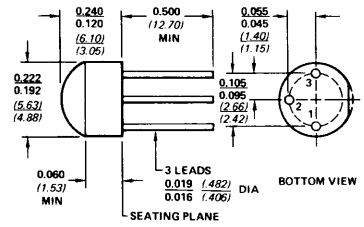
Performance Curves NVA
See Page 4-48

N-CHANNEL SILICON JUNCTION FIELD-EFFECT TRANSISTORS

FOR ANALOG SWITCHES, CHOPPERS AND COMMUTATORS

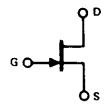
These epoxy-encapsulated FETs are characterized for analog switching applications requiring zero dc offset voltage, low ON resistance and low switching aperture times.

- $r_{DS(on)}$ = 3 Ω Max (E105)
- $t_{d(on)} + t_r + t_{d(off)} + t_f$ = 70 ns Typical



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

TO-106



PIN	OUT
1	S
2	D
3	G

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	-30 V
Gate Current	50 mA
Total Device Dissipation (25°C Free-Air Temperature)	350 mW
Power Derating (to +125°C)	3.5 mW/°C
Storage Temperature Range	-55 to +125°C
Operating Temperature Range	-55 to +125°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		E105			E106			E107			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-3			-3			-3	nA	V_{DS} = 0, V_{GS} = -15 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4.5		-10	-2		-6	-0.5		-4.5	V	V_{DS} = 5 V, I_D = 1 μA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-30			-30			-30			V	V_{DS} = 0, I_G = -1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	500			200			100			mA	V_{DS} = 15 V, V_{GS} = 0	
5	STATIC	$I_{D(off)}$	Drain Cutoff Current (Note 1)			3			3			3	nA	V_{DS} = 5 V, V_{GS} = -10 V	
6	STATIC	$r_{DS(on)}$	Drain Source ON Resistance			3			6			8	Ω	$V_{DS} \leq 0.1$ V, V_{GS} = 0	
7	DYNAMIC	$C_{dg(off)}$	Drain Gate OFF Capacitance			35			35			35	pF	V_{DS} = 0, V_{GS} = -10 V	f = 1 MHz
8	DYNAMIC	$C_{sg(off)}$	Source Gate OFF Capacitance			35			35			35	pF	V_{DS} = 0, V_{GS} = -10 V	f = 1 MHz
9	DYNAMIC	$C_{dg(on)} + C_{sg(on)}$	Drain Gate plus Source Gate ON Capacitance			160			160			160	pF	V_{DS} = V_{GS} = 0	f = 1 MHz
10	DYNAMIC	$t_{d(on)}$	Turn On Delay Time		15			15			15		ns	Switching Time Test Conditions	
11	DYNAMIC	t_r	Rise Time		20			20			20		ns		
12	DYNAMIC	$t_{d(off)}$	Turn Off Delay Time		15			15			15		ns		
13	DYNAMIC	t_f	Fall Time		20			20			20		ns		

Switching Time Test Conditions	E105	E106	E107
V_{DD}	1.5 V	1.5 V	1.5 V
$V_{GS(off)}$	-12 V	-7 V	-5 V
R_L	50 Ω	50 Ω	50 Ω

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ≤ 3%.

NVA

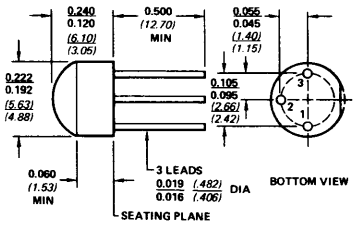
Performance Curves NI
See Page 4-30

N-CHANNEL SILICON JUNCTION FIELD-EFFECT TRANSISTORS

FOR ANALOG SWITCHES, CHOPPERS AND COMMUTATIONS

These epoxy-encapsulated FETs are characterized for analog switching applications requiring zero dc offset voltage, low ON resistance and low switching aperture times.

- $r_{DS(on)}$ = 8 Ω Max (E108)
- $t_{d(on)} + t_r + t_{d(off)} + t_f$ = 41 ns Typical



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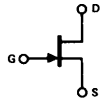


PIN	OUT
1	S
2	D
3	G

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage ..... -25 V
Gate Current ..... 50 mA
Total Device Dissipation
(25°C Free-Air Temperature) ..... 350 mW
Power Derating (to +125°C) ..... 3.5 mW/°C
Storage Temperature Range ..... -55 to +125°C
Operating Temperature Range ..... -55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) ..... 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		E108			E109			E110			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-3			-3			-3	nA	V_{DS} = 0, V_{GS} = -15 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-3		-10	-2		-6	-0.5		-4	V	V_{DS} = 5 V, I_D = 1 μA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25			V	V_{DS} = 0, I_G = -1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	80			40			10			mA	V_{DS} = 15 V, V_{GS} = 0	
5	STATIC	$I_{D(off)}$	Drain Cutoff Current (Note 1)			3			3			3	nA	V_{DS} = 5 V, V_{GS} = -10 V	
6	STATIC	$r_{DS(on)}$	Drain Source ON Resistance			8			12			18	Ω	V_{DS} < 0.1 V, V_{GS} = 0	
7	DYNAMIC	$C_{dg(off)}$	Drain Gate OFF Capacitance			15			15			15	pF	V_{DS} = 0, V_{GS} = -10 V	f = 1 MHz
8	DYNAMIC	$C_{sg(off)}$	Source Gate OFF Capacitance			15			15			15	pF	V_{DS} = 0, V_{GS} = -10 V	f = 1 MHz
9	DYNAMIC	$C_{dg(on)}$ + $C_{sg(on)}$	Drain Gate Plus Source Gate ON Capacitance			85			85			85	pF	V_{DS} = V_{GS} = 0	f = 1 MHz
10	DYNAMIC	$t_{d(on)}$	Turn On Delay Time		4			4			4		ns	Switching Time Test Conditions	
11	DYNAMIC	t_r	Rise Time		1			1			1		ns	V_{DD} E108: 1.5 V, E109: 1.5 V, E110: 1.5 V	
12	DYNAMIC	$t_{d(off)}$	Turn Off Delay Time		6			6			6		ns	V_{GS} E108: -12 V, E109: -7 V, E110: -5 V	
13	DYNAMIC	t_f	Fall Time		30			30			30		ns	R_L E108: 150 Ω, E109: 150 Ω, E110: 150 Ω	

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ≤ 3%.

NI

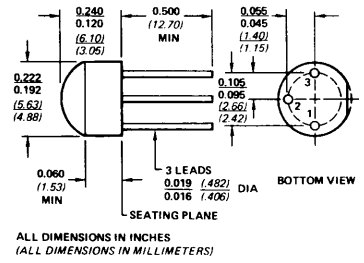
Performance Curves NC
See Page 4-23

N-CHANNEL SILICON JUNCTION FIELD-EFFECT TRANSISTORS

FOR ANALOG SWITCHES, CHOPPERS AND COMMUTATORS

These epoxy-encapsulated FETs are characterized for analog switching applications requiring zero dc offset voltage and moderate values of ON resistance and capacitance.

- $r_{DS(on)}$ = 30 Ω Max (E111)
- $C_{dg(on)} + C_{sg(on)}$ = 28 pF Max



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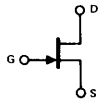


PIN	OUT
1	S
2	D
3	G

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage ..... -35 V
Gate Current ..... 50 mA
Total Device Dissipation
(25°C Free-Air Temperature)..... 350 mW
Power Derating (to +125°C)..... 3.5 mW/°C
Storage Temperature Range..... -55 to +125°C
Operating Temperature Range ..... -55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds)..... 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristics		E111			E112			E113			Unit	Test Conditions
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)))			-1			-1			-1	nA	V_{DS} = 0, V_{GS} = -15 V
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-3		-10	-1		-5	-0.5		-3	V	V_{DS} = 5 V, I_D = 1 μA
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-35			-35			-35			V	V_{DS} = 0, I_G = -1 μA
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	20			5			2			mA	V_{DS} = 15 V, V_{GS} = 0
5	STATIC	$I_{D(off)}$	Drain Cutoff Current (Note 1)			1			1			1	nA	V_{DS} = 5 V, V_{GS} = -10 V
6	STATIC	$r_{DS(on)}$	Drain Source ON Resistance			30			50			100	Ω	V_{DS} < 0.1 V, V_{GS} = 0
7	DYNAMIC	$C_{dg(off)}$	Drain Gate OFF Capacitance			5			5			5	pF	V_{DS} = 0, V_{GS} = -10 V; f = 1 MHz
8	DYNAMIC	$C_{sg(off)}$	Source Gate OFF Capacitance			5			5			5	pF	V_{DS} = 0, V_{GS} = -10 V; f = 1 MHz
9	DYNAMIC	$C_{dg(on)} + C_{sg(on)}$	Drain Gate Plus Source Gate ON Capacitance			28			28			28	pF	V_{DS} = V_{GS} = 0; f = 1 MHz
10	DYNAMIC	$t_{d(on)}$	Turn on Delay Time		7			7			7		ns	Switching Time Test Conditions
11	DYNAMIC	t_r	Rise Time		6			6			6		ns	
12	DYNAMIC	$t_{d(off)}$	Turn Off Delay Time		20			20			20		ns	
13	DYNAMIC	t_f	Fall Time		15			15			15		ns	

Switching Time Test Conditions	E111	E112	E113
V_{DD}	10 V	10 V	10 V
V_{GS}	-12 V	-7 V	-5 V
R_L	800 Ω	1,600 Ω	3,200 Ω

NC

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ≤ 3%.

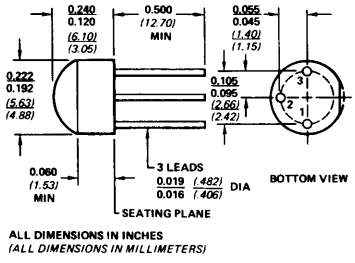
Performance Curves NZF
See Page 4-49

N-CHANNEL SILICON JUNCTION FIELD-EFFECT TRANSISTOR

FOR ANALOG SWITCHES, CHOPPERS AND COMMUTATORS

This FET is characterized for analog switching applications requiring zero dc offset voltage, low capacitance, and fast switching.

- $C_{gd(on)} + C_{sg(on)}$ = 8 pF Max
- t_r = 3 ns Typical
- t_f = 8 ns Typical



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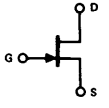


PIN	OUT
1	S
2	D
3	G

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage ..... -25 V
Gate Current ..... 50 mA
Total Device Dissipation
(25°C Free-Air Temperature)..... 350 mW
Power Derating (to +125°C)..... 3.5 mW/°C
Storage Temperature Range..... -55 to +125°C
Operating Temperature Range..... -55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds)..... 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		E114 Min	E114 Typ	E114 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-1	nA	V_{DS} = 0, V_{GS} = -15 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-3		-10	V	V_{DS} = 5 V, I_D = 1 μA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-25			V	V_{DS} = 0, I_G = -1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	15			mA	V_{DS} = 15 V, V_{GS} = 0	
5	STATIC	$I_{D(off)}$	Drain Cutoff Current (Note 1)			1	nA	V_{DS} = 5 V, V_{GS} = -10 V	
6	STATIC	$r_{DS(on)}$	Drain Source ON Resistance			150	Ω	$V_{DS} \leq 0.1$ V, V_{GS} = 0	
7	DYNAMIC	$C_{dg(off)}$	Drain Gate OFF Capacitance			2	pF	V_{DS} = 0, V_{GS} = -10 V	f = 1 MHz
8	DYNAMIC	$C_{sg(off)}$	Source Gate OFF Capacitance			2	pF	V_{DS} = 0, V_{GS} = -10 V	f = 1 MHz
9	DYNAMIC	$C_{dg(on)}$ + $C_{sg(on)}$	Drain Gate Plus Source Gate ON Capacitance			8	pF	V_{DS} = V_{GS} = 0	f = 1 MHz
10	DYNAMIC	$t_{d(on)}$	Turn On Delay Time		3		ns	Switching Time Test Conditions: V_{DD} = 10 V, V_{GS} = -12 V, R_L = 1 KΩ	
11	DYNAMIC	t_r	Rise Time		3		ns		
12	DYNAMIC	$t_{d(off)}$	Turn Off Delay Time		12		ns		
13	DYNAMIC	t_f	Fall Time		8		ns		

NZF

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ≤ 3%.

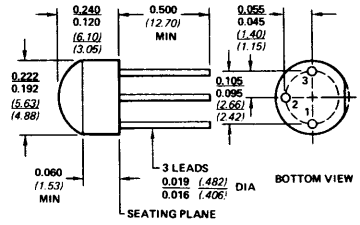
Performance Curves PS
See Page 4-61

P-CHANNEL SILICON JUNCTION FIELD-EFFECT TRANSISTORS

FOR ANALOG SWITCHES, CHOPPERS AND COMMUTATORS

These epoxy-encapsulated FETs are characterized for analog switching applications requiring zero dc offset voltage, low ON resistance (for P-channel devices) and low switching aperture times.

- $r_{DS(on)}$ = 85 Ω Max (E174)
- $t_{d(on)} + t_r + t_{d(off)} + t_f$ = 22 ns Typical



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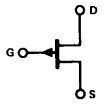

PIN	OUT
1	S
2	G
3	D

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) ..... 30 V
Gate Current ..... 50 mA
Total Device Dissipation
(25°C Free-Air Temperature)..... 350 mW
Power Derating (to +125°C)..... 3.5 mW/°C
Storage Temperature Range..... -55 to +125°C
Operating Temperature Range ..... -55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds)..... 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristics		E174			E175			E176			E177			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			1			1			1			1	nA	V_{DS} = 0, V_{GS} = 20 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	5		10	3		6	1		4	0.8		2.25	V	V_{DS} = -15 V, I_D = -10 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30			30			30			30			V	V_{DS} = 0, I_G = 1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 3)	-20		-100	-7		-60	-2		-25	-1.5		-20	mA	V_{DS} = -15 V, V_{GS} = 0	
5	STATIC	$I_{D(off)}$	Drain Cutoff Current (Note 2)			-1			-1			-1			-1	nA	V_{DS} = -15 V, V_{GS} = 10 V	
6	STATIC	$r_{DS(on)}$	Drain Source ON Resistance			85			125			250			300	Ω	$V_{DS} \leq$ 0.1 V, V_{GS} = 0	
7	DYNAMIC	$C_{dg(off)}$	Drain Gate OFF Capacitance		5.5			5.5			5.5			5.5		pF	V_{DS} = 0, V_{GS} = 10 V	f = 1 MHz
8	DYNAMIC	$C_{sg(off)}$	Source Gate OFF Capacitance		5.5			5.5			5.5			5.5		pF	V_{DS} = 0, V_{GS} = 10 V	f = 1 MHz
9	DYNAMIC	$C_{dg(on)}$ + $C_{sg(on)}$	Drain Gate Plus Source Gate ON Capacitance		40			40			40			40		pF	V_{DS} = V_{GS} = 0	f = 1 MHz
10	DYNAMIC	$t_{d(on)}$	Turn On Delay Time		2			5			15			20		ns	Switching Time Test Conditions	
11	DYNAMIC	t_r	Rise Time		5			10			20			25		ns		
12	DYNAMIC	$t_{d(off)}$	Turn Off Delay Time		5			10			15			20		ns		
13	DYNAMIC	t_f	Fall Time		10			20			20			25		ns		

Switching Time Test Conditions	E174	E175	E176	E177
V_{DD}	-10 V	-6 V	-6 V	-6 V
$V_{GS(off)}$	12 V	8 V	6 V	3 V
R_L	560 Ω	1.2 KΩ	5.6 KΩ	10 KΩ

NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 300 μs; duty cycle ≤ 3%.

PS