HEWLETT PACKARD

POWER MOS FIELD-EFFECT TRANSISTORS

HPWR-6501
HPWR-6502
HPWR-6503
HPWR-6504

TECHNICAL DATA SHEET SEPTEMBER 1980

Features

FAST SWITCHING WITH SIMPLE DRIVE CIRCUITS

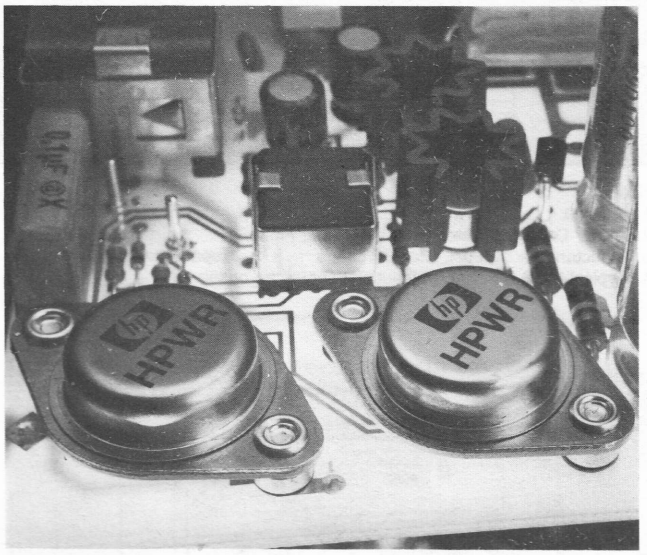
MAJORITY-CARRIER DEVICE: NO STORAGE TIME UPON TURNOFF

HIGH BREAKDOWN VOLTAGE

NO SECOND BREAKDOWN

TEMPERATURE-STABLE SWITCHING SPEEDS

EASE OF PARALLEL OPERATION



Applications

SWITCHING POWER SUPPLIES

POWER INVERTERS & CONVERTERS

MOTOR DRIVES

ULTRASONIC DRIVERS

AUDIO AMPLIFIERS

GENERAL INDUSTRIAL HIGH VOLTAGE, HIGH CURRENT SWITCHING

Description

The Hewlett-Packard HPWR-6501 Series are silicon MOS Field-Effect Power Transistors. They are N-channel, enhancement-mode devices designed for use in high voltage, high current, high speed power switching applications.

Electrical Specifications at T_{CASE} =25°C

Symbol	Parameters and Test Conditions		HPWR-6501	HPWR-6502	HPWR-6503	HPWR-6504	Units
BV_{DSS}(1)	Breakdown Voltage (Drain-to-Source)	I_D = 0.1 mA, V_{GS} = 0	450	400	450	400	V min
I_{DSS}(2)	Leakage Current (Drain-to-Source)	V_{GS} = 0, V_{DS} = 400V	10	—	10	—	μA max
		V_{DS} = 360V	—	10	—	10	μA max
$R_{DS(on)}$(1)	On-State Resistance (Drain-to-Source)	V_{GS} = 20V, I_D = 3A, T_C = 25°C	0.85	0.75	1.0	1.0	Ω max
		T_C = 125°C	1.7	1.5	2.0	2.0	Ω typ
g_{fs}(1)	Forward Transconductance V_{DS} = 20V, I_D = 3A		1.8	1.8	1.8	1.8	S (℧) typ
$V_{GS}(th)$(2)	Gate Threshold Voltage I_D = 1.0 mA, V_{GD} = 0		3/7	3/7	3/7	3/7	V min/max
I_{GSS}(2)	Gate Leakage Current V_{GS} = ±20V		0.1	0.1	0.1	0.1	μA max
C_{iss}	Input Capacitance	f = 1.0 MHz	1000	1000	1000	1000	pF typ
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 50V	30	30	30	30	
C_{oss}	Output Capacitance	V_{GS} = 0	100	100	100	100	
$t_{d(on)}$(3)	Turn on Delay Time	V_{DD} = 200V, I_D = 3A	30	30	30	30	ns typ
t_r(3)	Drain Current Rise Times		20	20	20	20	
$t_{d(off)}$(3)	Turn off Delay Time		60	60	60	60	
t_f(3)	Drain Current Fall Time		15	15	15	15	
θ_{Jc}	Thermal Resistance, Junction to Case		1.39	1.39	1.39	1.39	°C/W max

Notes:
1. Pulsed Test: tp ≤ 300 μs, Duty Factor ≤ 1.8%.
2. D.C. Test Curve-Tracer or Equivalent.
3. See Figures 11,12,13,14.

Maximum Ratings

Symbol	Parameter	HPWR-6501	HPWR-6502	HPWR-6503	HPWR-6504	Units
V_{DS}	Voltage, Drain to Source(1)	450	400	450	400	V
I_D	Drain Current, Continuous	6	6	5	5	A
I_{DM}	Drain Current, Pulsed	12	12	10	10	A
V_{GS}	Voltage, Gate-to-Source(4)	±40	±40	±40	±40	V
P_D	Power Dissipation(2)	90	90	90	90	W
I_L	Drain Current, Clamped Inductive(3)	6	6	5	5	A
T_j (oper)	Junction Operating Temperature	−55 to +150	−55 to +150	−55 to +150	−55 to +150	°C
T_{stg}	Storage Temperature					
	Lead Temperature during soldering, 1.6 mm (.063") from case for 10 sec max	+300	+300	+300	+300	°C

Notes:
1. V_{GS} = 0.
2. Linear Derating Factor = 0.8W/°C (see Figure 2).
3. Inductance = 100 uH, Clamp Voltage = .8 V_{DSS} (see Figures 15 & 16).
4. Typical MOS handling precautions should be observed.

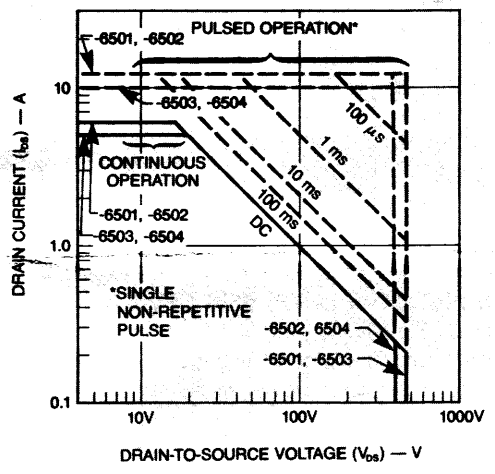


Figure 1. Safe Operating Area for All Types. (T_C = 25°C).

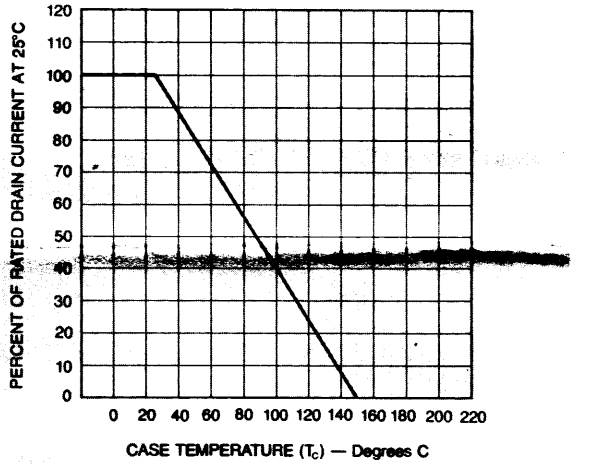


Figure 2. Derating Curve for All Types.

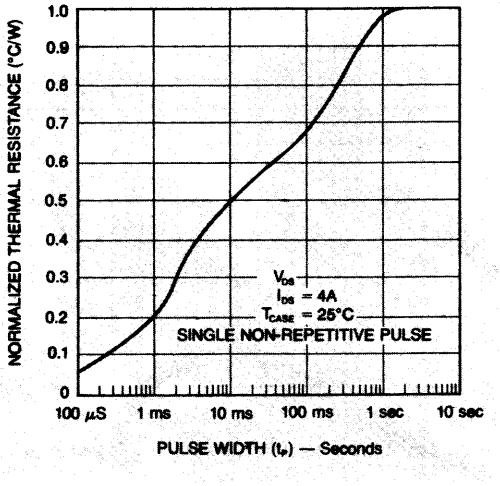


Figure 3. Typical Thermal Response Characteristics for All Types.

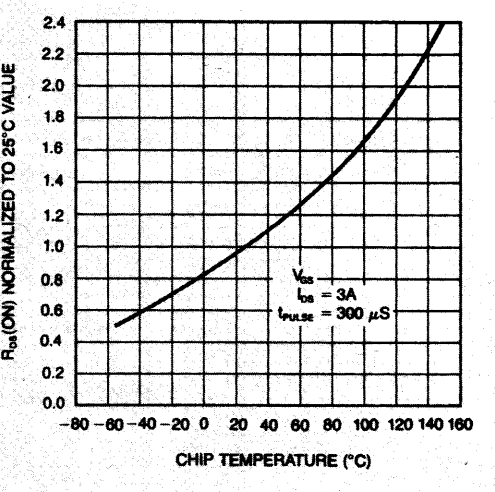


Figure 4. Typical Normalized On-Resistance Versus Chip Temperature.

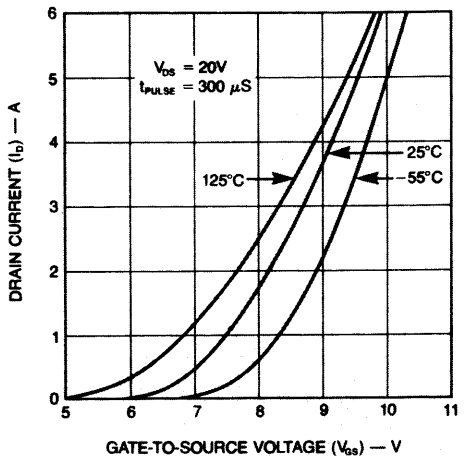


Figure 5. Typical Transfer Characteristics for All Types.

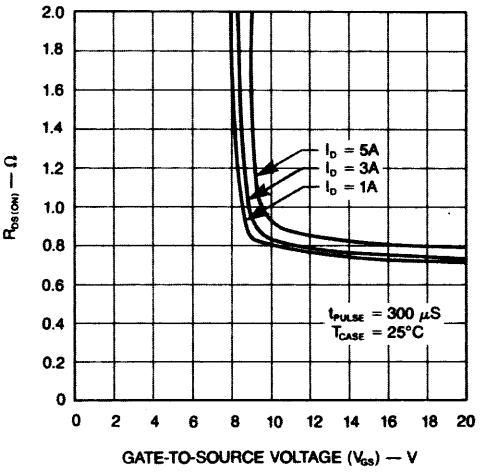


Figure 6. Typical On-Resistance Characteristics for All Types.

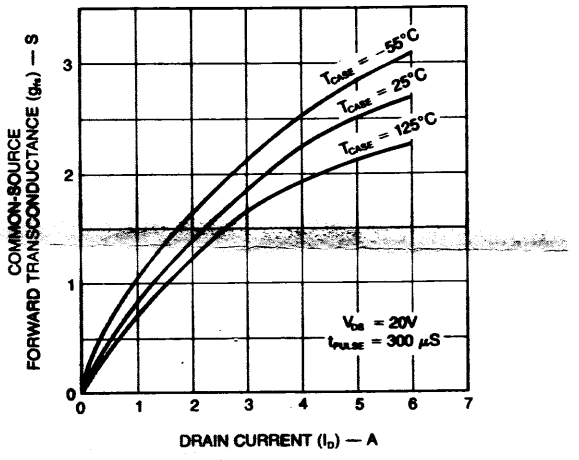


Figure 7. Typical Transconductance Versus Drain Current for All Types.

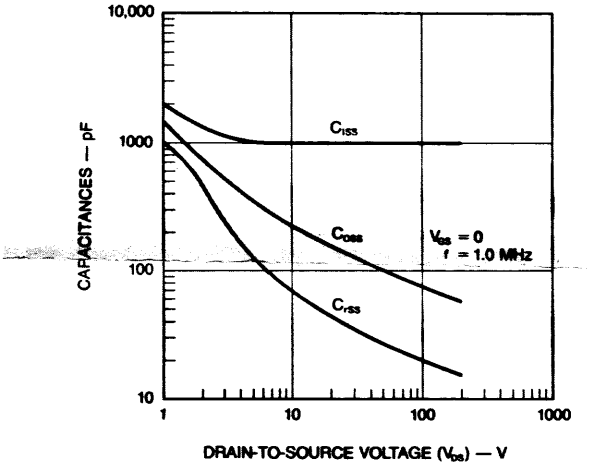


Figure 8. Typical Capacitances for All Types.

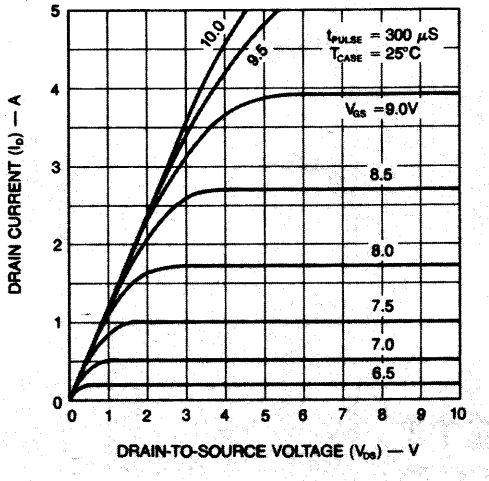


Figure 9. Typical Drain Characteristics for All Types.

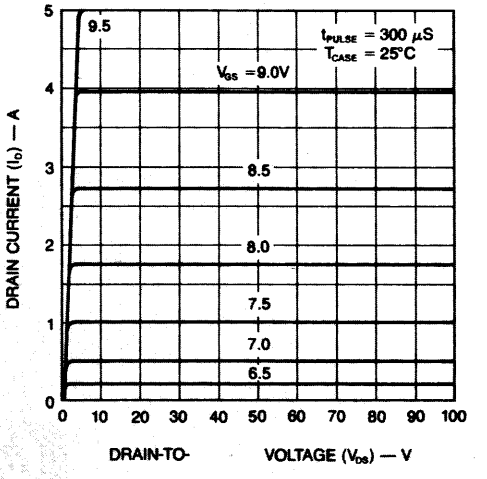


Figure 10. Typical Drain Characteristics for All Types.

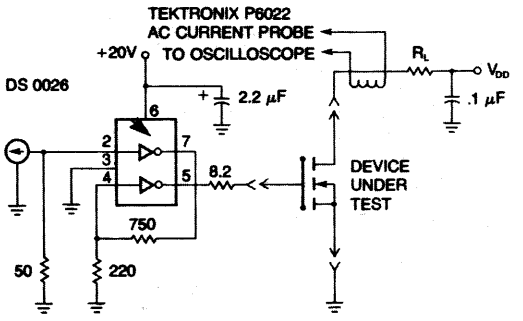


Figure 11. Switching Speed Measurement Test Circuit.

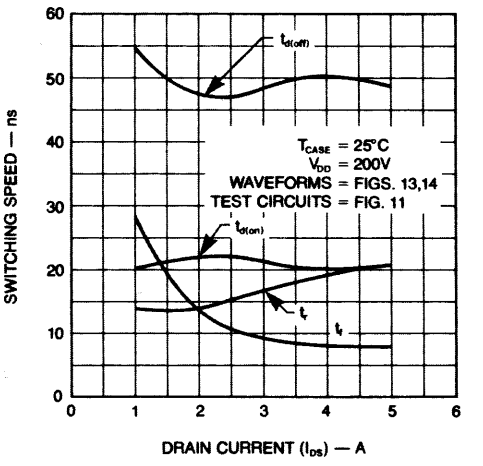


Figure 12. Typical Switching Speed Versus Drain Current for All Types.

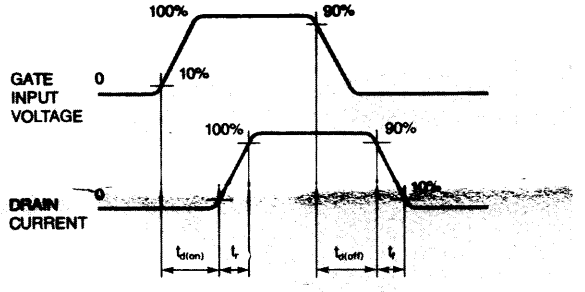


Figure 13. Definition of Switching Times.

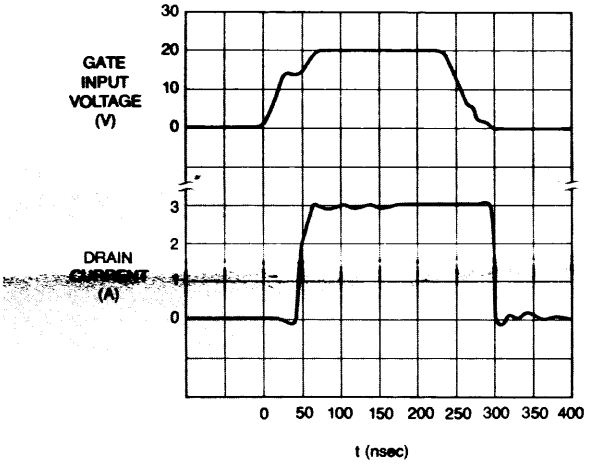


Figure 14. Typical Switching Waveforms.

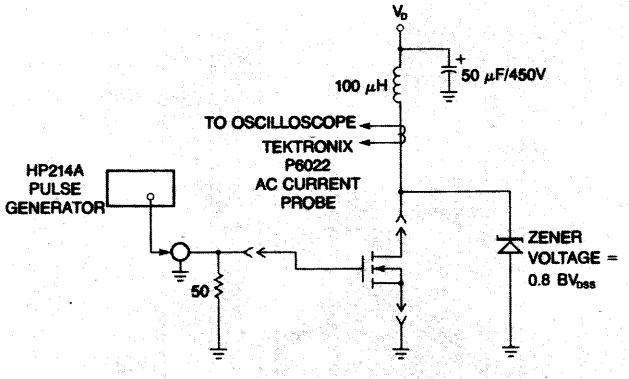


Figure 15. Circuit for Clamped Inductive Switching.

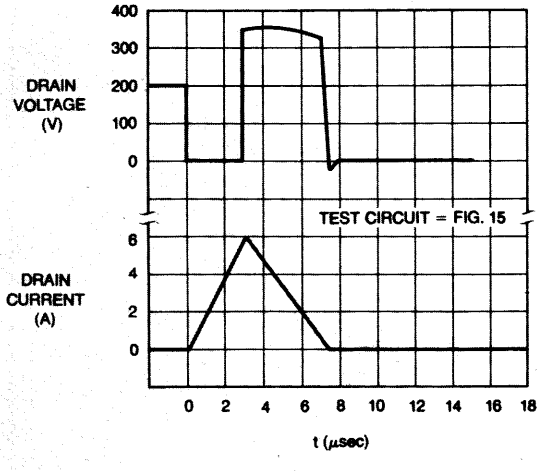
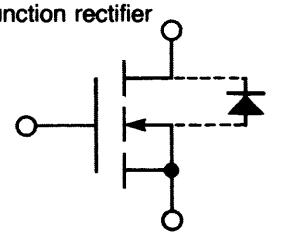


Figure 16. Typical Clamped Inductive Switching Waveforms.

Substrate-Drain Diode Ratings and Characteristics

Symbol	Parameters	HPWR-6501 HPWR-6502	HPWR-6503 HPWR-6504	Units	Test Conditions
I_{DR}	Continuous Reverse Drain Current	6	5	A max	MOSFET symbol showing reverse P-N junction rectifier 
I_{DRM}	Pulsed Reverse Drain Current	12	10	A max	
V_{SD}	Diode Forward Voltage	0.9	0.9	V typ	T_J = 25°C, $I_F = I_{DR}$, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	150	150	ns typ	T_J = 150°C, $I_F = I_{DRM}$, dI_F/dt = 100 A/μS

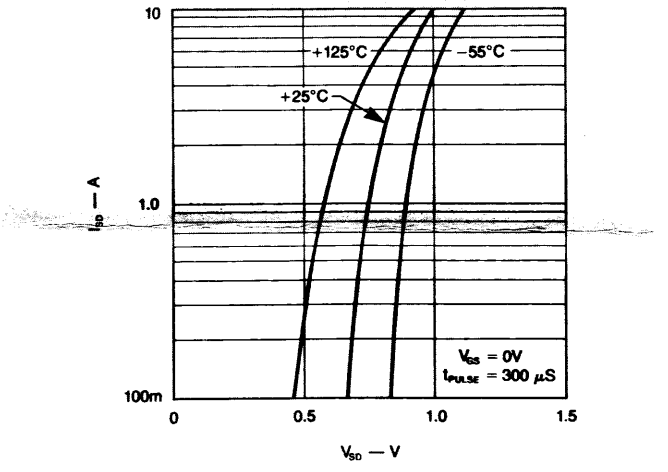


Figure 17. Typical Substrate-Drain Diode Conduction Characteristics for All Types.

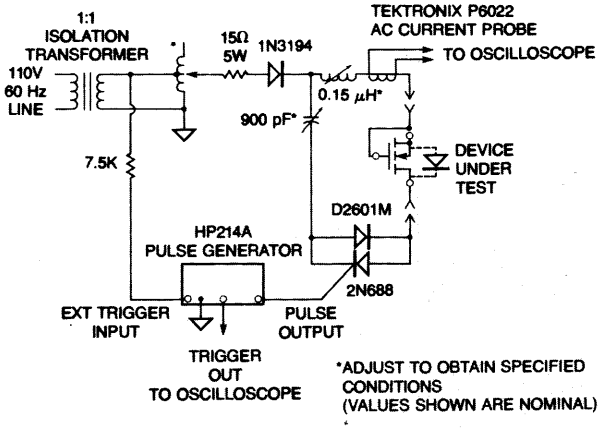


Figure 18. Substrate-Drain Diode Reverse Recovery Time Test Circuit.

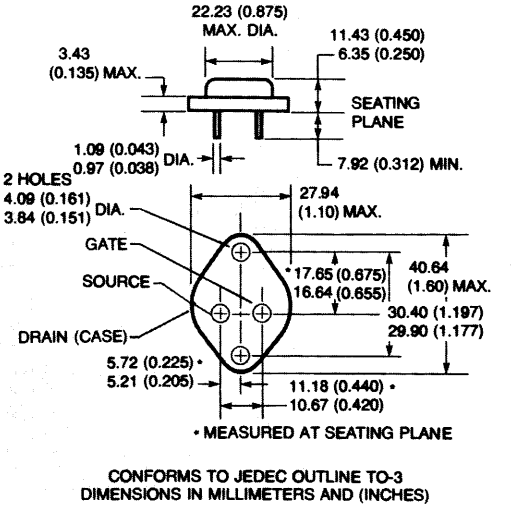


Figure 19. Package Outline.

For more information call your local HP Sales Office or East (301) 948-6370 — Midwest (312) 255-9800 — South (404) 955-1500 — West (213) 970-7500. Or write: Hewlett-Packard Components, 350 West Trimble Road, San Jose, California 95131. In Europe, Hewlett-Packard GmbH, P.O. Box 250, Herrenberger Str. 110, D-7030 Boeblingen, West Germany. In Japan, YHP, 3-29-21, Takaido-Higashi, Suginami Ku, Tokyo 168.

Printed in U.S.A. Data Subject to Change 5953-4431 (09/80)