

August 1991

Features

- 6.2A and 5.4A, 600V
- $r_{DS(on)} = 1.2\Omega$ and 1.6Ω
- Repetitive Avalanche Ratings
- Simple Drive Requirements
- Ease of Paralleling

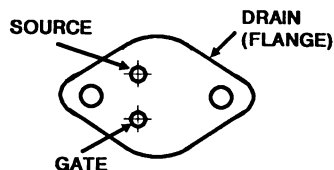
Description

The IRFAC40R and IRFAC42R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFAC types are supplied in the JEDEC TO-204AA steel package.

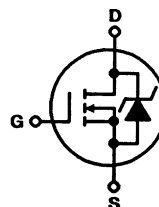
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$), Unless Otherwise Specified

	IRFAC40R	IRFAC42R	UNITS
Continuous Drain Current			
$T_C = +25^\circ\text{C}$ I_D	6.2	5.4	A
$T_C = +100^\circ\text{C}$ I_D	3.9	3.4	A
Pulsed Drain Current (1) I_{DM}	25	22	A
Gate-Source Voltage V_{GS}	± 20	± 20	V
Maximum Power Dissipation			
$T_C = +25^\circ\text{C}$ P_D	125	125	W
Linear Derating Factor θ_{JA}	1.0	1.0	W/°C
Single Pulse Avalanche Energy Rating (2) (see Figure 14) E_{AS}	570	570	mJ
Operating and Storage Junction T_J, T_{STG}	-55 to +150	-55 to +150	°C
Temperature Range			
Maximum Lead Temperature for Soldering T_L	300	300	°C
(0.063" (1.6mm) from case for 10s)			

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature (see Figure 5).
2. $V_{DD} = 50\text{V}$, Starting $T_J = +25^\circ\text{C}$, $L = 16\text{mH}$, $R_G = 25\Omega$, Peak $I_L = 6.8\text{A}$.

Specifications IRFAC40R, IRFAC42R

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS} Drain-to-Source Breakdown Voltage	IRFAC40R IRFAC42R	600	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$ Static Drain-to-Source On-State Resistance ③	IRFAC40R IRFAC42R	— —	0.97 1.2	1.2 1.6	Ω	$V_{GS} = 10V, I_D = 3.4A$
$I_{D(on)}$ On-State Drain Current ③	IRFAC40R IRFAC42R	6.2 5.4	— —	— —	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max. $V_{GS} = 10V$
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs} Forward Transconductance ③	ALL	4.7	70	—	S(U)	$V_{DS} \geq 50V, I_{DS} = 3.4A$
I_{DSS} Zero Gate Voltage Drain Current	ALL	— —	— —	250 1000	μA	$V_{DS} = \text{Max. Rating}, V_{GS} = 0V$ $V_{DS} = 0.8 \times \text{Max. Rating}, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS} Gate-to-Source Leakage Forward	ALL	—	—	100	nA	$V_{GS} = 20V$
I_{GSS} Gate-to-Source Leakage Reverse	ALL	—	—	-100	nA	$V_{GS} = -20V$
Q_g Total Gate Charge	ALL	—	40	60	nC	$V_{GS} = 10V, I_D = 6.2A$
Q_{gs} Gate-to-Source Charge	ALL	—	5.5	—	nC	$V_{DS} = 0.8 \times \text{Max. Rating}$ See Fig. 16
Q_{gd} Gate-to-Drain ("Miller") Charge	ALL	—	20	—	nC	(Independent of operating temperature)
$t_{d(on)}$ Turn-On Delay Time	ALL	—	13	20	ns	$V_{DD} = 300V, I_D = 6.2A, R_G = 9.1\Omega$
t_r Rise Time	ALL	—	18	27	ns	$R_D = 47\Omega$
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	55	83	ns	See Fig. 15
t_f Fall Time	ALL	—	20	30	ns	(Independent of operating temperature)
L_D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S Internal Source Inductance	ALL	—	13	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss} Input Capacitance	ALL	—	1300	—	pF	$V_{GS} = 0V, V_{DS} = 25V$
C_{oss} Output Capacitance	ALL	—	160	—	pF	$f = 1.0\text{MHz}$
C_{rss} Reverse Transfer Capacitance	ALL	—	30	—	pF	See Fig. 10
R_{thJC} Junction-to-Case	ALL	—	—	1.0	$^\circ\text{C/W}$	
R_{thCS} Case-to-Sink	ALL	—	0.12	—	$^\circ\text{C/W}$	Mounting surface flat, smooth, and greased
R_{thJA} Junction-to-Ambient	ALL	—	—	30	$^\circ\text{C/W}$	Typical-socket mount

Source-Drain Diode Ratings and Characteristics

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
I_S Continuous Source Current (Body Diode)	ALL	—	—	6.2	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier.
I_{SM} Pulse Source Current (Body Diode) ①	ALL	—	—	25	A	
V_{SD} Diode Forward Voltage ③	ALL	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 6.2A, V_{GS} = 0V$
t_{rr} Reverse Recovery Time	ALL	200	450	940	ns	$T_J = 25^\circ\text{C}, I_F = 6.2A, di/dt = 100A/\mu s$
Q_{RR} Reverse Recovery Charge	ALL	1.8	3.8	7.9	μC	
t_{on} Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① Repetitive Rating: Pulse width limited by maximum junction temperature (see figure 5).

② @ $V_{DD} = 50V$, Starting $T_J = 25^\circ\text{C}$,
 $L = 16\text{mH}$, $R_G = 25\Omega$,
Peak $I_L = 6.8A$

③ Pulse width $\leq 300\mu s$; Duty Cycle $\leq 2\%$

4

N-CHANNEL
POWER MOSFETS



IRFAC40R, IRFAC42R

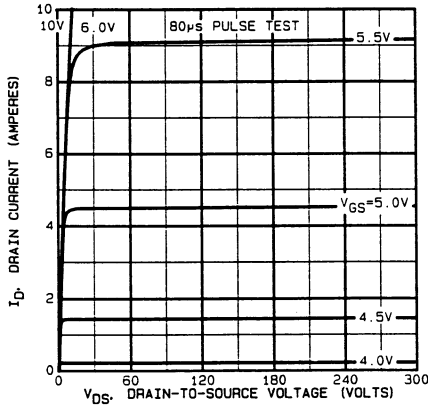


Fig. 1 - Typical Output Characteristics

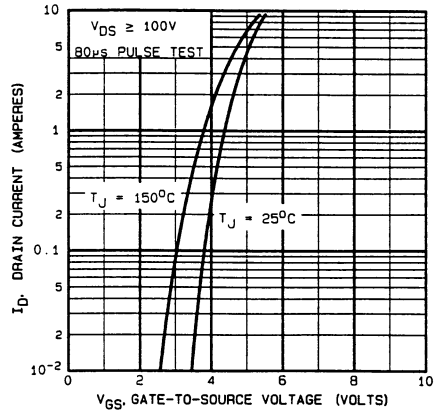


Fig. 2 - Typical Transfer Characteristics

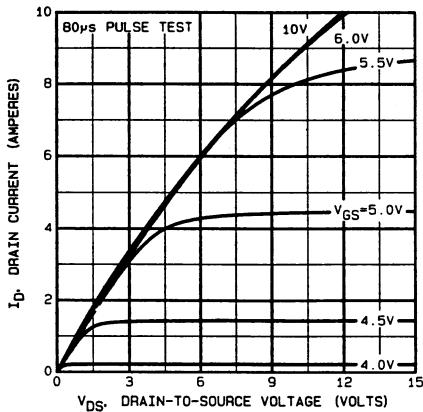


Fig. 3 - Typical Saturation Characteristics

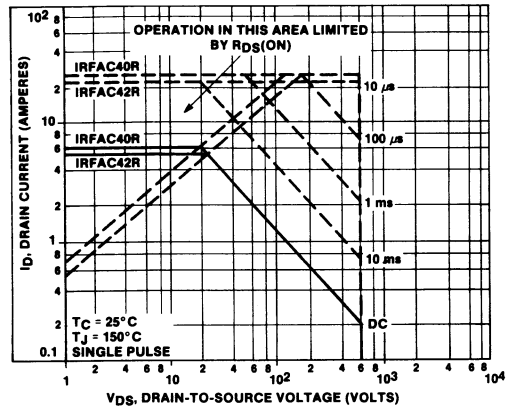


Fig. 4 - Maximum Safe Operating Area

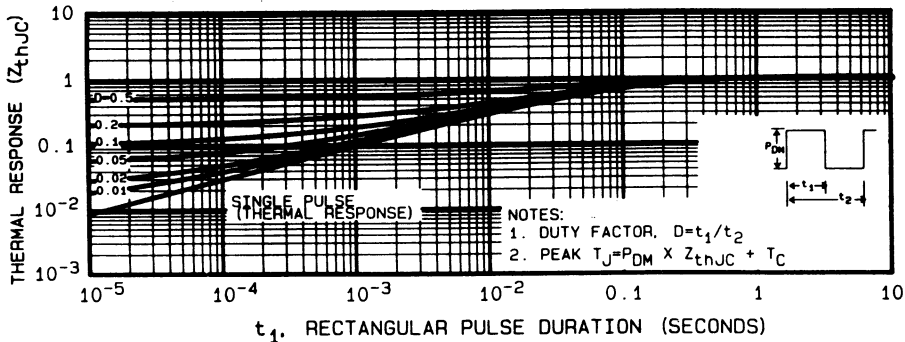


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

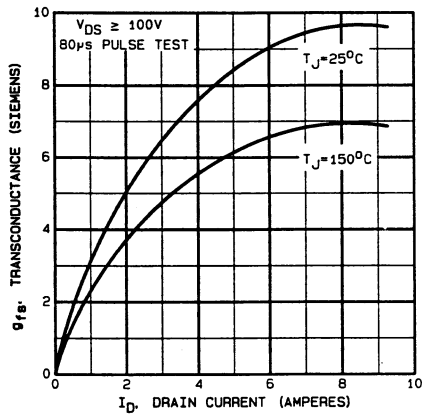


Fig. 6 - Typical Transconductance Vs. Drain Current

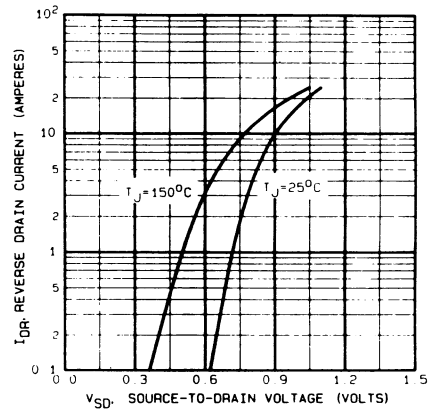


Fig. 7 - Typical Source-Drain Diode Forward Voltage

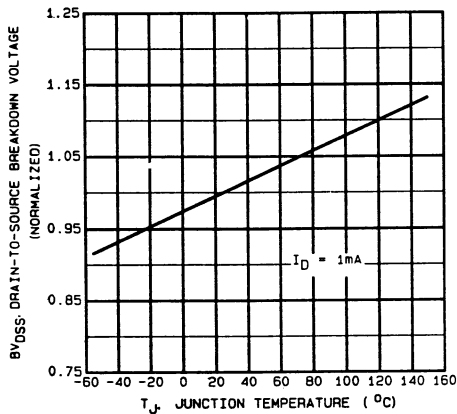


Fig. 8 - Breakdown Voltage Vs. Temperature

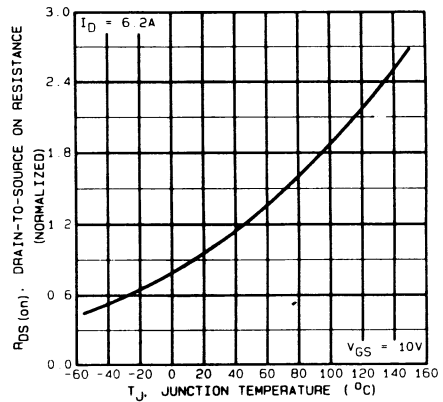


Fig. 9 - Normalized On-Resistance Vs. Temperature

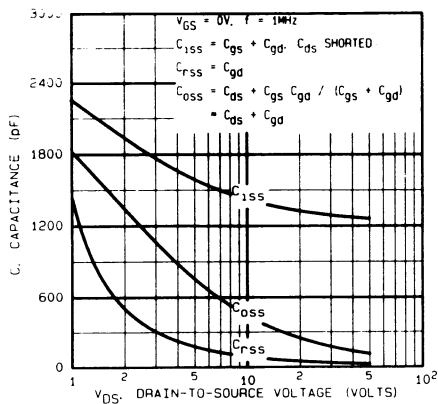


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

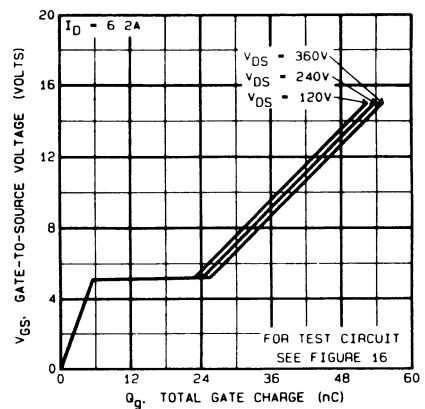


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

IRFAC40R, IRFAC42R

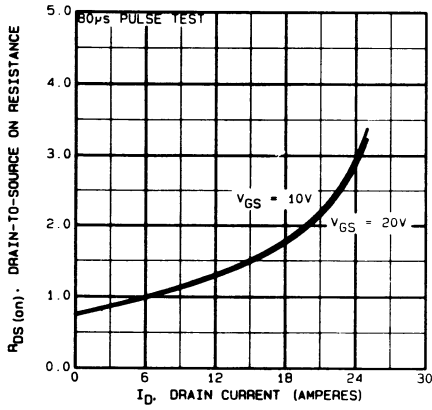


Fig. 12 - Typical On-Resistance Vs. Drain Current

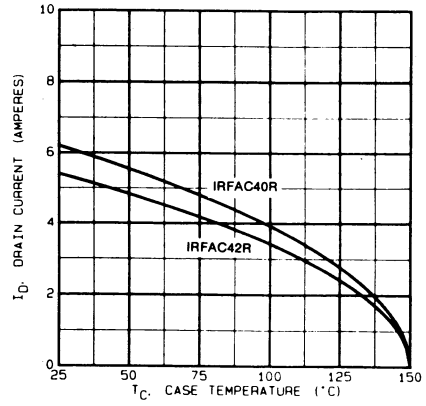


Fig. 13 - Maximum Drain Current Vs. Case Temperature

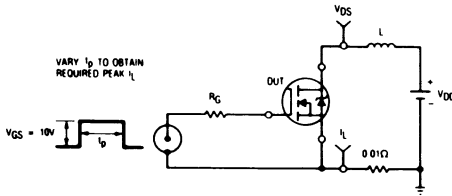


Fig. 14a - Unclamped Inductive Test Circuit

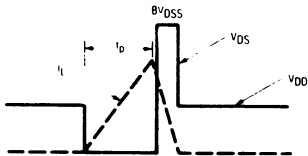


Fig. 14b - Unclamped Inductive Waveforms

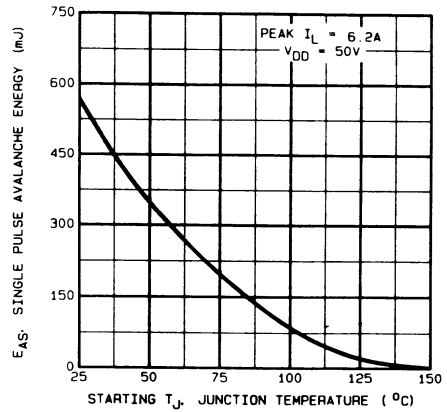


Fig. 14c - Maximum Avalanche Energy Vs. Starting Junction Temperature

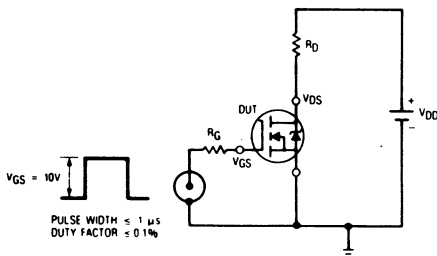


Fig. 15a - Switching Time Test Circuit

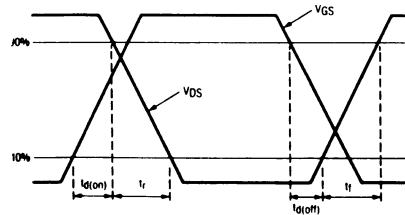


Fig. 15b - Switching Time Waveforms

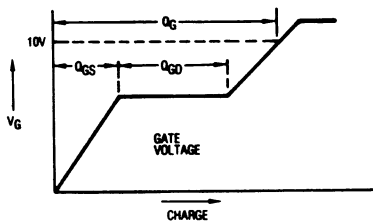


Fig. 16a - Basic Gate Charge Waveform

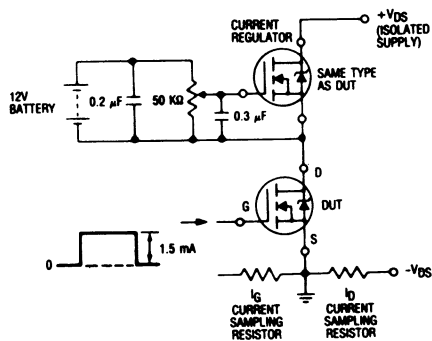


Fig. 16b - Gate Charge Test Circuit

August 1991

Features

- 6.2A and 5.4A, 600V
- $r_{DS(on)} = 1.2\Omega$ and 1.6Ω
- Repetitive Avalanche Ratings
- Simple Drive Requirements
- Ease of Paralleling

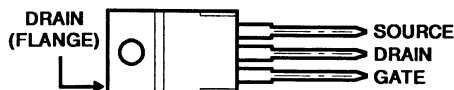
Description

The IRFBC40R and IRFBC42R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFAC types are supplied in the JEDEC TO-220AB steel package.

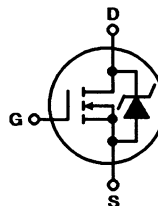
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$), Unless Otherwise Specified

	IRFBC40R	IRFBC42R	UNITS
Continuous Drain Current			
$T_C = +25^\circ\text{C}$	6.2	5.4	A
$T_C = +100^\circ\text{C}$	3.9	3.4	A
Pulsed Drain Current (1)	25	22	A
Gate-Source Voltage	± 20	± 20	V
Maximum Power Dissipation			
$T_C = +25^\circ\text{C}$	125	125	W
Linear Derating Factor	1.0	1.0	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy Rating (2) (see Figure 14)	570	570	mJ
Operating and Storage Junction Temperature Range	-55 to $+150$	-55 to $+150$	$^\circ\text{C}$
Maximum Lead Temperature for Soldering	300	300	$^\circ\text{C}$
(0.063" (1.6mm) from case for 10s)			

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature (see Figure 5).
2. $V_{DD} = 50\text{V}$, Starting $T_J = +25^\circ\text{C}$, $L = 16\text{mH}$, $R_G = 25\Omega$, Peak $I_L = 6.8\text{A}$.

Specifications IRFBC40R, IRFBC42R

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS} Drain-to-Source Breakdown Voltage	IRFBC40R IRFBC42R	600	—	—	V	$V_{GS} = 0V$, $I_D = 250\mu A$
$R_{DS(on)}$ Static Drain-to-Source On-State Resistance ③	IRFBC40R IRFBC42R	—	0.97 1.2	1.2 1.6	Ω	$V_{GS} = 10V$, $I_D = 3.4A$
$I_{D(on)}$ On-State Drain Current ③	IRFBC40R IRFBC42R	6.2 5.4	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max. $V_{GS} = 10V$
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
g_{fs} Forward Transconductance ③	ALL	4.7	70	—	S(t)	$V_{DS} \geq 100V$, $I_{DS} = 3.4A$
I_{OSS} Zero Gate Voltage Drain Current	ALL	—	—	250 1000	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0V$ $V_{DS} = 0.8 \times \text{Max. Rating}$, $V_{GS} = 0V$, $T_J = 125^\circ\text{C}$
I_{GSS} Gate-to-Source Leakage Forward	ALL	—	—	500	nA	$V_{GS} = 20V$
I_{GSS} Gate-to-Source Leakage Reverse	ALL	—	—	-500	nA	$V_{GS} = -20V$
Q_g Total Gate Charge	ALL	—	40	60	nC	$V_{DS} = 10V$, $I_D = 6.2A$ $V_{DS} = 0.7 \times \text{Max. Rating}$ See Fig. 16
Q_{gs} Gate-to-Source Charge	ALL	—	5.5	—	nC	(Independent of operating temperature)
Q_{gd} Gate-to-Drain ("Miller") Charge	ALL	—	20	—	nC	(Independent of operating temperature)
$t_{d(on)}$ Turn-On Delay Time	ALL	—	13	20	ns	$V_{DD} = 300V$, $I_D = 6.2A$, $R_G = 9.1\Omega$
t_r Rise Time	ALL	—	18	27	ns	$R_D = 47\Omega$
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	55	83	ns	See Fig. 15
t_f Fall Time	ALL	—	20	30	ns	(Independent of operating temperature)
L_D Internal Drain Inductance	ALL	—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss} Input Capacitance	ALL	—	1300	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$
C_{oss} Output Capacitance	ALL	—	160	—	pF	$f = 1.0\text{ MHz}$
C_{rss} Reverse Transfer Capacitance	ALL	—	45	—	pF	See Fig. 10
$R_{\theta JC}$ Junction-to-Case	ALL	—	—	1.0	$^\circ\text{C/W}$	
$R_{\theta CS}$ Case-to-Sink	ALL	—	0.50	—	$^\circ\text{C/W}$	Mounting surface flat, smooth, and greased
$R_{\theta JA}$ Junction-to-Ambient	ALL	—	—	80	$^\circ\text{C/W}$	Typical-socket mount

Source-Drain Diode Ratings and Characteristics

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
I_S Continuous Source Current (Body Diode)	ALL	—	—	6.2	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier.
I_{SM} Pulse Source Current (Body Diode) ①	ALL	—	—	25	A	
V_{SD} Diode Forward Voltage ③	ALL	—	—	1.5	V	$T_J = 25^\circ\text{C}$, $I_S = 6.2A$, $V_{GS} = 0V$
t_r Reverse Recovery Time	ALL	200	450	940	ns	$T_J = 25^\circ\text{C}$, $I_F = 6.2A$, $di/dt = 100A/\mu s$
Q_{RR} Reverse Recovery Charge	ALL	1.8	3.8	8.0	μC	
t_{on} Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① Repetitive Rating: Pulse width limited by maximum junction temperature (see figure 5).

② @ $V_{DD} = 50V$, Starting $T_J = 25^\circ\text{C}$,
 $L = 16mH$, $R_G = 25\Omega$,
Peak $I_L = 6.8A$

③ Pulse width $\leq 300\mu s$; Duty Cycle $\leq 2\%$



IRFBC40R, IRFBC42R

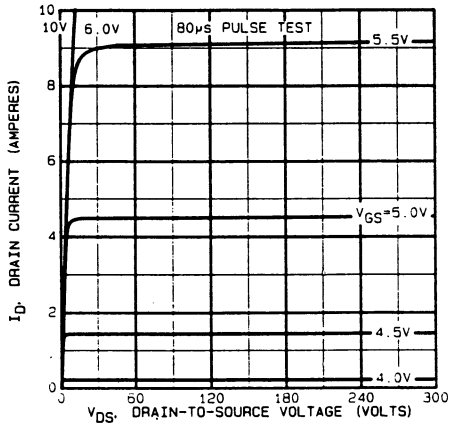


Fig. 1 - Typical Output Characteristics

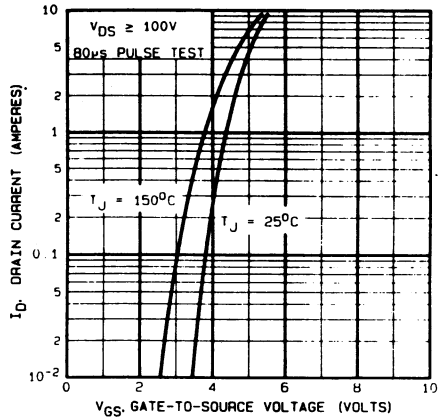


Fig. 2 - Typical Transfer Characteristics

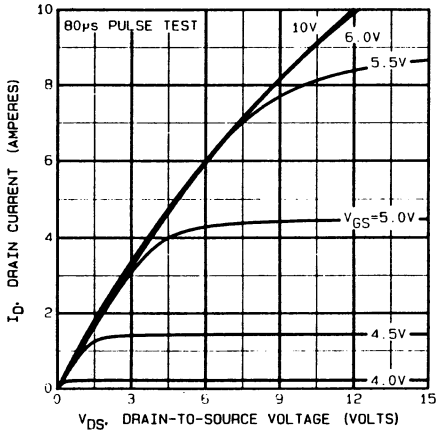


Fig. 3 - Typical Saturation Characteristics

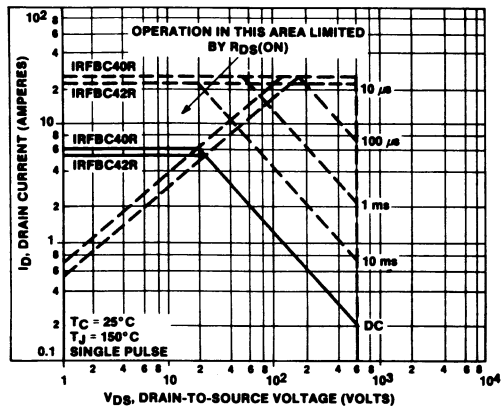


Fig. 4 - Maximum Safe Operating Area

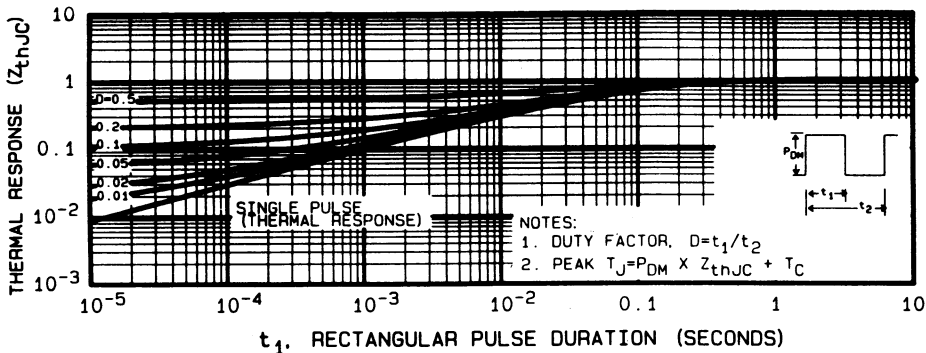


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

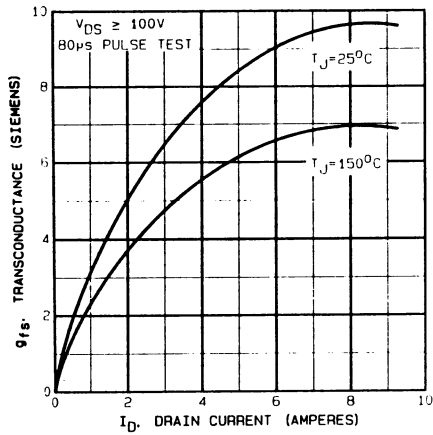


Fig. 6 - Typical Transconductance Vs. Drain Current

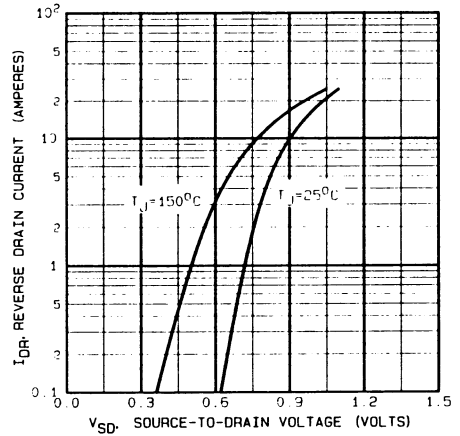


Fig. 7 - Typical Source-Drain Diode Forward Voltage

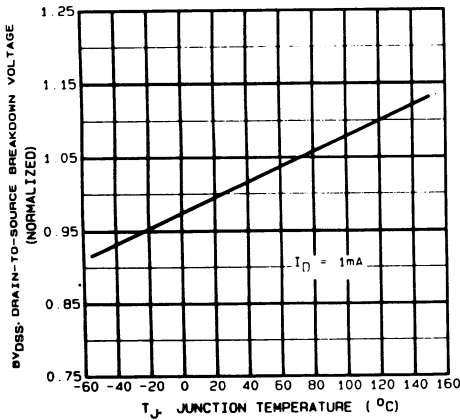


Fig. 8 - Breakdown Voltage Vs. Temperature

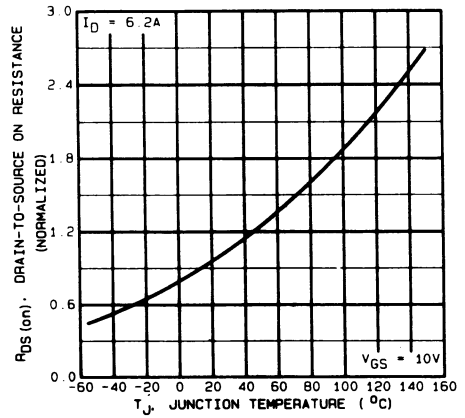


Fig. 9 - Normalized On-Resistance Vs. Temperature

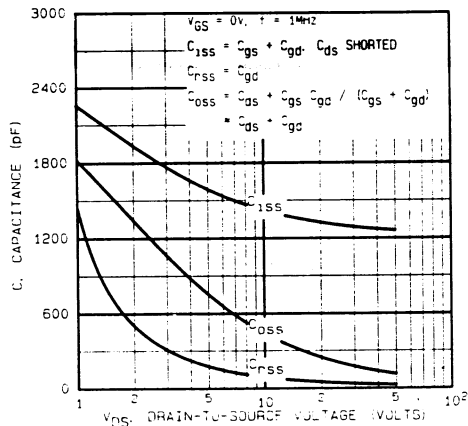


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

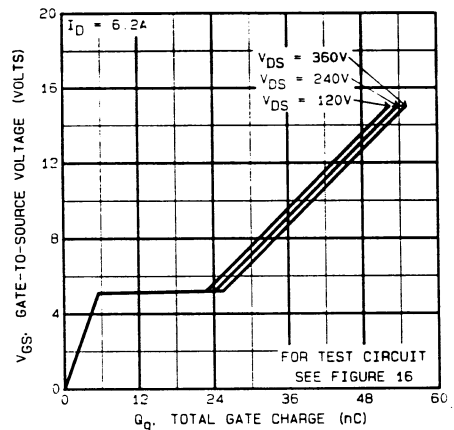


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

IRFBC40R, IRFBC42R

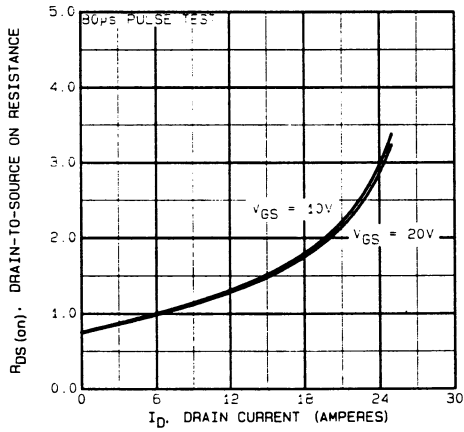


Fig. 12 - Typical On-Resistance Vs. Drain Current

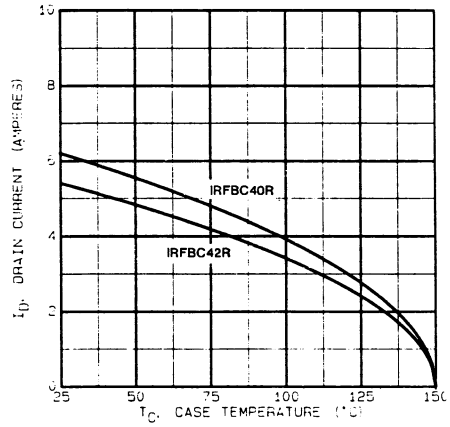


Fig. 13 - Maximum Drain Current Vs. Case Temperature

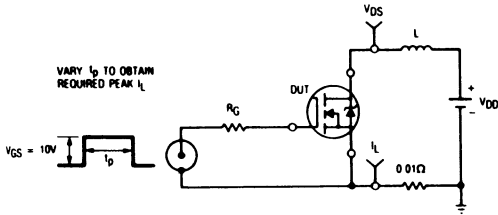


Fig. 14a - Unclamped Inductive Test Circuit

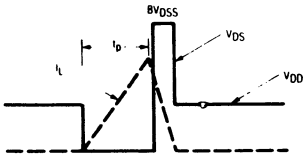


Fig. 14b - Unclamped Inductive Waveforms

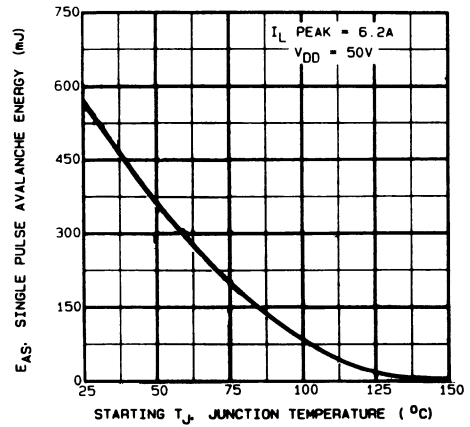


Fig. 14c - Maximum Avalanche Energy Vs. Starting Junction Temperature

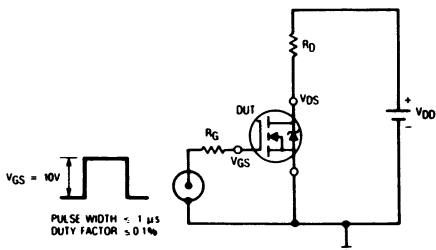


Fig. 15a - Switching Time Test Circuit

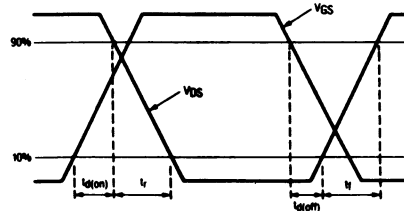


Fig. 15b - Switching Time Waveforms