HARRIS

IRFD2Z0, IRFD2Z1 IRFD2Z2, IRFD2Z3

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 0.30A and 0.32A, 150V - 200V
- $r_{DS(on)}$ = 5.0Ω and 6.5Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Description

The IRFD2Z0, IRFD2Z1, IRFD2Z2, and IRFD2Z3 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

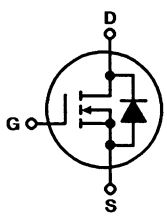
The IRFD types are supplied in the 4-pin DIP package.

Package

4-PIN DIP
TOP VIEW

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFD2Z0	IRFD2Z1	IRFD2Z2	IRFD2Z3	UNITS
Drain-Source Voltage (1)	V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	200	150	200	150	V
Continuous Drain Current T_C = +25°C	I_D	0.32	0.32	0.30	0.30	A
Pulsed Drain Current	I_{DM}	1.5	1.5	1.4	1.4	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C (See Figure 13)	P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 13)		0.008	0.008	0.008	0.008	W/°C
Inductive Current, Clamped (3)	I_{LM}	1.5	1.5	1.4	1.4	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. See Figures 14 and 15. L = 100μH

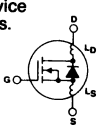
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **2329.1**

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRFD2Z0 IRFD2Z2	200	—	—	V	V_{GS} = 0 V
		IRFD2Z1 IRFD2Z3	150	—	—	V	I_D = 250 μA
Gate Threshold Voltage	$V_{GS(th)}$	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	500	nA	V_{GS} = 20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	-500	nA	V_{GS} = -20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_{D(on)}$	IRFD2Z0 IRFD2Z1	0.32	—	—	A	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, V_{GS} = -10 V
		IRFD2Z2 IRFD2Z3	0.30	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS(on)}$	IRFD2Z0 IRFD2Z1	—	4.6	5.0	Ω	V_{GS} = 10 V, I_D = 0.15 A
		IRFD2Z2 IRFD2Z3	—	5.7	6.5	Ω	
Forward Transconductance ②	g_{fs}	ALL	0.06	0.11	—	S(℧)	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, I_D = 0.15 A
Input Capacitance	C_{iss}	ALL	—	37	—	pF	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz See Fig. 9
Output Capacitance	C_{oss}	ALL	—	15	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	4.0	—	pF	
Turn-On Delay Time	$t_{d(on)}$	ALL	—	15	—	ns	$V_{DD} \simeq 0.5\ BV_{DSS}$, I_D = 0.15 A, Z_O = 50 Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	10	—	ns	
Turn-Off Delay Time	$t_{d(off)}$	ALL	—	22	—	ns	
Fall Time	t_f	ALL	—	28	—	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	2.5	4.0	nC	V_{GS} = 10 V, I_D = 1.5 A, V_{DS} = 0.8 V Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	1.5	—	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	1.5	—	nC	
Internal Drain Inductance	L_D	ALL	—	4.0	—	nH	Measured from the drain lead, 2.0 mm (0.08 in.) from package to center of die.
Internal Source Inductance	L_S	ALL	—	6.0	—	nH	Measured from the source lead, 2.0 mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

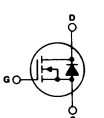


THERMAL RESISTANCE

Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	120	°C/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRFD2Z0 IRFD2Z1	—	—	0.32	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD2Z2 IRFD2Z3	—	—	0.30	A	
Pulse Source Current (Body Diode)	I_{SM}	IRFD2Z0 IRFD2Z1	—	—	1.5	A	
		IRFD2Z2 IRFD2Z3	—	—	1.4	A	
Diode Forward Voltage ②	V_{SD}	IRFD2Z0 IRFD2Z1	—	—	1.3	V	T_C = 25°C, I_S = 0.32 A, V_{GS} = 0 V
		IRFD2Z2 IRFD2Z3	—	—	1.3	V	T_C = 25°C, I_S = 0.30 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	—	125	—	ns	T_J = 150°C, I_F = 0.30 A, dI_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	—	0.2	—	μC	T_J = 150°C, I_F = 0.30 A, dI_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25° C to 150° C.
② Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%.
③ (See Fig. 14 and 15) L = 100 μH

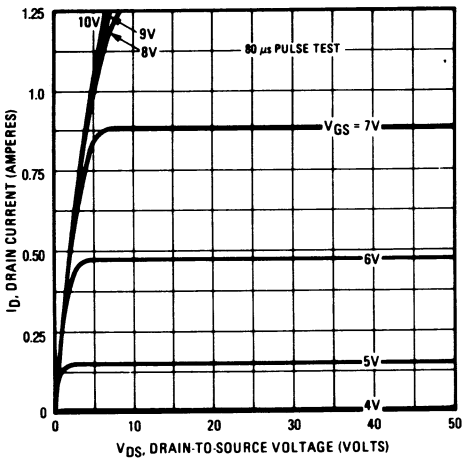


Fig. 1 – Typical Output Characteristics

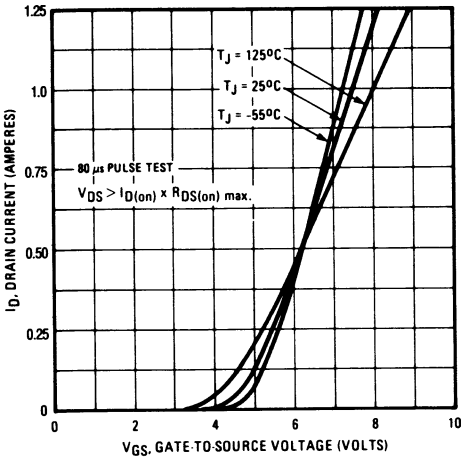


Fig. 2 – Typical Transfer Characteristics

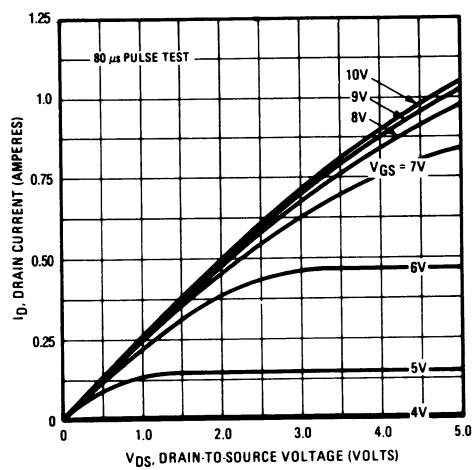


Fig. 3 – Typical Saturation Characteristics

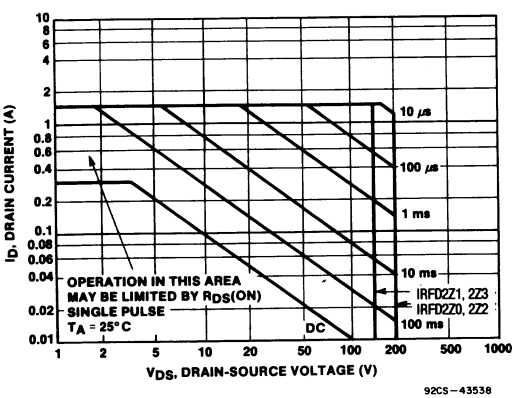


Fig. 4 – Maximum Safe Operating Area

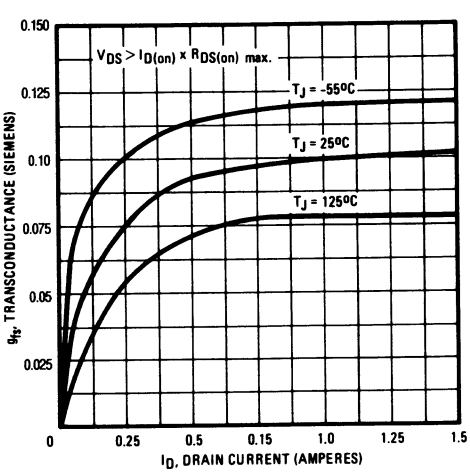


Fig. 5 – Typical Transconductance Vs. Drain Current

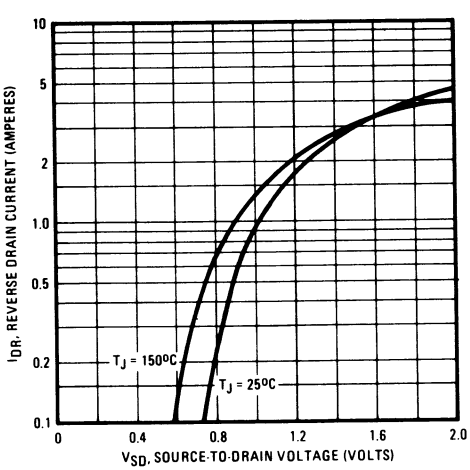


Fig. 6 – Typical Source-Drain Diode Forward Voltage

4 N-CHANNEL POWER MOSFETs

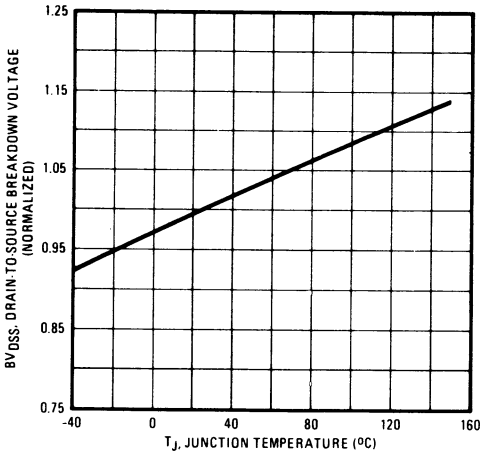


Fig. 7 – Breakdown Voltage Vs. Temperature

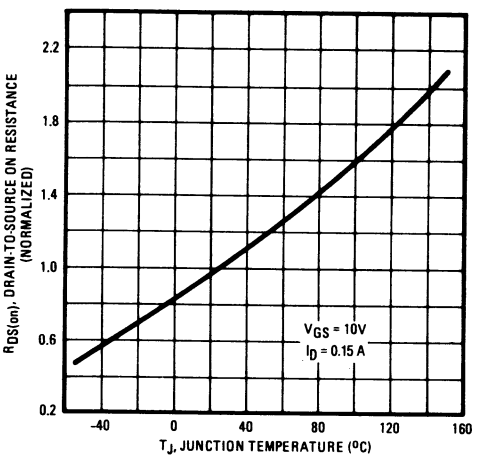


Fig. 8 – Normalized On-Resistance Vs. Temperature

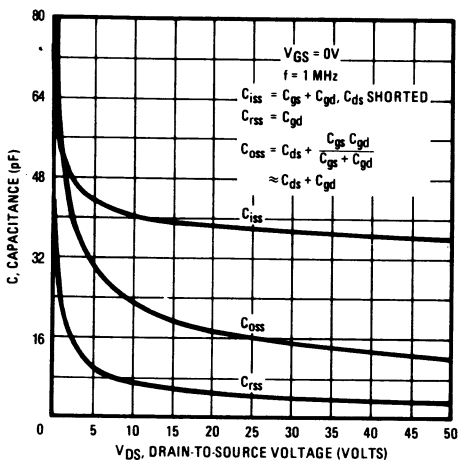


Fig. 9 – Typical Capacitance Vs. Drain-to-Source Voltage

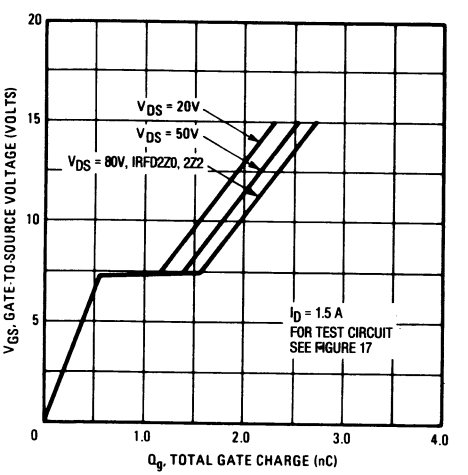


Fig. 10 – Typical Gate Charge Vs. Gate-to-Source Voltage

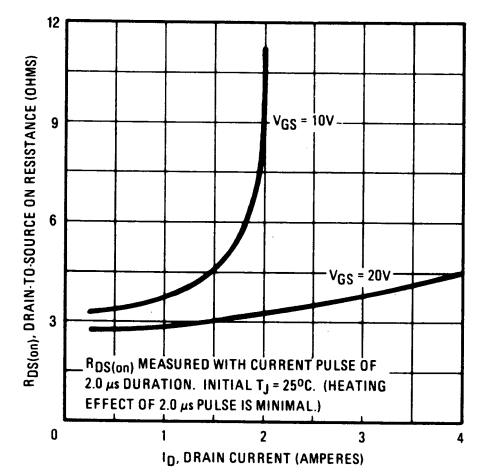


Fig. 11 – Typical On-Resistance Vs. Drain Current

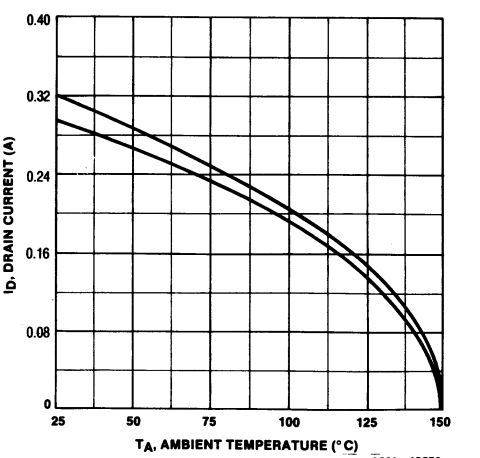


Fig. 12 – Maximum Drain Current Vs. Case Temperature

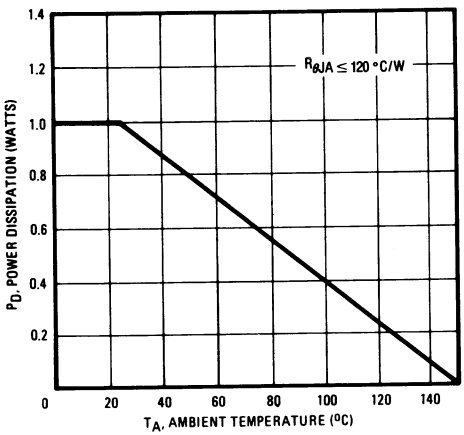


Fig. 13 – Power Vs. Temperature Derating Curve

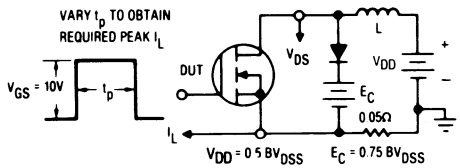


Fig. 14 — Clamped Inductive Test Circuit

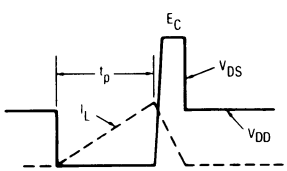


Fig. 15 — Clamped Inductive Waveforms

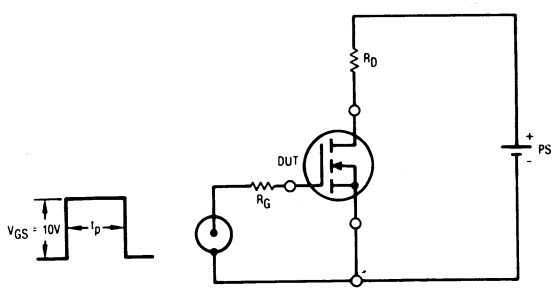


Fig. 16 – Switching Time Test Circuit

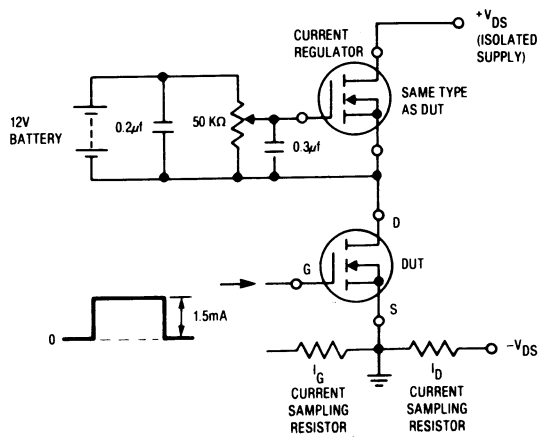


Fig. 17 — Gate Charge Test Circuit