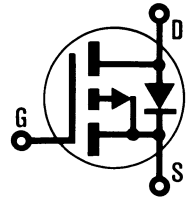
INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRFD9110 IRFD9113

P-CHANNEL HEXDIP™

1-WATT RATED POWER MOSFETs
IN A 4-PIN, DUAL-IN-LINE PACKAGE



-100 Volt, 1.2 Ohm, 1-Watt HEXDIP

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P-Channel HEXFETs are designed for application which require the convenience of reverse polarity operation. They retain all of the features of the more common N-Channel HEXFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and excellent temperature stability. the P-Channel IRFD9110 device is an approximate electrical complement to the N-Channel IRFD1Z0 HEXFET.

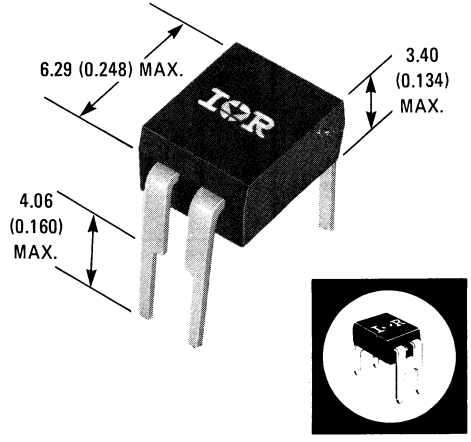
P-Channel HEXFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

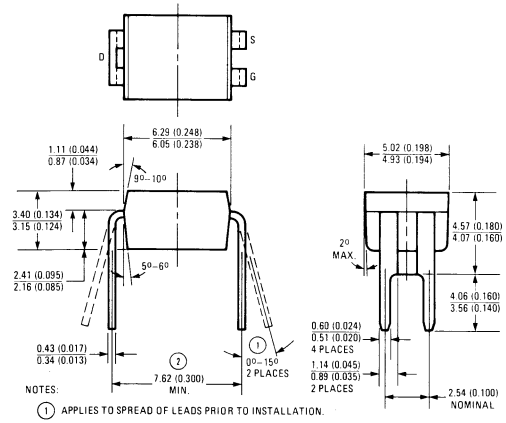
- P-Channel Versatility
- For Automatic Insertion
- Compact, End Stackable
- Fast Switching
- Low Drive Current
- Easily Paralleled
- No Second Breakdown
- Excellent Temperature Stability

Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFD9110	-100V	1.2Ω	-0.7A
IRFD9113	-60V	1.6Ω	-0.6A

CASE STYLE AND DIMENSIONS





NOTES:
1. APPLIES TO SPREAD OF LEADS PRIOR TO INSTALLATION.
2. APPLIES TO INSTALLED LEAD CENTERS.

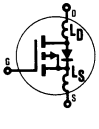
Case Style HD-1 (Similar to JEDEC Outline MO-001AN)
Dimensions in Millimeters and (Inches)

IRFD9110, IRFD9113 Devices

Absolute Maximum Ratings

	Parameter	IRFD9110	IRFD9113	Units
V_{DS}	Drain — Source Voltage ①	−100	−60	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 20 kΩ) ①	−100	−60	V
I_D @ T_A = 25°C	Continuous Drain Current	−0.7	−0.6	A
I_{DM}	Pulsed Drain Current	−3.0	−2.5	A
V_{GS}	Gate — Source Voltage	± 20		V
P_D @ T_A = 25°C	Max. Power Dissipation	1.0 (See Fig. 13)		W
	Linear Derating Factor	0.01 (See Fig. 13)		W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 14 and 15) L = 100μH −3.0	−2.5	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150		°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C

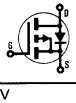
Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV_{DSS}	Drain — Source Breakdown Voltage	IRFD9110	−100	—	—	V	V_{GS} = 0V	
		IRFD9113	−60	—	—	V	I_D = −250μA	
$V_{GS(th)}$	Gate Threshold Voltage	ALL	−2.0	—	−4.0	V	V_{DS} = V_{GS}, I_D = −250μA	
I_{GSS}	Gate — Source Leakage Forward	ALL	—	—	−500	nA	V_{GS} = −20V	
I_{GSS}	Gate — Source Leakage Reverse	ALL	—	—	500	nA	V_{GS} = 20V	
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	−250	μA	V_{DS} = Max. Rating, V_{GS} = 0V	
			—	—	−1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C	
$I_{D(on)}$	On-State Drain Current ②	IRFD9110	−0.7	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = −10V	
		IRFD9113	−0.6	—	—	A		
$R_{DS(on)}$	Static Drain — Source On-State Resistance ②	IRFD9110	—	1.0	1.2	Ω	V_{GS} = −10V, I_D = −0.3A	
		IRFD9113	—	1.2	1.6	Ω		
g_{fs}	Forward Transconductance ②	ALL	0.6	0.8	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = −0.3A	
C_{iss}	Input Capacitance	ALL	—	180	250	pF	V_{GS} = 0V, V_{DS} = −25V, f = 1.0 MHz See Fig. 9	
C_{oss}	Output Capacitance	ALL	—	85	100	pF		
C_{rss}	Reverse Transfer Capacitance	ALL	—	30	35	pF		
$t_{d(on)}$	Turn-On Delay Time	ALL	—	15	30	ns	V_{DD} ≈ 0.5 I_D = −0.3A, Z_o = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)	
t_r	Rise Time	ALL	—	30	60	ns		
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	20	40	ns		
t_f	Fall Time	ALL	—	20	40	ns		
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	11	15	nC	V_{GS} = −15V, I_D = −1.5A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q_{gs}	Gate-Source Charge	ALL	—	5.7	—	nC		
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	5.3	—	nC		
L_D	Internal Drain Inductance	ALL	—	4.0	—	nH	Measured from the drain lead, 2.0mm (0.08 in.) from header to center of die.	Modified MOSFET symbol showing the internal device inductances. 
L_S	Internal Source Inductance	ALL	—	6.0	—	nH	Measured from the source lead, 2.0mm (0.08 in.) from header to source bonding pad.	

Thermal Resistance

R_{thJA}	Junction-to-Ambient	ALL	—	—	120	K/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD9110	—	—	−0.7	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRFD9113	—	—	−0.6	A	
I_{SM}	Pulse Source Current (Body Diode)	IRFD9110	—	—	−3.0	A	
		IRFD9113	—	—	−2.5	A	
V_{SD}	Diode Forward Voltage ②	IRFD9110	—	—	−5.5	V	T_C = 25°C, I_S = −0.7A, V_{GS} = 0V
		IRFD9113	—	—	−5.3	V	T_C = 25°C, I_S = −0.6A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	120	—	ns	T_J = 150°C, I_F = −0.7A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	6.0	—	μC	T_J = 150°C, I_F = −0.7A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

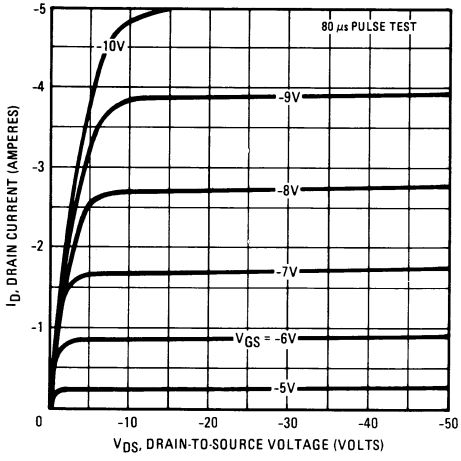


Fig. 1 — Typical Output Characteristics

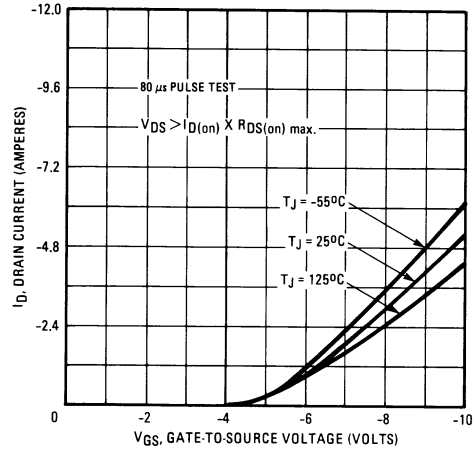


Fig. 2 — Typical Transfer Characteristics

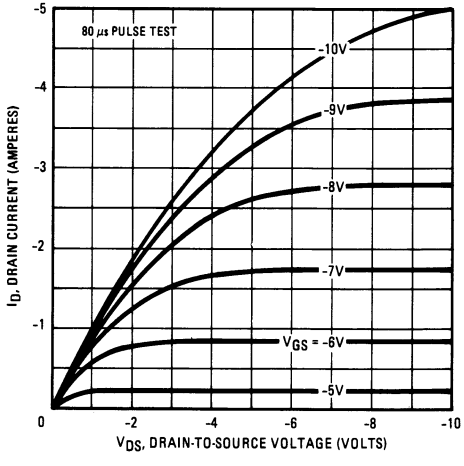


Fig. 3 — Typical Saturation Characteristics

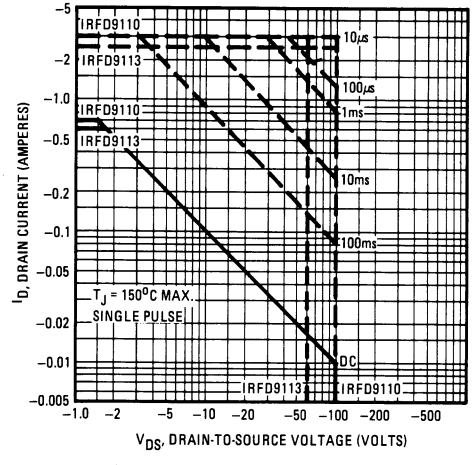


Fig. 4 — Maximum Safe Operating Area

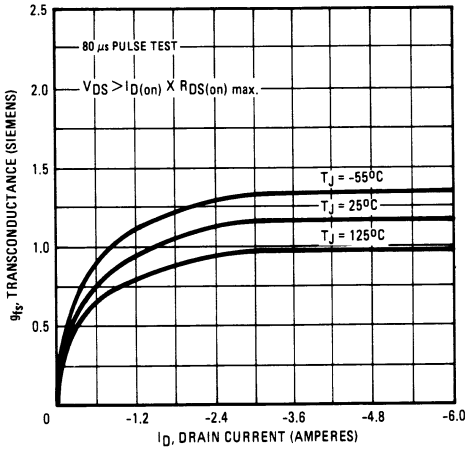


Fig. 5 – Typical Transconductance Vs. Drain Current

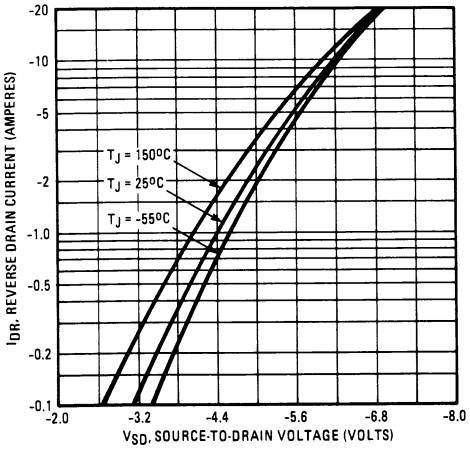


Fig. 6 – Typical Source-Drain Diode Forward Voltage

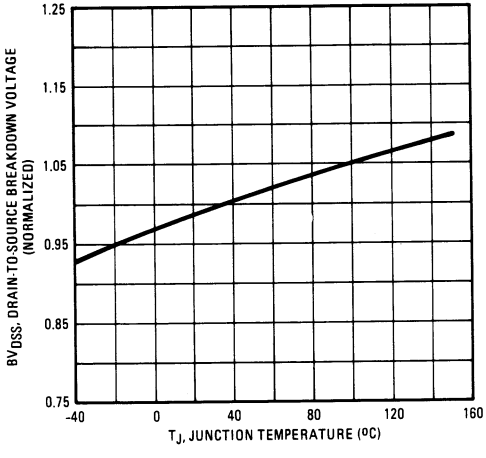


Fig. 7 – Breakdown Voltage Vs. Temperature

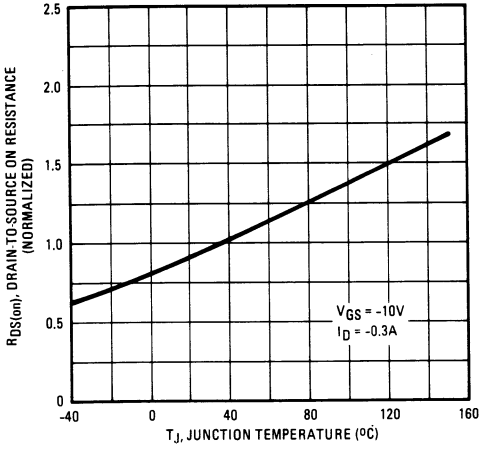


Fig. 8 – Normalized On-Resistance Vs. Temperature

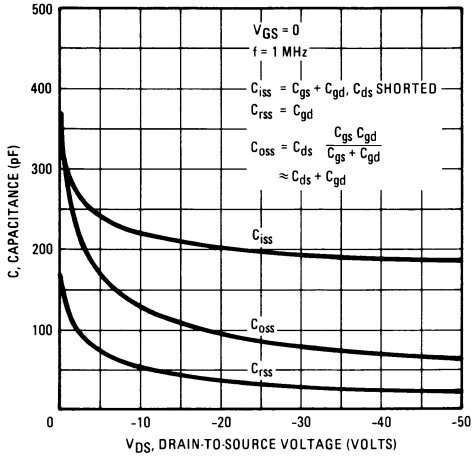


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

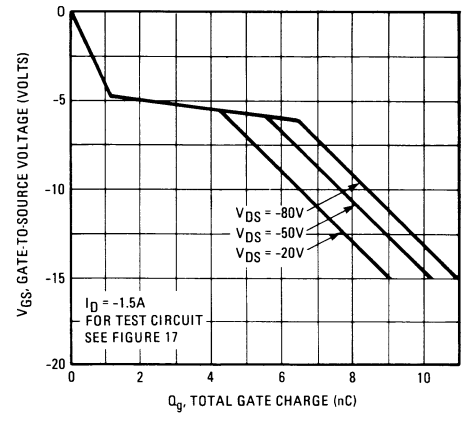


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

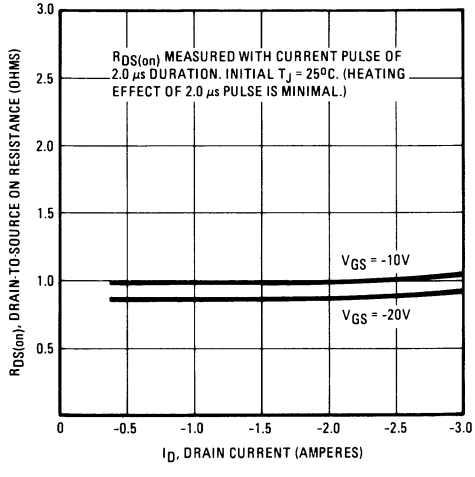


Fig. 11 — Typical On-Resistance Vs. Drain Current

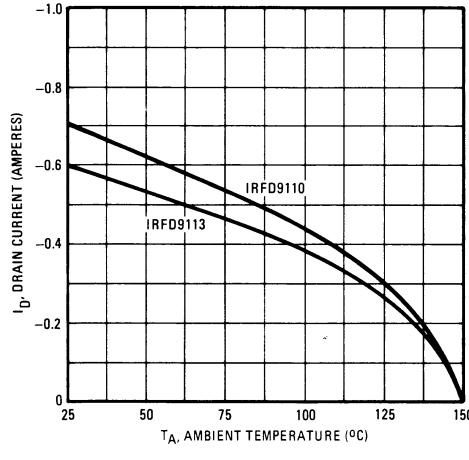


Fig. 12 — Maximum Drain Current Vs. Case Temperature

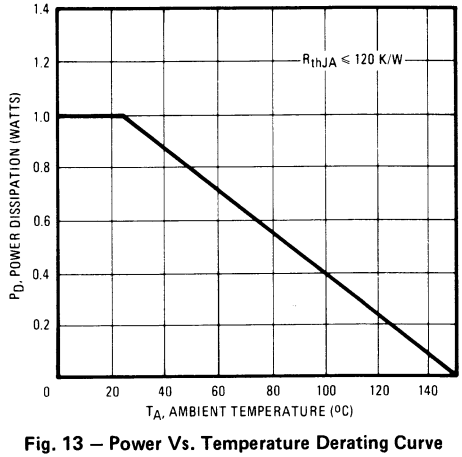


Fig. 13 — Power Vs. Temperature Derating Curve

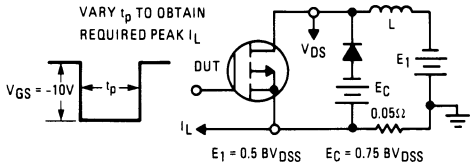


Fig. 14 — Clamped Inductive Test Circuit

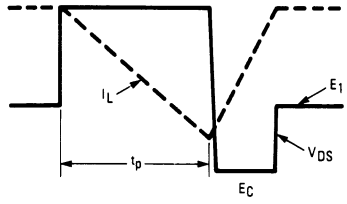


Fig. 15 — Clamped Inductive Waveforms

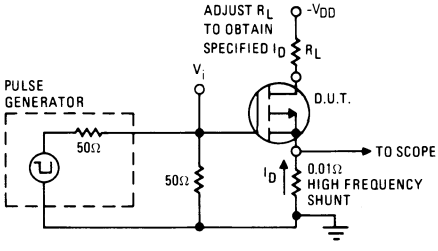


Fig. 16 — Switching Time Test Circuit

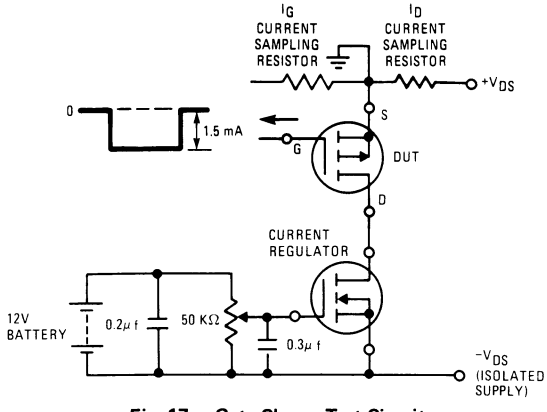


Fig. 17 — Gate Charge Test Circuit

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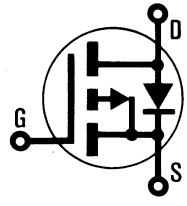
HEXFET® TRANSISTORS IRFD9210 IRFD9213

P-CHANNEL HEXDIP™

1-WATT RATED POWER MOSFETs
IN A 4-PIN, DUAL-IN-LINE PACKAGE



-200 Volt, 3.0 Ohm, 1-Watt HEXDIP

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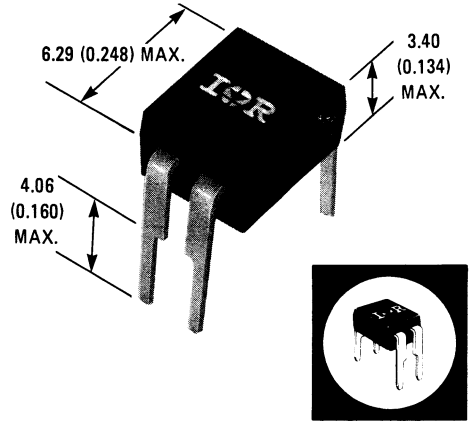
P-Channel HEXFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters,control circuits, and pulse amplifiers.

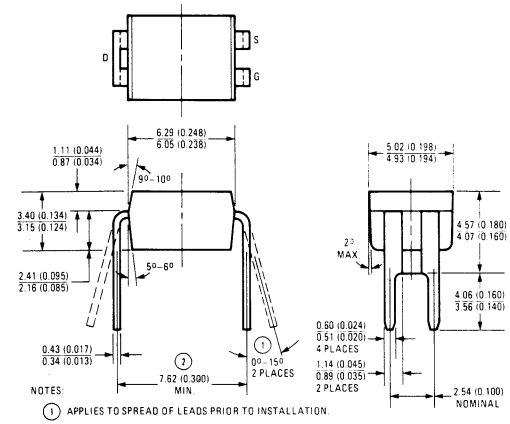
- P-Channel Versatility
- For Automatic Insertion
- Compact, End Stackable
- Fast Switching
- Low Drive Current
- Easily Paralleled
- No Second Breakdown
- Excellent Temperature Stability

Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFD9210	-200V	3.0Ω	-0.4A
IRFD9213	-150V	4.5Ω	-0.3A

CASE STYLE AND DIMENSIONS





NOTES:
1. APPLIES TO SPREAD OF LEADS PRIOR TO INSTALLATION.
2. APPLIES TO INSTALLED LEAD CENTERS.

Case Style HD-1 (Similar to JEDEC Outline MO-001AN)
Dimensions in Millimeters and (Inches)

IRFD9210, IRFD9213 Devices

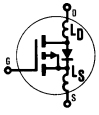
Absolute Maximum Ratings

Parameter		IRFD9210	IRFD9213	Units
V_{DS}	Drain — Source Voltage ①	−200	−150	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 20 kΩ)①	−200	−150	V
I_D @ T_A = 25°C	Continuous Drain Current	−0.4	−0.3	A
I_{DM}	Pulsed Drain Current	−1.6	−1.2	A
V_{GS}	Gate — Source Voltage	±20		V
P_D @ T_A = 25°C	Max. Power Dissipation	1.0 (See Fig. 13)		W
	Linear Derating Factor	0.008 (See Fig. 13)		W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 14 and 15) L = 100μH −1.6	−1.2	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150		°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRFD9210	−200	—	—	V	V_{GS} = 0V
		IRFD9213	−150	—	—	V	I_D = −250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	−2.0	—	−4.0	V	V_{DS} = V_{GS}, I_D = −250μA
I_{GSS}	Gate — Source Leakage Forward	ALL	—	—	−500	nA	V_{GS} = −20V
I_{GSS}	Gate — Source Leakage Reverse	ALL	—	—	500	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	−250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	−1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFD9210	−0.4	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = −10V
		IRFD9213	−0.3	—	—	A	
$R_{DS(on)}$	Static Drain — Source On-State Resistance ②	IRFD9210	—	2.3	3.0	Ω	V_{GS} = −10V, I_D = −0.3A
		IRFD9213	—	3.5	4.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.9	1.3	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = −0.3A
C_{iss}	Input Capacitance	ALL	—	170	300	pF	V_{GS} = 0V, V_{DS} = −25V, f = 1.0 MHz See Fig. 9
C_{oss}	Output Capacitance	ALL	—	50	100	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	15	35	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	8.0	15	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = −0.3A, Z_o = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	10	15	ns	
t_f	Fall Time	ALL	—	8.0	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	8.0	11	nC	V_{GS} = −15V, I_D = −3.5A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	5.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	4.0	—	nH	Measured from the drain lead, 2.0mm (0.08 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	—	6.0	—	nH	Measured from the source lead, 2.0mm (0.08 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJA}	Junction-to-Ambient	ALL	—	—	120	K/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD9210	—	—	−0.4	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD9213	—	—	−0.3	A	
I_{SM}	Pulse Source Current (Body Diode)	IRFD9210	—	—	−1.6	A	
		IRFD9213	—	—	−1.2	A	
V_{SD}	Diode Forward Voltage ②	IRFD9210	—	—	−5.8	V	T_C = 25°C, I_S = −0.4A, V_{GS} = 0V
		IRFD9213	—	—	−5.5	V	T_C = 25°C, I_S = −0.3A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	240	—	ns	T_J = 150°C, I_F = −0.4A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	1.7	—	μC	T_J = 150°C, I_F = −0.4A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

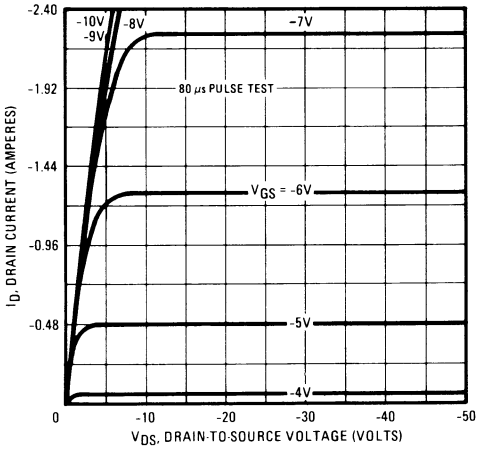


Fig. 1 — Typical Output Characteristics

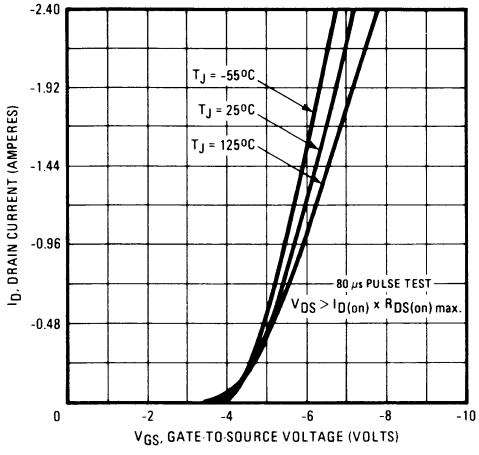


Fig. 2 — Typical Transfer Characteristics

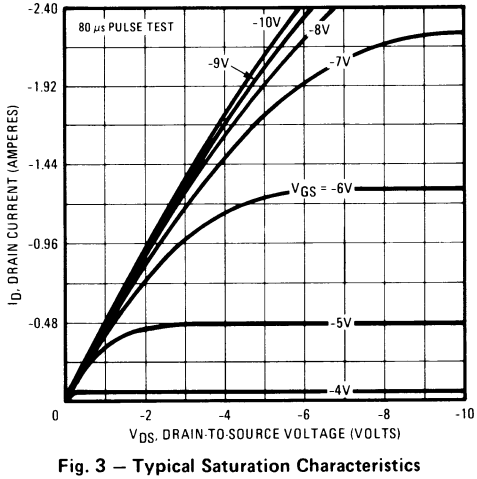


Fig. 3 — Typical Saturation Characteristics

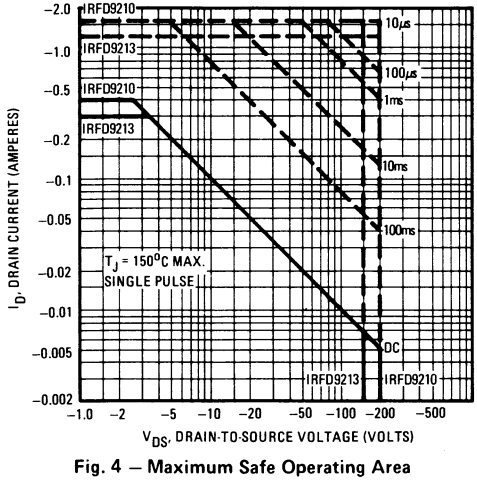


Fig. 4 — Maximum Safe Operating Area

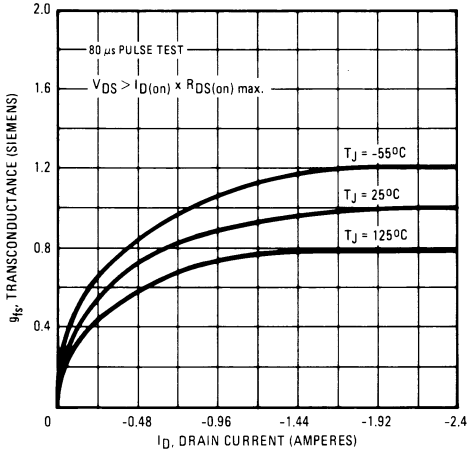


Fig. 5 — Typical Transconductance Vs. Drain Current

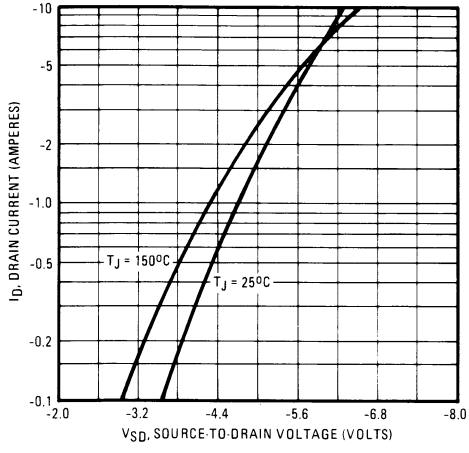


Fig. 6 — Typical Source-Drain Diode Forward Voltage

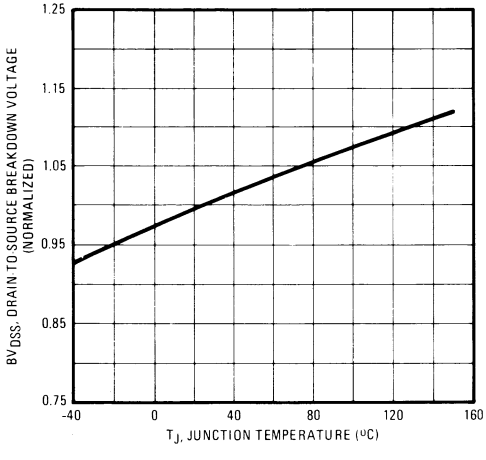


Fig. 7 — Breakdown Voltage Vs. Temperature

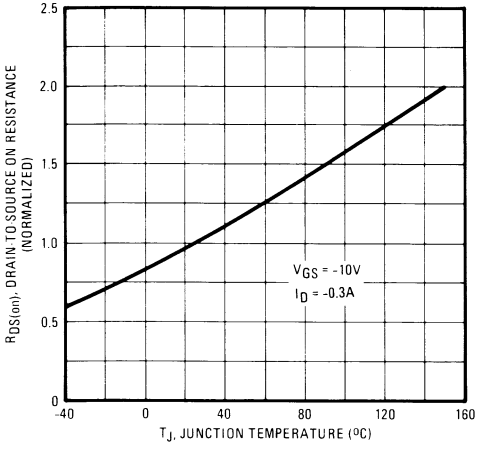


Fig. 8 — Normalized On-Resistance Vs. Temperature

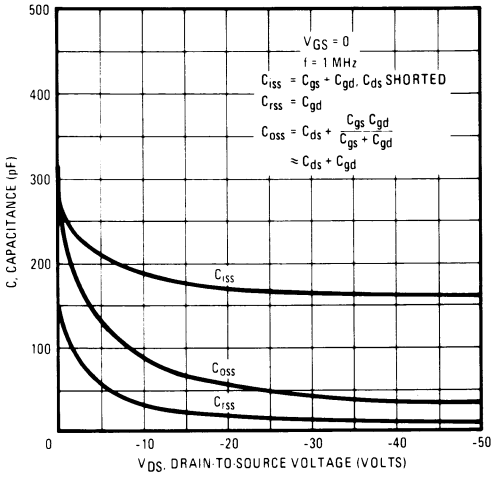


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

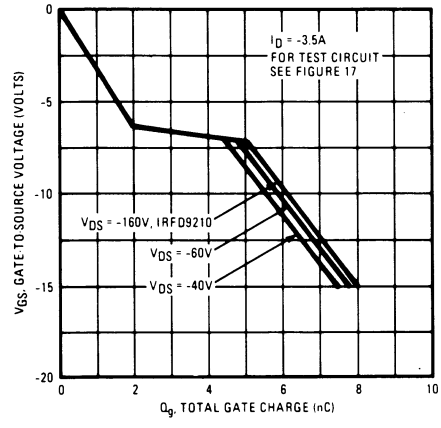


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

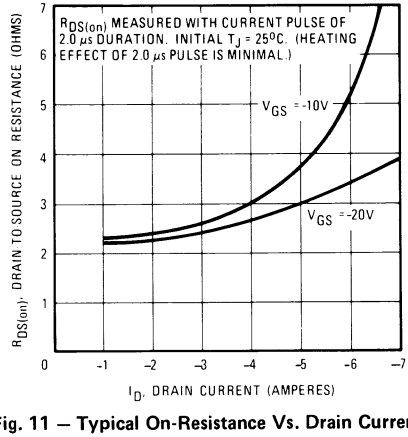


Fig. 11 — Typical On-Resistance Vs. Drain Current

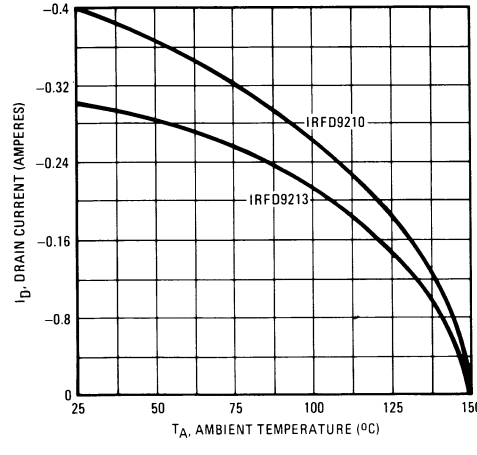


Fig. 12 — Maximum Drain Current Vs. Case Temperature

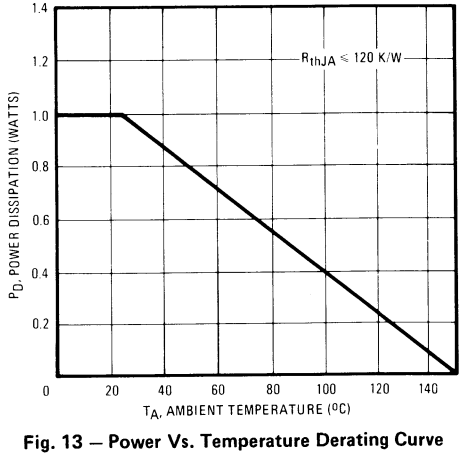


Fig. 13 — Power Vs. Temperature Derating Curve

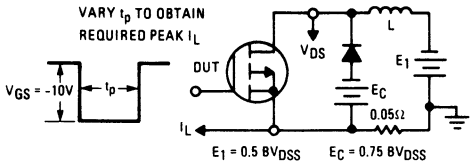


Fig. 14 – Clamped Inductive Test Circuit

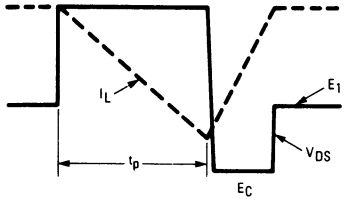


Fig. 15 – Clamped Inductive Waveforms

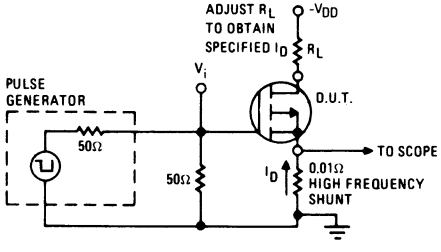


Fig. 16 – Switching Time Test Circuit

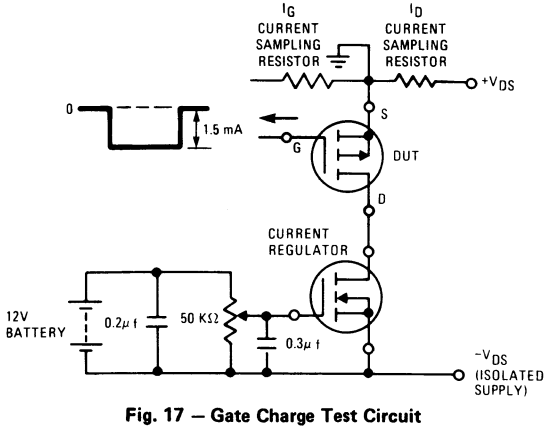


Fig. 17 – Gate Charge Test Circuit