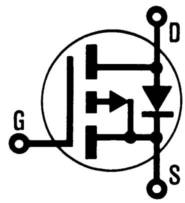
INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRFF9110 IRFF9111 IRFF9112 IRFF9113

P-CHANNEL POWER MOSFETs TO-39 PACKAGE



-100 Volt, 1.2 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P-Channel HEXFETs are designed for applications which require the convenience of reverse polarity operation. They retain all of the features of the more common N-Channel HEXFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and excellent temperature stability. The P-Channel IRFF9110 device is an approximate electrical complement to the N-Channel IRFF110 HEXFET.

P-Channel HEXFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

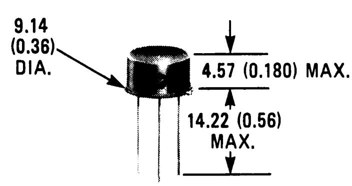
Features:

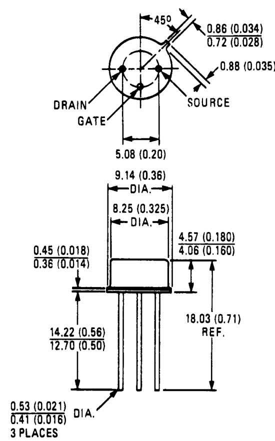
- P-Channel Versatility
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFF9110	-100V	1.2Ω	-2.6A
IRFF9111	-60V	1.2Ω	-2.6A
IRFF9112	-100V	1.6Ω	-2.3A
IRFF9113	-60V	1.6Ω	-2.3A

CASE STYLE AND DIMENSIONS





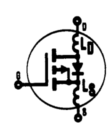
Conforms to JEDEC Outline TO-205AF (TO-39)
Dimensions in Millimeters and (Inches)

IRFF9110, IRFF9111, IRFF9112, IRFF9113 Devices

Absolute Maximum Ratings

Parameter		IRFF9110	IRFF9111	IRFF9112	IRFF9113	Units
V_{DS}	Drain — Source Voltage ①	-100	-60	-100	-60	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 20 kΩ) ①	-100	-60	-100	-60	V
I_D @ T_C = 25°C	Continuous Drain Current	-2.6	-2.6	-2.3	-2.3	A
I_{DM}	Pulsed Drain Current ③	-10	-10	-9.0	-9.0	A
V_{GS}	Gate — Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	15 (See Fig. 14)				W
	Linear Derating Factor	0.12 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH -10	-10	-9.0	-9.0	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

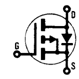
Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRFF9110 IRFF9112	-100	—	—	V	V_{GS} = 0V
		IRFF9111 IRFF9113	-60	—	—	V	I_D = -250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
I_{GSS}	Gate — Source Leakage Forward	ALL	—	—	-100	nA	V_{GS} = -20V
I_{GSS}	Gate — Source Leakage Reverse	ALL	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF9110 IRFF9111	-2.6	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = -10V
		IRFF9112 IRFF9113	-2.3	—	—	A	
$R_{DS(on)}$	Static Drain — Source On-State Resistance ②	IRFF9110 IRFF9111	—	1.0	1.2	Ω	V_{GS} = -10V, I_D = -1.5A
		IRFF9112 IRFF9113	—	1.2	1.6	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.8	1.1	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = -1.5A
C_{iss}	Input Capacitance	ALL	—	180	250	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	85	100	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	30	35	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	15	30	ns	V_{DD} ≈ -50V, I_D = -1.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	30	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	20	40	ns	
t_f	Fall Time	ALL	—	20	40	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	8.5	11	nC	V_{GS} = -15V, I_D = -5.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	3.8	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	4.7	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die. — Modified MOSFET symbol showing the internal device inductances. 
L_S	Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	8.33	K/W	
R_{thJA}	Junction-to-Ambient	ALL	—	—	175	K/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF9110 IRFF9111	–	–	-2.6	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRFF9112 IRFF9113	–	–	-2.3	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF9110 IRFF9111	–	–	-10	A	
		IRFF9112 IRFF9113	–	–	-9.0	A	
V_{SD}	Diode Forward Voltage ②	IRFF9110 IRFF9111	–	–	-5.5	V	$T_C = 25°C, I_S = -2.6A, V_{GS} = 0V$
		IRFF9112 IRFF9113	–	–	-5.3	V	$T_C = 25°C, I_S = -2.3A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	–	120	–	ns	$T_J = 150°C, I_F = -2.6A, dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	–	6.0	–	μC	$T_J = 150°C, I_F = -2.6A, dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

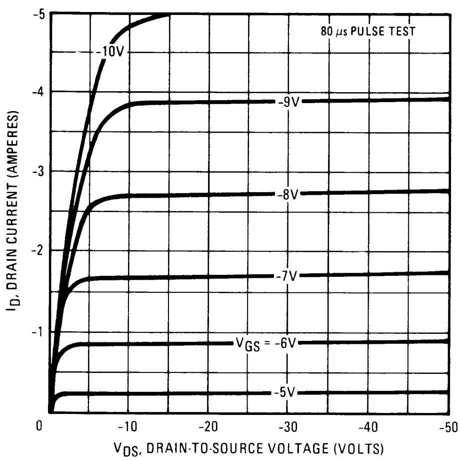


Fig. 1 — Typical Output Characteristics

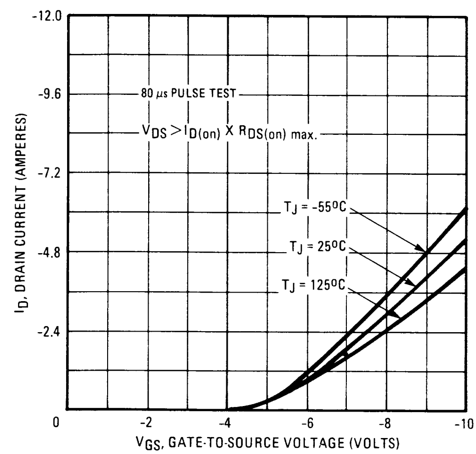


Fig. 2 — Typical Transfer Characteristics

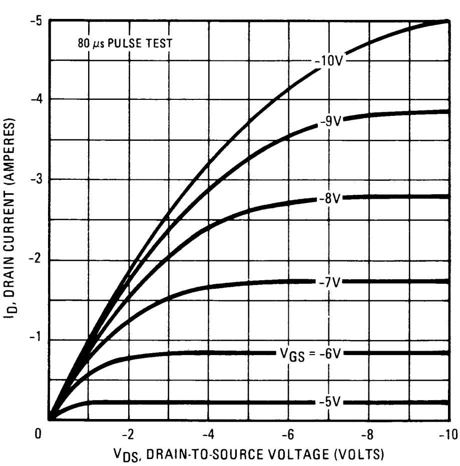


Fig. 3 — Typical Saturation Characteristics

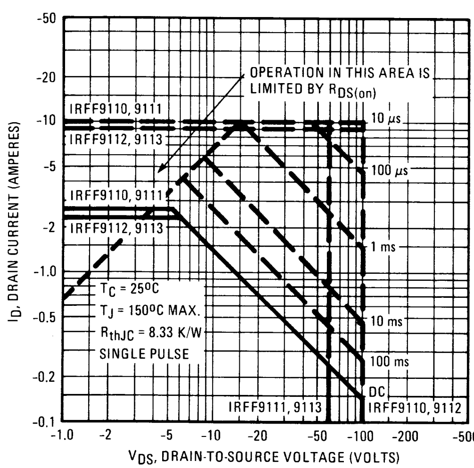


Fig. 4 — Maximum Safe Operating Area

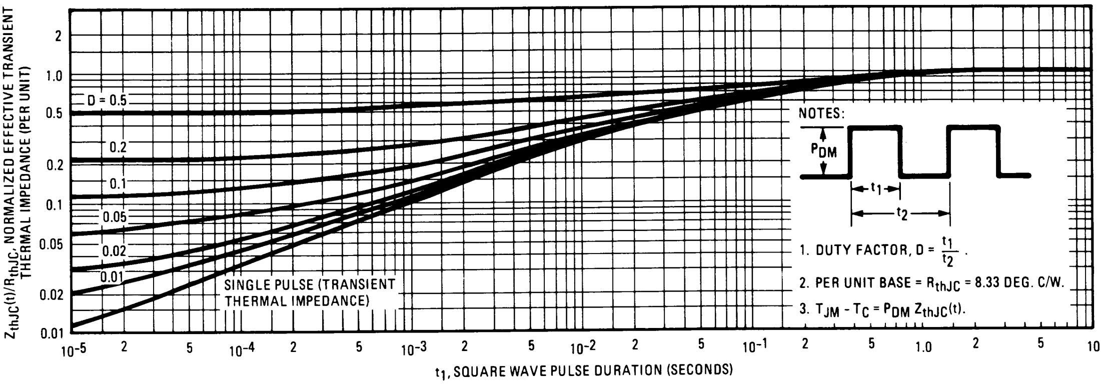


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

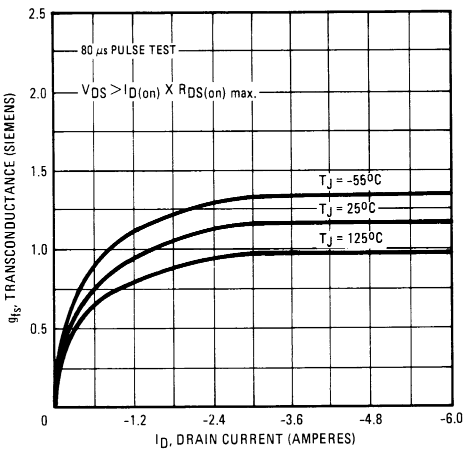


Fig. 6 — Typical Transconductance Vs. Drain Current

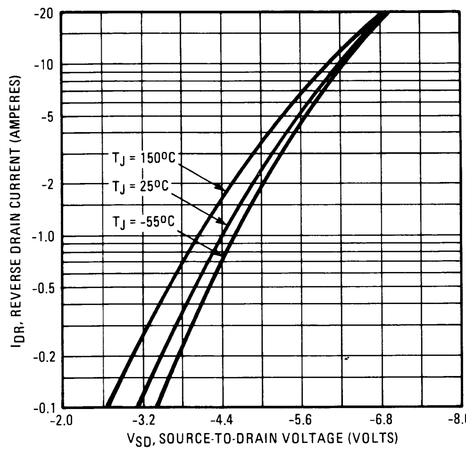


Fig. 7 — Typical Source-Drain Diode Forward Voltage

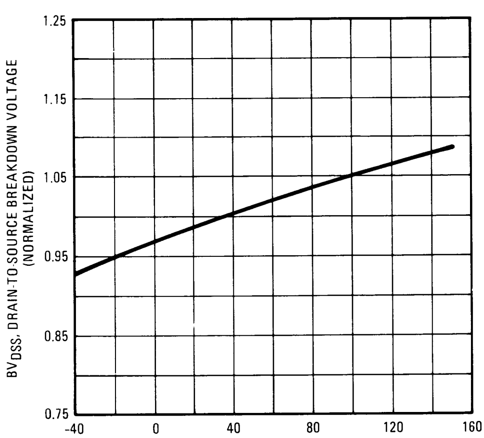


Fig. 8 — Breakdown Voltage Vs. Temperature

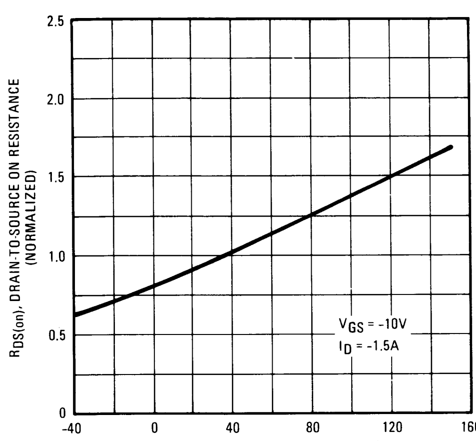


Fig. 9 — Normalized On-Resistance Vs. Temperature

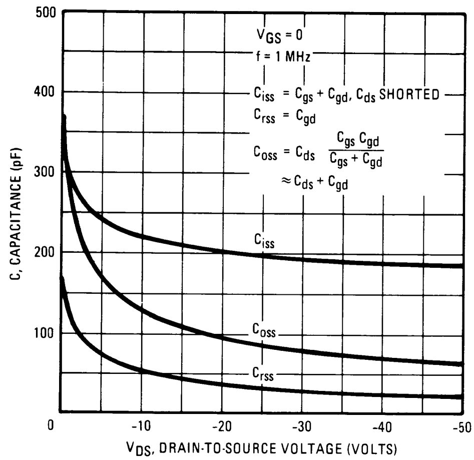


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

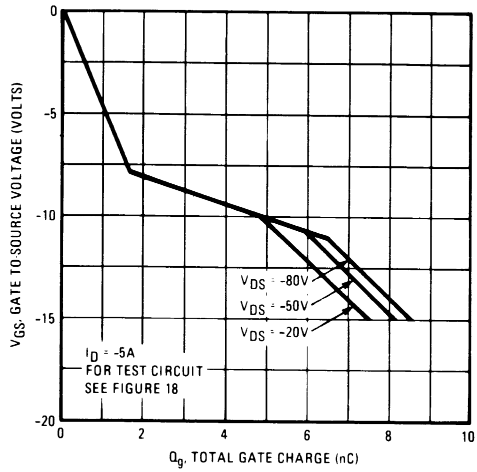


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

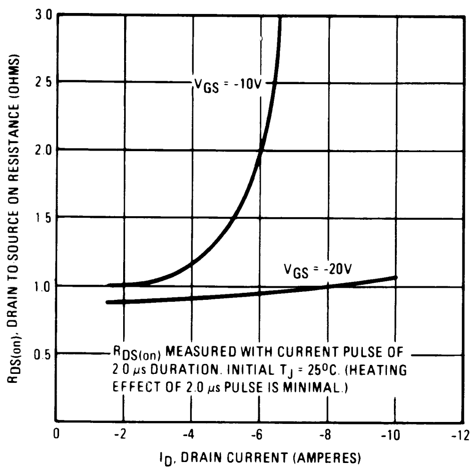


Fig. 12 — Typical On-Resistance Vs. Drain Current

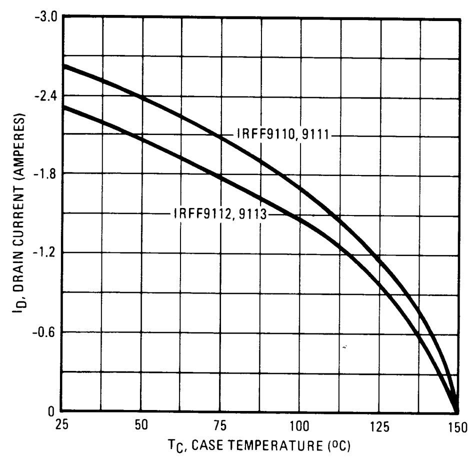


Fig. 13 — Maximum Drain Current Vs. Case Temperature

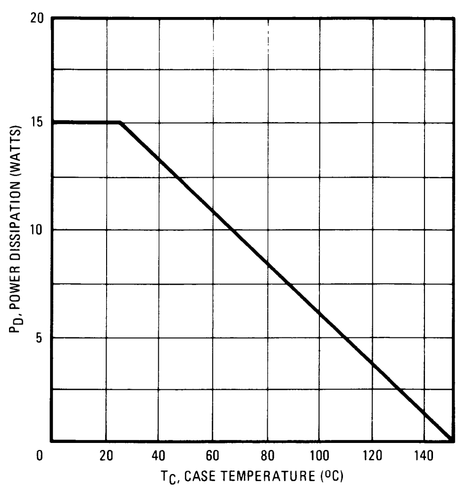


Fig. 14 — Power Vs. Temperature Derating Curve

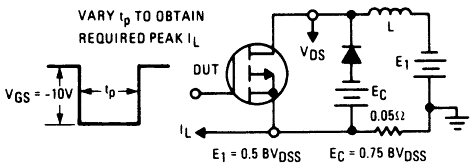


Fig. 15 — Clamped Inductive Test Circuit

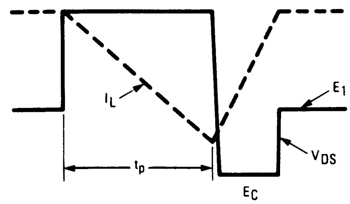


Fig. 16 — Clamped Inductive Waveforms

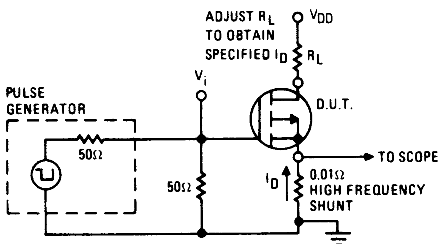


Fig. 17 — Switching Time Test Circuit

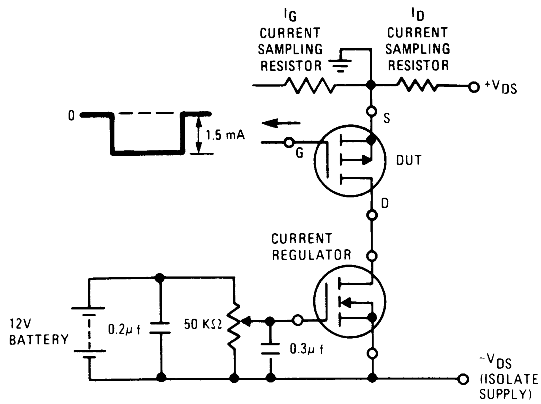


Fig. 18 — Gate Charge Test Circuit

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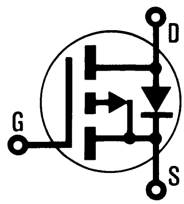
HEXFET® TRANSISTORS IRFF9120 IRFF9121 IRFF9122 IRFF9123

P-CHANNEL POWER MOSFETs TO-39 PACKAGE



-100 Volt, 0.6 Ohm HEXFET

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P-Channel HEXFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

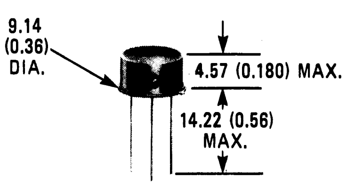
Features:

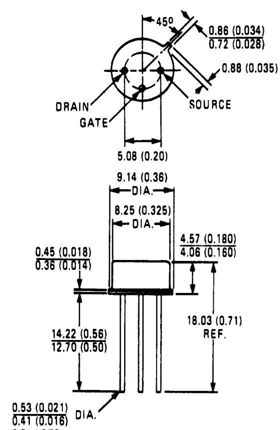
- P-Channel Versatility
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFF9120	-100V	0.6Ω	-4.0A
IRFF9121	-60V	0.6Ω	-4.0A
IRFF9122	-100V	0.8Ω	-3.5A
IRFF9123	-60V	0.8Ω	-3.5A

CASE STYLE AND DIMENSIONS





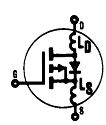
Conforms to JEDEC Outline TO-205AF (TO-39)
Dimensions in Millimeters and (Inches)

Absolute Maximum Ratings

	Parameter	IRFF9120	IRFF9121	IRFF9122	IRFF9123	Units
V_{DS}	Drain — Source Voltage ①	-100	-60	-100	-60	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 20 kΩ) ①	-100	-60	-100	-60	V
I_D @ T_C = 25°C	Continuous Drain Current	-4.0	-4.0	-3.5	-3.5	A
I_{DM}	Pulsed Drain Current ③	-16	-16	-14	-14	A
V_{GS}	Gate — Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH -16	-16	-15	-15	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

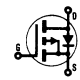
	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRFF9120 IRFF9122	-100	—	—	V	V_{GS} = 0V
		IRFF9121 IRFF9123	-60	—	—	V	I_D = -250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
I_{GSS}	Gate — Source Leakage Forward	ALL	—	—	-100	nA	V_{GS} = -20V
I_{GSS}	Gate — Source Leakage Reverse	ALL	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF9120 IRFF9121	-4.0	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = -10V
		IRFF9122 IRFF9123	-3.5	—	—	A	
$R_{DS(on)}$	Static Drain — Source On-State Resistance ②	IRFF9120 IRFF9121	—	0.5	0.6	Ω	V_{GS} = -10V, I_D = -2.0A
		IRFF9122 IRFF9123	—	0.6	0.8	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.25	2.0	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = -2.0A
C_{iss}	Input Capacitance	ALL	—	300	450	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	200	350	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	50	100	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	25	50	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = -2.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	50	100	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	50	100	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	16	22	nC	V_{GS} = -15V, I_D = -8.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	9.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	7.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die. — Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	6.25	K/W	
R_{thJA}	Junction-to-Ambient	ALL	—	—	175	K/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF9120 IRFF9121	—	—	-4.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRFF9122 IRFF9123	—	—	-3.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF9120 IRFF9121	—	—	-16	A	
		IRFF9122 IRFF9123	—	—	-14	A	
V_{SD}	Diode Forward Voltage ②	IRFF9120 IRFF9121	—	—	-6.3	V	T_C = 25°C, I_S = -4.0A, V_{GS} = 0V
		IRFF9122 IRFF9123	—	—	-6.0	V	T_C = 25°C, I_S = -3.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	230	—	ns	T_J = 150°C, I_F = -4.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	1.3	—	μC	T_J = 150°C, I_F = -4.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

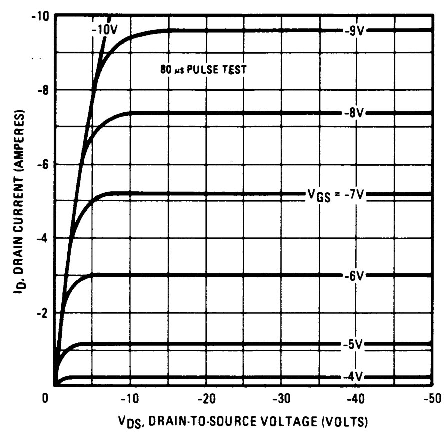


Fig. 1 — Typical Output Characteristics

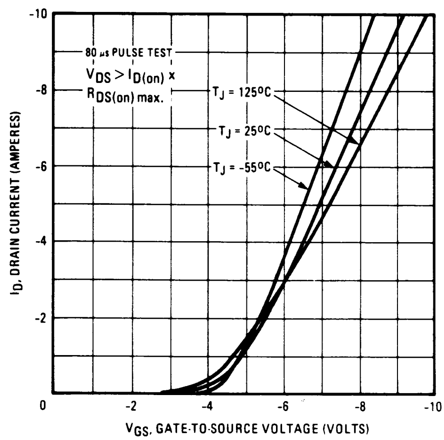


Fig. 2 — Typical Transfer Characteristics

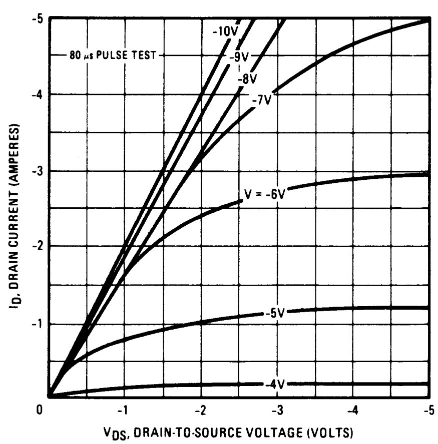


Fig. 3 — Typical Saturation Characteristics

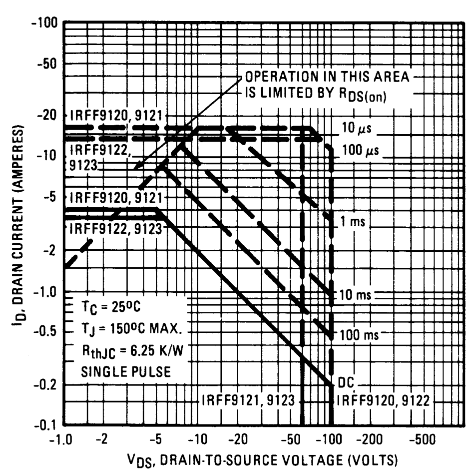


Fig. 4 — Maximum Safe Operating Area

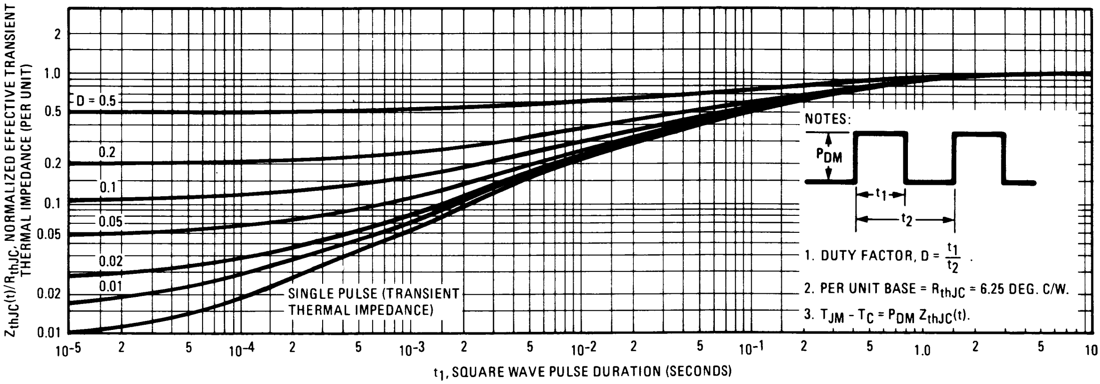


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

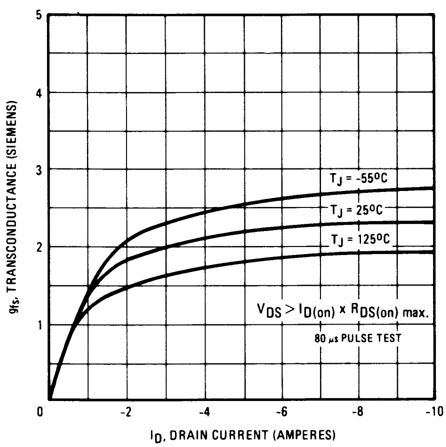


Fig. 6 — Typical Transconductance Vs. Drain Current

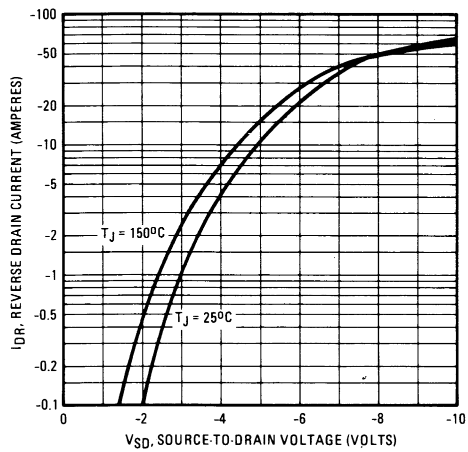


Fig. 7 — Typical Source-Drain Diode Forward Voltage

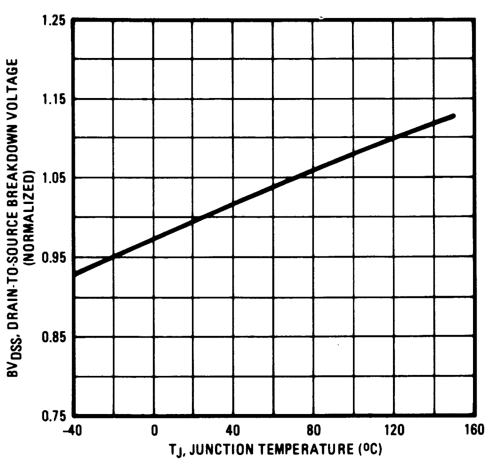


Fig. 8 — Breakdown Voltage Vs. Temperature

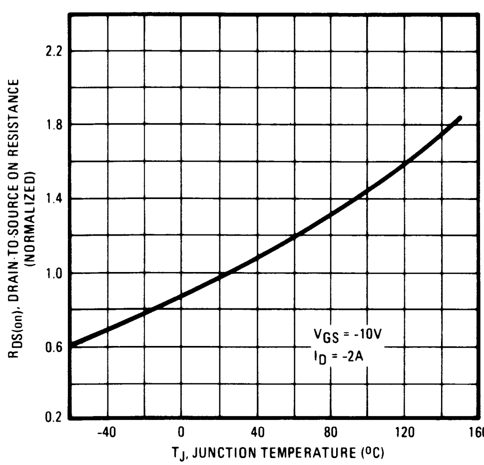


Fig. 9 — Normalized On-Resistance Vs. Temperature

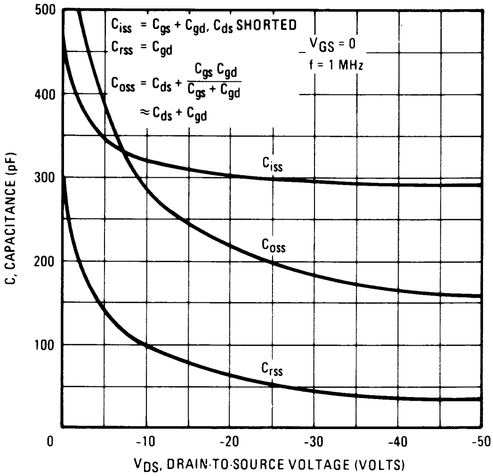


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

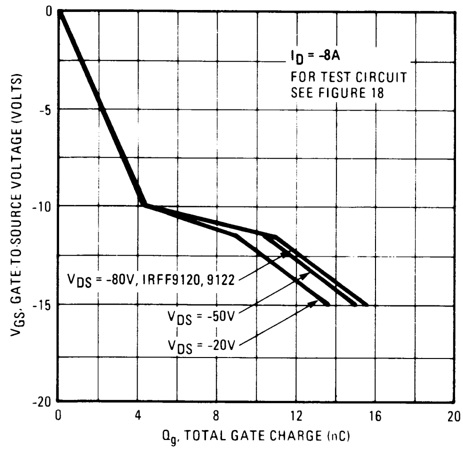


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

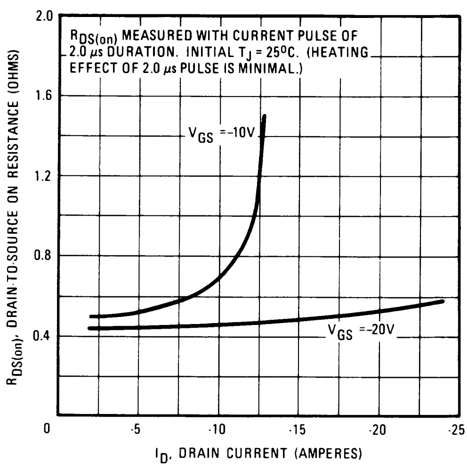


Fig. 12 — Typical On-Resistance Vs. Drain Current

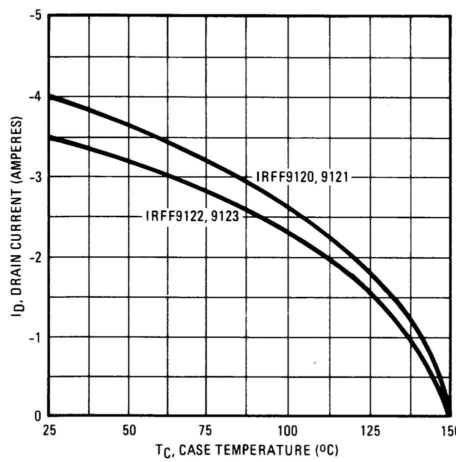


Fig. 13 — Maximum Drain Current Vs. Case Temperature

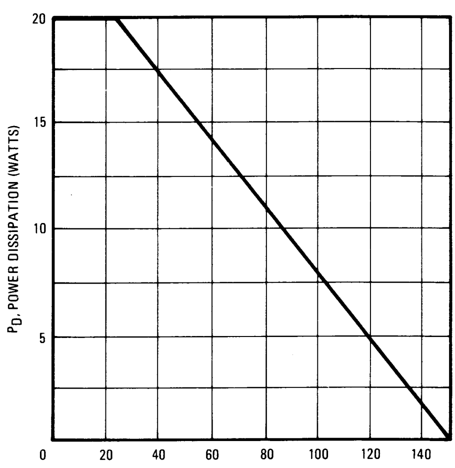


Fig. 14 — Power Vs. Temperature Derating Curve

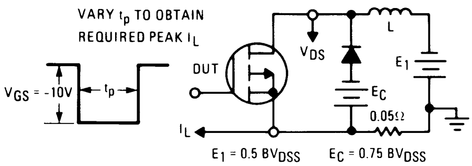


Fig. 15 — Clamped Inductive Test Circuit

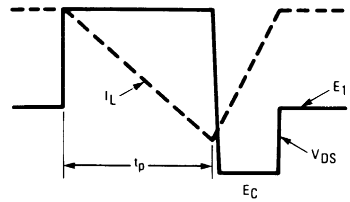


Fig. 16 — Clamped Inductive Waveforms

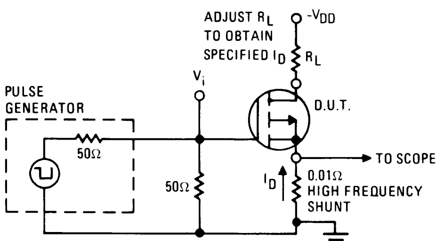


Fig. 17 — Switching Time Test Circuit

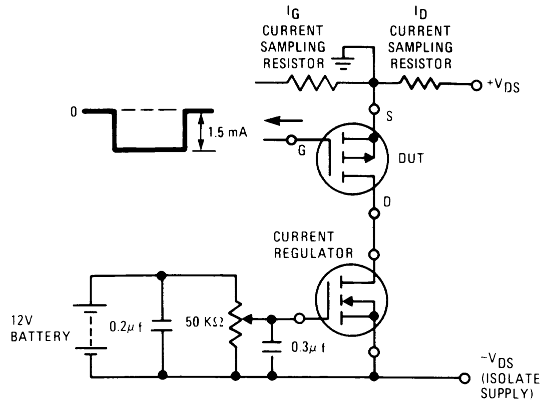
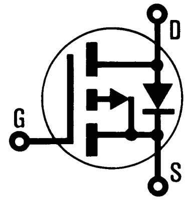


Fig. 18 — Gate Charge Test Circuit

INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRFF9130 IRFF9131 IRFF9132 IRFF9133

P-CHANNEL POWER MOSFETs TO-39 PACKAGE



-100 Volt, 0.3 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P-Channel HEXFETs are designed for applications which require the convenience of reverse polarity operation. They retain all of the features of the more common N-Channel HEXFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and excellent temperature stability. The P-Channel IRFF9130 device is an approximate electrical complement to the N-Channel IRFF120 HEXFET.

P-Channel HEXFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

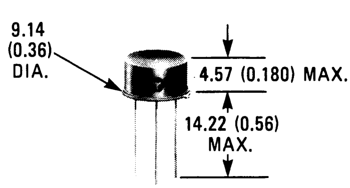
Features:

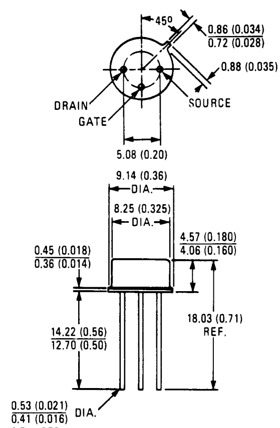
- P-Channel Versatility
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFF9130	-100V	0.3Ω	-6.5A
IRFF9131	-60V	0.3Ω	-6.5A
IRFF9132	-100V	0.4Ω	-5.5A
IRFF9133	-60V	0.4Ω	-5.5A

CASE STYLE AND DIMENSIONS





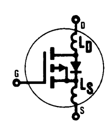
Conforms to JEDEC Outline TO-205AF (TO-39)
Dimensions in Millimeters and (Inches)

IRFF9130, IRFF9131, IRFF9132, IRFF9133 Devices

Absolute Maximum Ratings

Parameter		IRFF9130	IRFF9131	IRFF9132	IRFF9133	Units
V_{DS}	Drain — Source Voltage ①	−100	−60	−100	−60	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 20 kΩ) ①	−100	−60	−100	−60	V
I_D @ T_C = 25°C	Continuous Drain Current	−6.5	−6.5	−5.5	−5.5	A
I_{DM}	Pulsed Drain Current ③	−26	−26	−22	−22	A
V_{GS}	Gate — Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	25 (See Fig. 14)				W
	Linear Derating Factor	0.2 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH −26	−26	−22	−22	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

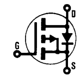
Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRFF9130 IRFF9132	−100	—	—	V	V_{GS} = 0V
		IRFF9131 IRFF9133	−60	—	—	V	I_D = −250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	−2.0	—	−4.0	V	V_{DS} = V_{GS}, I_D = −250μA
I_{GSS}	Gate — Source Leakage Forward	ALL	—	—	−100	nA	V_{GS} = −20V
I_{GSS}	Gate — Source Leakage Reverse	ALL	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	−250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	−1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF9130 IRFF9131	−6.5	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = −10V
		IRFF9132 IRFF9133	−5.5	—	—	A	
$R_{DS(on)}$	Static Drain — Source On-State Resistance ②	IRFF9130 IRFF9131	—	0.25	0.30	Ω	V_{GS} = −10V, I_D = −3.0A
		IRFF9132 IRFF9133	—	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.5	3.5	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = −3.0A
C_{iss}	Input Capacitance	ALL	—	500	700	pF	V_{GS} = 0V, V_{DS} = −25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	300	450	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	100	200	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	30	60	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = −3.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	70	140	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	70	140	ns	
t_f	Fall Time	ALL	—	70	140	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	25	45	nC	V_{GS} = −15V, I_D = −15A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	13	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	12	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die. / Modified MOSFET symbol showing the internal device inductances. 
L_S	Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	5.0	K/W	
R_{thJA}	Junction-to-Ambient	ALL	—	—	175	K/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF9130 IRFF9131	—	—	-6.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRFF9132 IRFF9133	—	—	-5.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF9130 IRFF9131	—	—	-26	A	
		IRFF9132 IRFF9133	—	—	-22	A	
V_{SD}	Diode Forward Voltage ②	IRFF9130 IRFF9131	—	—	-6.3	V	T_C = 25°C, I_S = -6.5A, V_{GS} = 0V
		IRFF9132 IRFF9133	—	—	-6.0	V	T_C = 25°C, I_S = -5.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	300	—	ns	T_J = 150°C, I_F = -6.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	1.8	—	μC	T_J = 150°C, I_F = -6.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

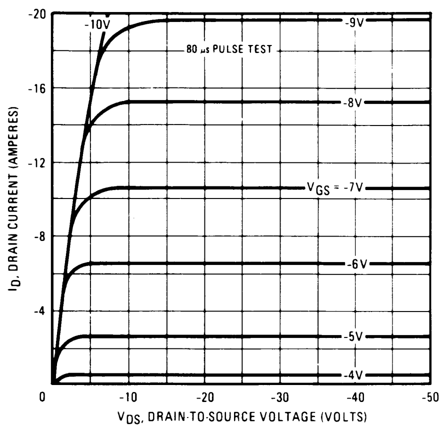


Fig. 1 — Typical Output Characteristics

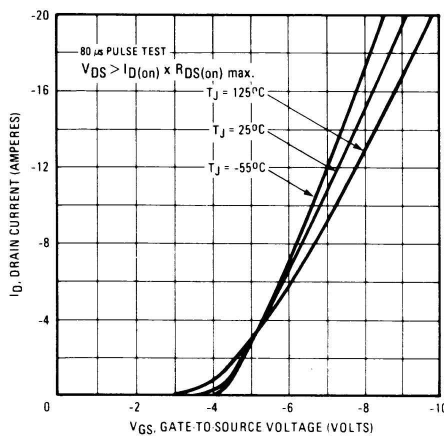


Fig. 2 — Typical Transfer Characteristics

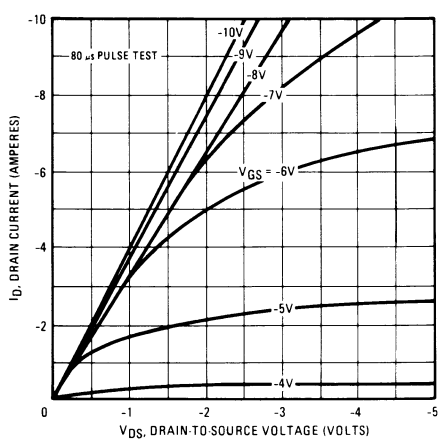


Fig. 3 — Typical Saturation Characteristics

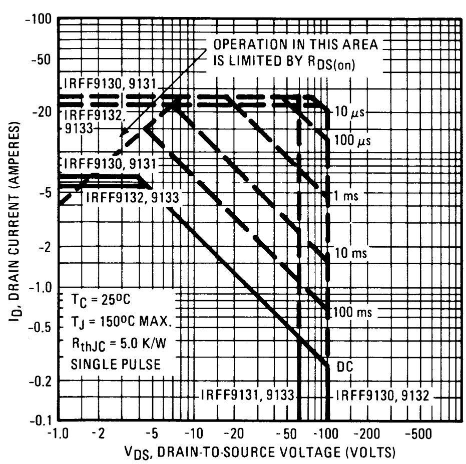


Fig. 4 — Maximum Safe Operating Area

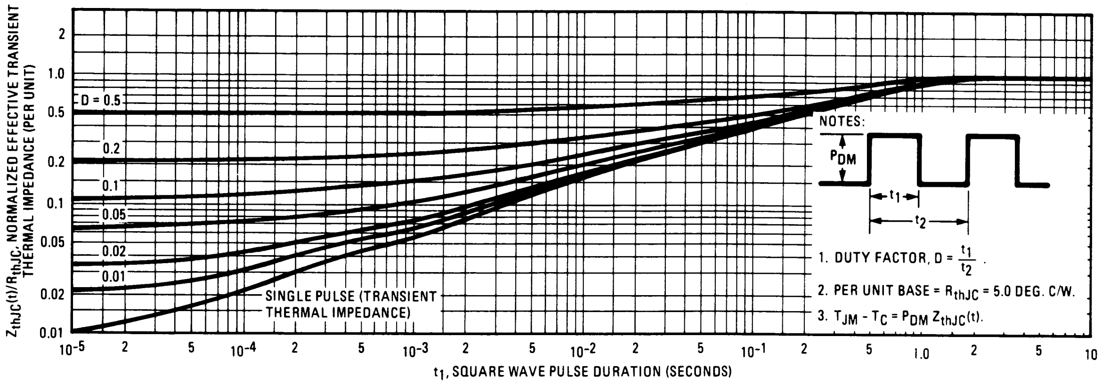


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

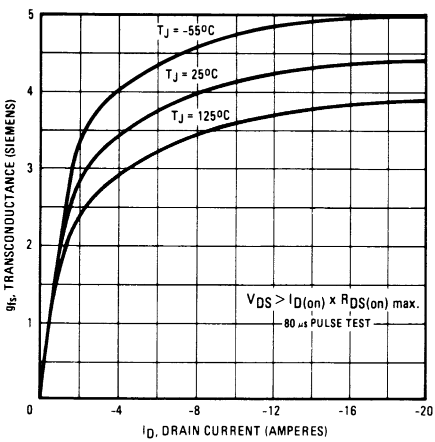


Fig. 6 — Typical Transconductance Vs. Drain Current

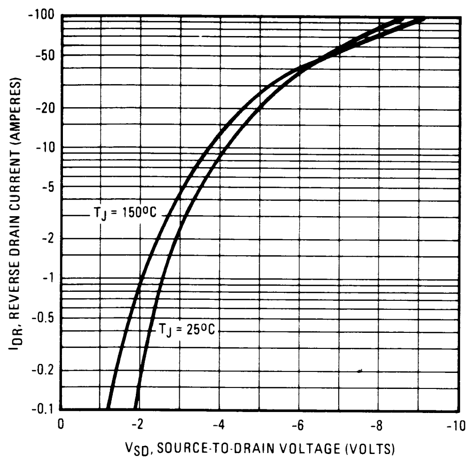


Fig. 7 — Typical Source-Drain Diode Forward Voltage

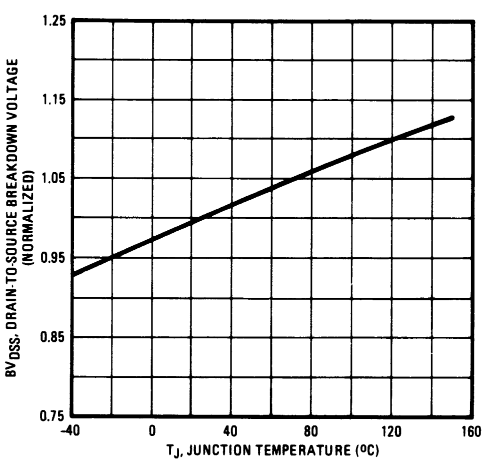


Fig. 8 — Breakdown Voltage Vs. Temperature

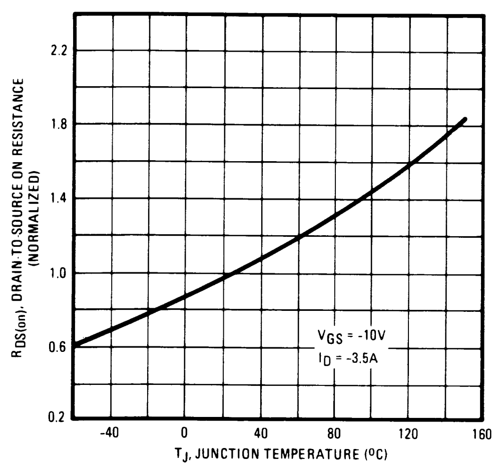


Fig. 9 — Normalized On-Resistance Vs. Temperature

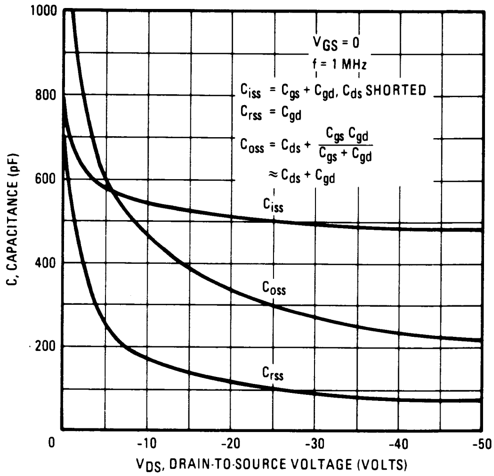


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

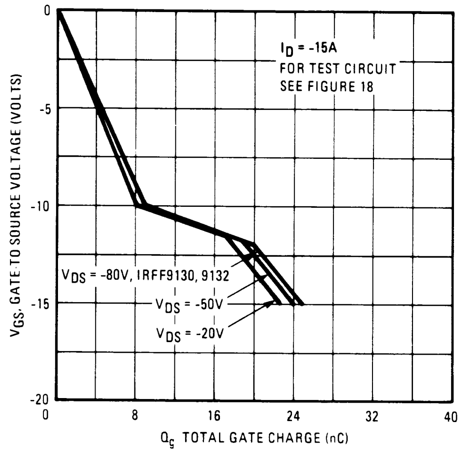


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

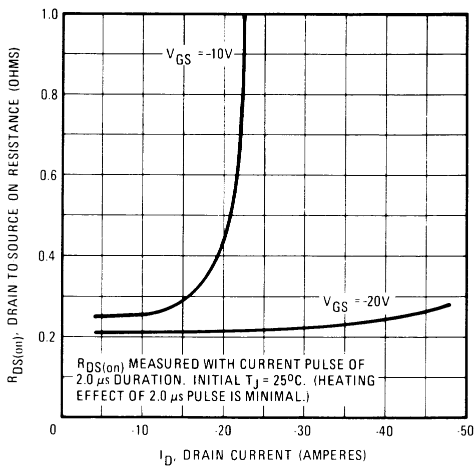


Fig. 12 — Typical On-Resistance Vs. Drain Current

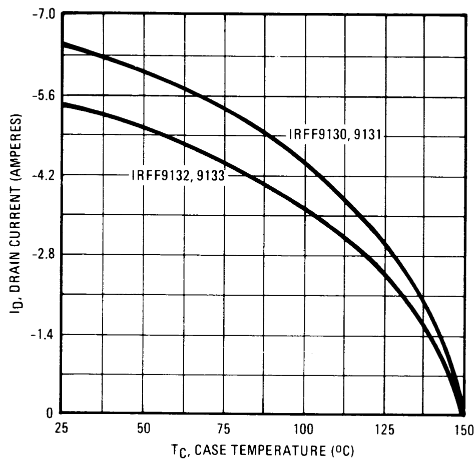


Fig. 13 — Maximum Drain Current Vs. Case Temperature

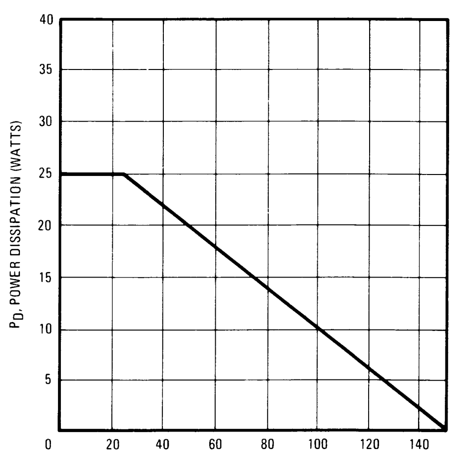


Fig. 14 — Power Vs. Temperature Derating Curve

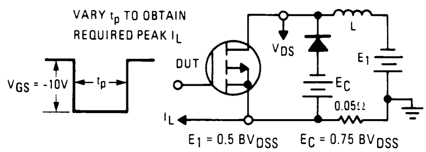


Fig. 15 — Clamped Inductive Test Circuit

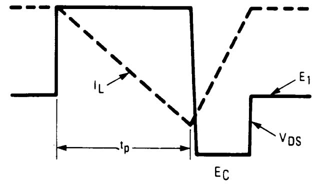


Fig. 16 — Clamped Inductive Waveforms

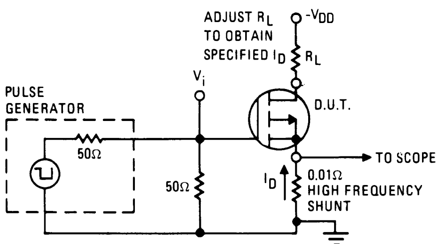


Fig. 17 — Switching Time Test Circuit

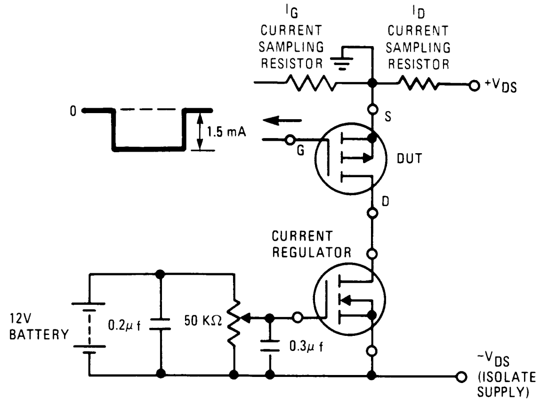


Fig. 18 — Gate Charge Test Circuit