HARRIS

IRFPC40R
IRFPC42R

N-Channel Power MOSFETs
Avalanche-Energy-Rated

May 1992

Features

- 6.8A, 5.9A and 600V
- $r_{DS(ON)}$ = 1.2Ω and 1.6Ω
- Isolated Central Mounting Hole
- Repetitive Avalanche Ratings
- Simple Drive Requirements
- Ease of Paralleling

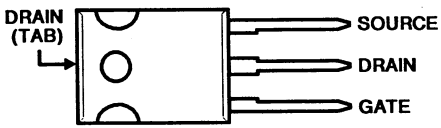
Description

The IRFPC40R and IRFPC42R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFPC types are supplied in the JEDEC TO-247 plastic package.

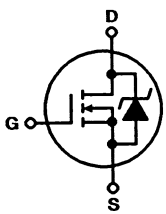
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



N-CHANNEL

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFPC40R	IRFPC42R	UNITS
Continuous Drain Current				
T_C = +25°C	I_D	6.8	5.9	A
T_C = +100°C	I_D	4.3	3.7	A
Pulsed Drain Current (2)	I_{DM}	27	24	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (3) (See Figure 14)	E_{as}	410	410	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

NOTES:

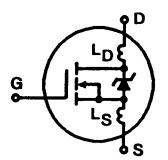
1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
3. V_{DD} = 50V, Start T_J = +25°C, L = 16mH, R_G = 25Ω, Peak I_L = 6.8A

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number 2158.1

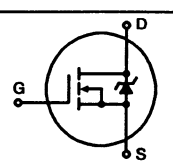
Electrical Characteristics $T_C = 25^oC$, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V$, $I_D = 250\mu A$	600	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	$V_{GS} = 20V$	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	$V_{GS} = -20V$	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, $V_{GS} = 0V$	-	-	250	μA
		V_{DS} = Max Rating x 0.8, $V_{GS} = 0V$, $T_J = +125^oC$	-	-	1000	μA
On-State Drain Current (Note 1) IRFPC40R	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, $V_{GS} = 10V$	6.8	-	-	A
IRFPC42R			5.9	-	-	A
Static Drain-Source On-State Resistance (Note 1) IRFPC40R	$r_{DS(ON)}$	$V_{GS} = 10V$, $I_D = 3.7A$	-	0.97	1.2	Ω
IRFPC42R			-	1.2	1.6	Ω
Forward Transconductance (Note 1)	g_{fs}	$I_{DS} = 3.7A$, $V_{DS} \geq 100V$	4.9	7.3	-	S(℧)
Input Capacitance	C_{ISS}	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1.0MHz See Figure 10	-	1300	-	pF
Output Capacitance	C_{OSS}		-	160	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	45	-	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 200V$, $I_D = 6.2A$, $R_G = 9.1\Omega$ $R_D = 47\Omega$. (Independent of operating temperature) See Figure 15.	-	13	20	ns
Rise Time	t_r		-	18	27	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	55	83	ns
Fall Time	t_f		-	20	30	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	$V_{GS} = 10V$, $I_D = 6.2A$, $V_{DS} = 0.6V$ x Max Rating. See Figure 16 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	40	60	nC
Gate-Source Charge	Q_{gs}		-	5.5	8.3	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	20	30	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 6mm (0.25") from package to center of die. Modified MOSFET symbol showing the internal inductances.	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from package to source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.10	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	6.8	A
Pulse Source Current (Body Diode) (Note 1)	I_{SM}		-	-	27	A
Diode Forward Voltage (Note 3)	V_{SD}	$T_J = +25^oC$, $I_S = 6.2A$, $V_{GS} = 0V$	-	-	1.5	V
Reverse Recovery Time	t_{rr}	$T_J = +25^oC$, $I_F = 6.2A$, $dI_F/dt = 100A/\mu s$	200	450	940	ns
Reverse Recovered Charge	Q_{RR}	$T_J = +25^oC$, $I_F = 6.2A$, $dI_F/dt = 100A/\mu s$	1.8	3.8	7.9	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	-	-	-	-



NOTES:

1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
3. $V_{DD} = 50V$, Start $T_J = +25^oC$, L = 16mH, $R_{GS} = 25\Omega$, $I_{PEAK} = 6.8A$

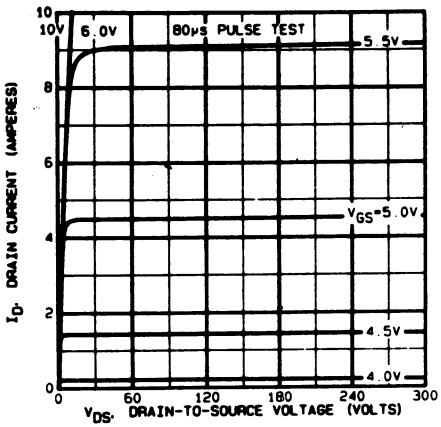


Fig. 1 - Typical Output Characteristics

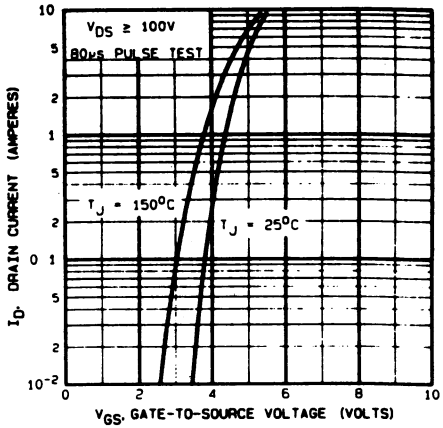


Fig. 2 - Typical Transfer Characteristics

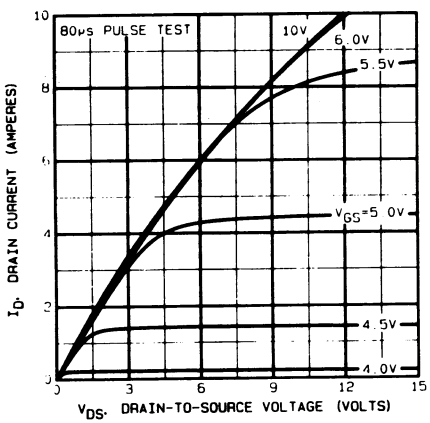


Fig. 3 - Typical Saturation Characteristics

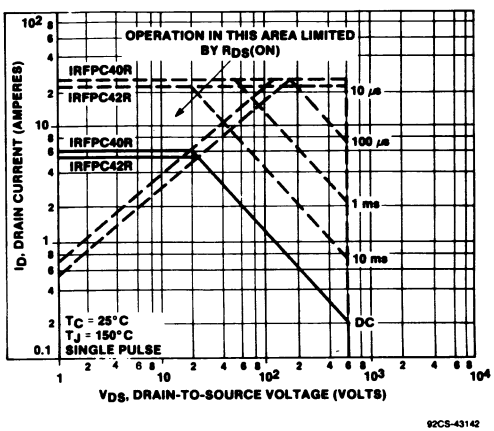


Fig. 4 - Maximum Safe Operating Area

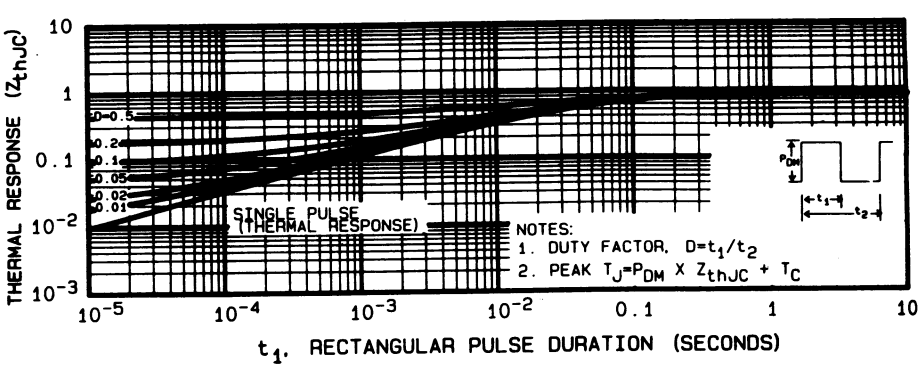


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

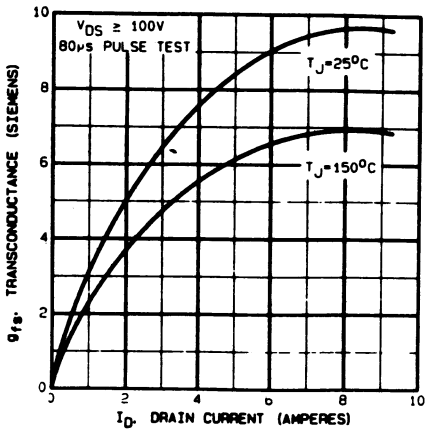


Fig. 6 - Typical Transconductance Vs. Drain Current

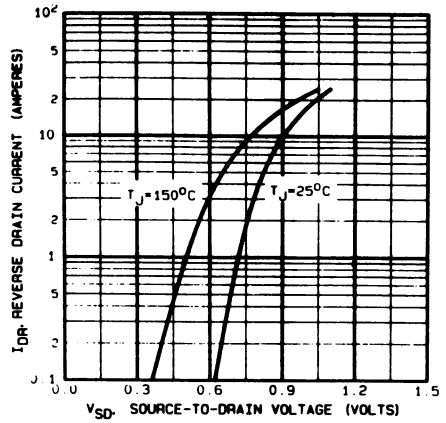


Fig. 7 - Typical Source-Drain Diode Forward Voltage

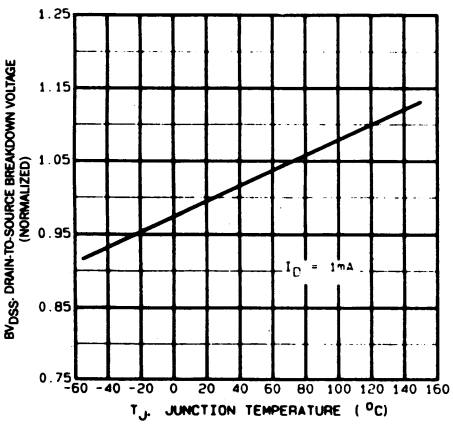


Fig. 8 - Breakdown Voltage Vs. Temperature

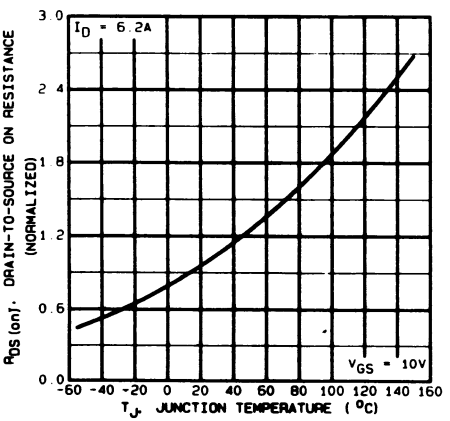


Fig. 9 - Normalized On-Resistance Vs. Temperature

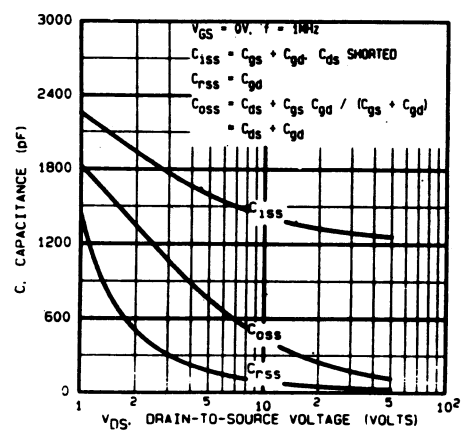


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

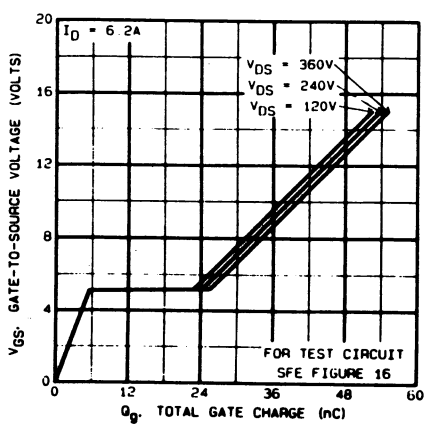


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

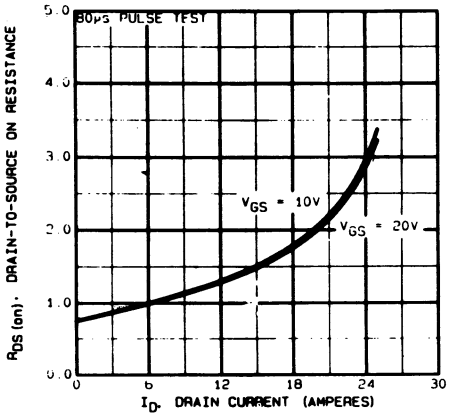


Fig. 12 - Typical On-Resistance Vs. Drain Current

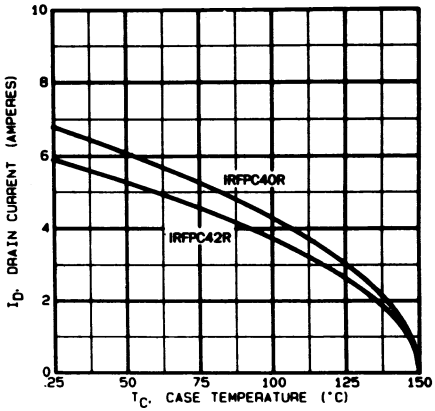


Fig. 13 - Maximum Drain Current Vs. Case Temperature

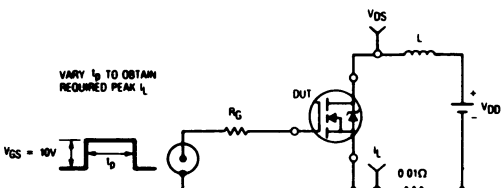


Fig. 14a - Unclamped Inductive Test Circuit

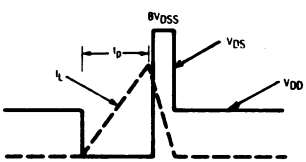


Fig. 14b - Unclamped Inductive Waveforms

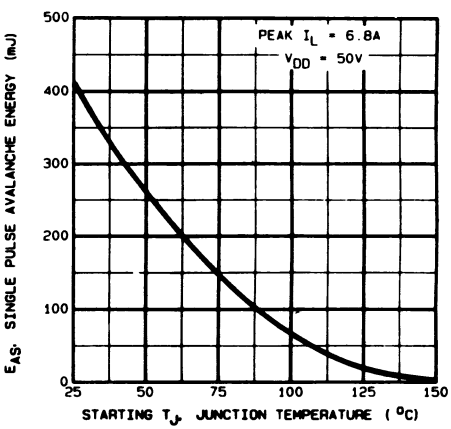


Fig. 14c - Maximum Avalanche Energy Vs. Starting Junction Temperature

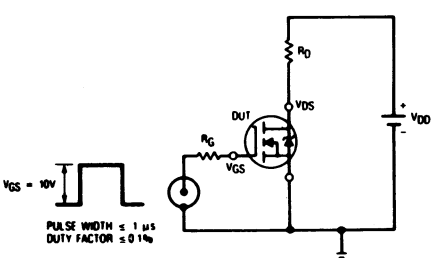


Fig. 15a - Switching Time Test Circuit

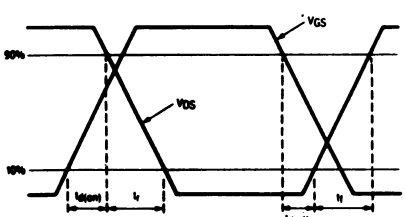


Fig. 15b - Switching Time Waveforms

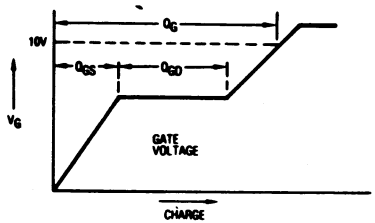
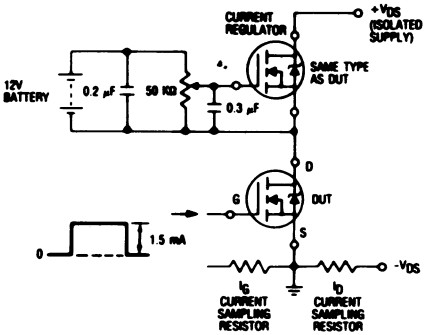


Fig. 16a - Basic Gate Charge Waveform



Fib. 16b - Gate Charge Test Circuit

HARRIS

IRFPG40
IRFPG42

High Voltage N-Channel Enhancement Mode Power Field Effect Transistor

August 1991

Features

- IRFPG40: 4.3A, 1000V, $r_{DS(ON)} = 3.5\Omega$
- IRFPG42: 3.9A, 1000V, $r_{DS(ON)} = 4.2\Omega$
- UIS SOA Rating Curve (Single Pulse)
- -55°C to 150°C Operating and Storage Temperature

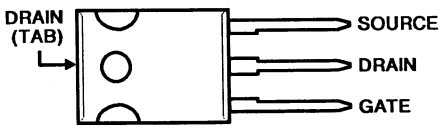
Description

The IRFPG40 and IRFPG42 are n-channel enhancement mode silicon-gate power field effect transistors. They are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFPG40 and IRFPG42 are supplied in the JEDEC TO-247 plastic package.

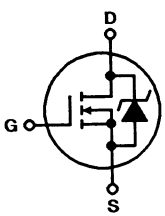
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

		IRFPG40	IRFPG42	UNITS
Drain-Souce	V_{DSS}	1000	1000	V
Drain-Gate	V_{DGR}	1000	1000	V
Continuous Drain Current	I_D	4.3	3.9	A
Pulsed Drain Current	I_{DM}	17	16	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = 25°C	P_D	150	150	W
Derate Above T_C = 25°C		0.83	0.83	W/°C
Single Pulse Avalanche Energy Rating (See Figure 13)	E_{as}	490	490	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number 2879

Electrical Characteristics (T_C = 25°C), Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V	1000	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 0.25mA	2.0	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0V	-		μA
		V_{DS} = 1000V T_C = 25°C	-	250	μA
		V_{DS} = 800V T_C = 150°C	-	1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	±500	nA
On Resistance	$r_{DS(ON)}$	I_D = 2.5A, V_{GS} = 10V			
IRFPG40			-	3.5	Ω
IRFPG42			-	4.2	Ω
Forward Transconductance	g_{fs}	I_D = 2.5A, V_{DS} = 100V	3.5	-	s
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 500V, I = 3.9A	-	30	ns
Rise Time	t_r	R_G = 9.1Ω	-	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$	R_D = 120Ω	-	170	ns
Fall Time	t_f	See Figure 14	-	50	ns
Total Gate Charge	Q_g	I_D = 3.9A, V_{DS} = 800V, V_{GS} = 10V	-	120	nC
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	0.83	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$		-	40	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Forward Voltage	V_{SD}	I_{SD} = 4.3A	-	1.8	V
Reverse Recovery Time	t_{rr}	I_F = 3.9A, dI_F/dT = 100 A/μs	-	1000	ns

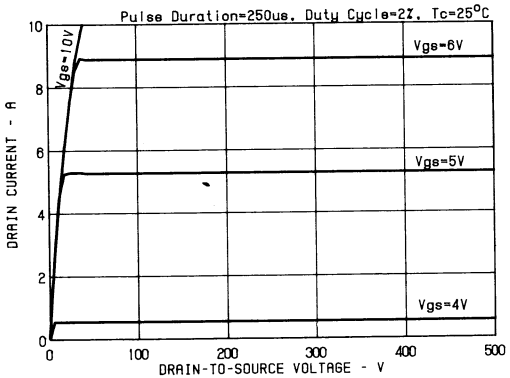


Figure 1 – Typical output characteristics.

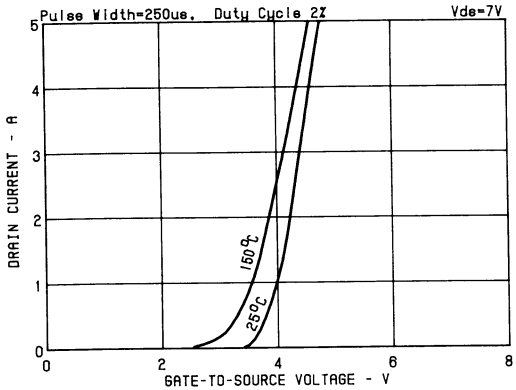


Figure 2 – Typical transfer characteristics.

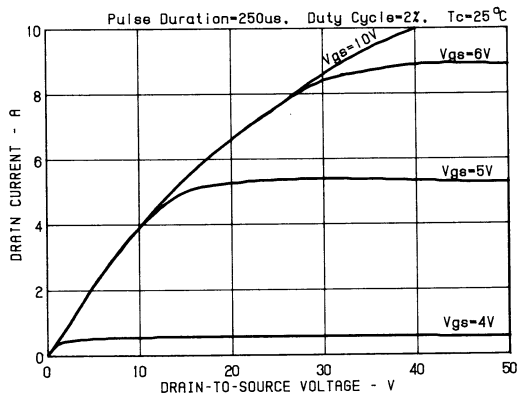


Figure 3 – Typical saturation characteristics.

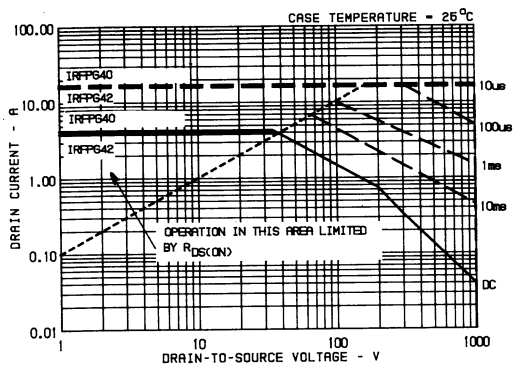


Figure 4 – Maximum safe operating area.

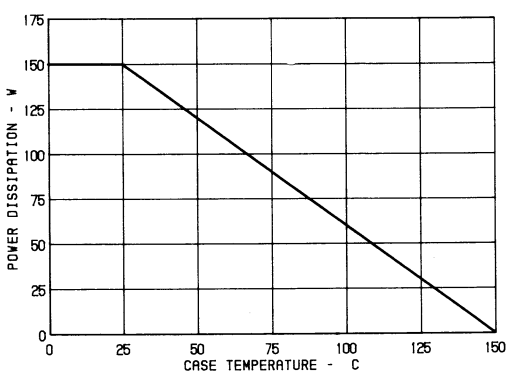


Figure 5 – Power vs. temperature derating curve.

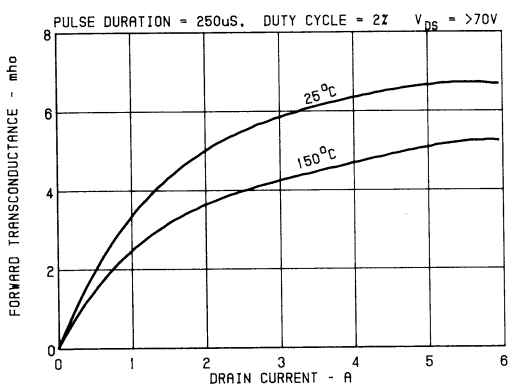


Figure 6 – Typical forward transconductance.

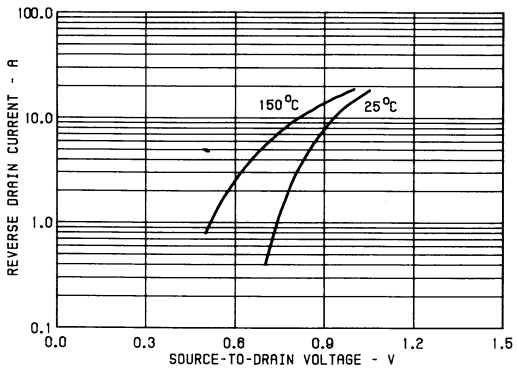


Figure 7 - Typical source-to-drain diode forward voltage.

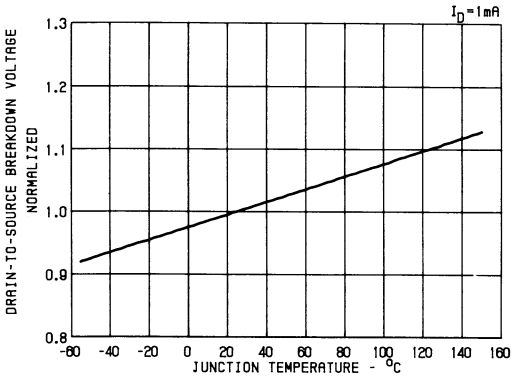


Figure 8 - Breakdown voltage vs. temperature.

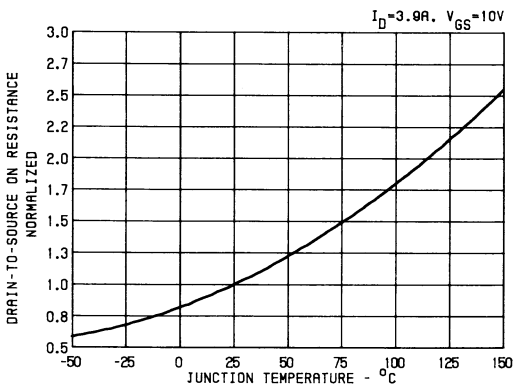


Figure 9 - Normalized drain-to-source on resistance.

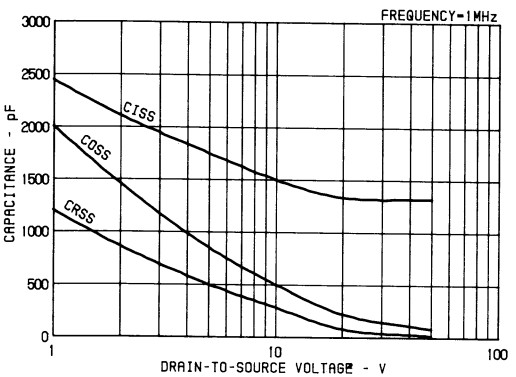


Figure 10 - Typical capacitance vs. voltage.

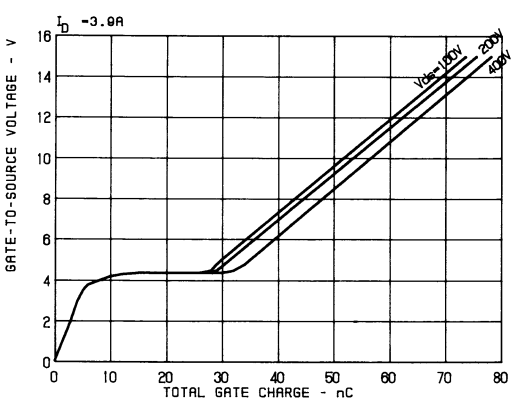


Figure 11 - Typical gate charge.

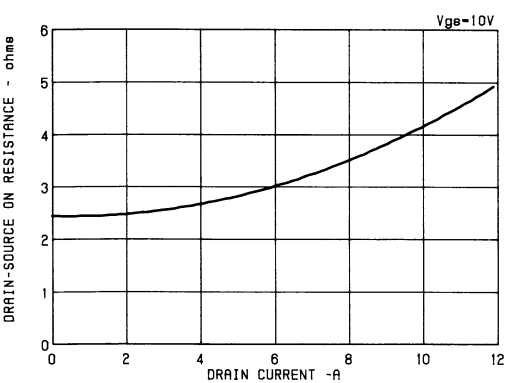


Figure 12 - Typical drain-source on resistance.

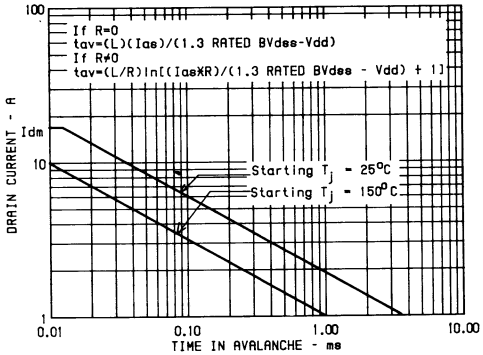


Figure 13 - Unclamped inductive switching SOA.

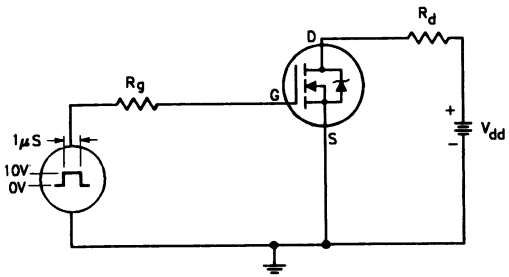


Figure 14 - Switching time test circuit.