HARRIS

IRFP360
IRFP362

N-Channel Power MOSFETs
Avalanche-Energy Rated

August 1991

Features

- 20A and 23A, 400V
- $r_{DS}(on)$ = 0.20Ω and 0.25Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

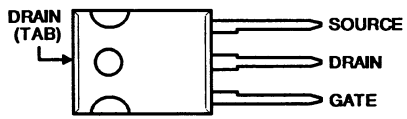
Description

The IRFP360 and IRFP362 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

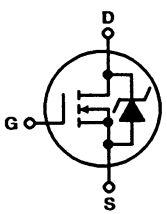
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

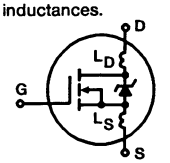
	IRFP360	IRFP362	UNITS
Continuous Drain Current			
T_C = +25°C ..... I_D	23	20	A
T_C = +100°C ..... I_D	14	13	A
Pulsed Drain Current (1) ..... I_{DM}	92	80	A
Gate-Source Voltage ..... V_{GS}	±20	±20	V
Maximum Power Dissipation			
T_C = +25°C ..... P_D	250	250	W
Linear Derating Factor	2.0	2.0	W/°C
Single Pulse Avalanche Energy Rating (2) ..... E_{AS} See Figure 14	1200	1200	mj
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	°C

NOTES:

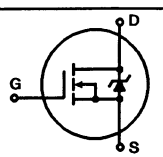
1. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
2. V_{DD} = 50V, starting T_J = +25°C, L = 4.0mH, R_{GS} = 25Ω, Peak I_L = 23A.
3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

File Number 2290.1

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	400	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 3) IRFP360	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	23	-	-	A
IRFP362			20	-	-	A
Static Drain-Source On-State Resistance (Note 3) IRFP360	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 13A	-	0.18	0.20	Ω
IRFP362			-	0.20	0.25	Ω
Forward Transconductance (Note 3)	g_{fs}	V_{DS} ≥ 50V, I_{DS} > 13A	14	21	-	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	4000	-	pF
Output Capacitance	C_{OSS}		-	550	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	97	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 200V, I_D = 25A, R_G = 4.3Ω R_D = 7.5Ω. (MOSFET switching times are essentially independent of operating temperature)	-	22	33	ns
Rise Time	t_r		-	94	140	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	80	120	ns
Fall Time	t_f		-	66	99	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 25A, V_{DS} = 0.8V x Max Rating. See Figure 16 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	68	100	nC
Gate-Source Charge	Q_{gs}		-	17	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	24	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	13	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.50	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.10	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	23	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	92	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 23A, V_{GS} = 0V	-	-	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 25A, dI_F/dt = 100A/μs	200	460	1000	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 25A, dI_F/dt = 100A/μs	3.1	7.1	16	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES:
1. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
2. V_{DD} = 50V, Start T_J = +25°C, L = 4.0mH, R_G = 25Ω, I_{PEAK} = 23A (See Figure 14)
3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

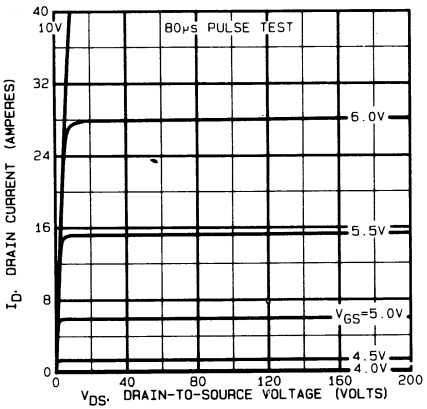


Fig. 1 - Typical output characteristics.

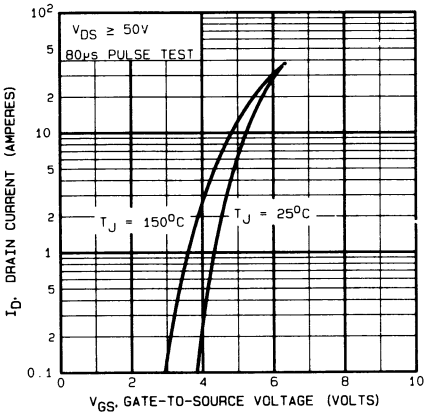


Fig. 2 - Typical transfer characteristics.

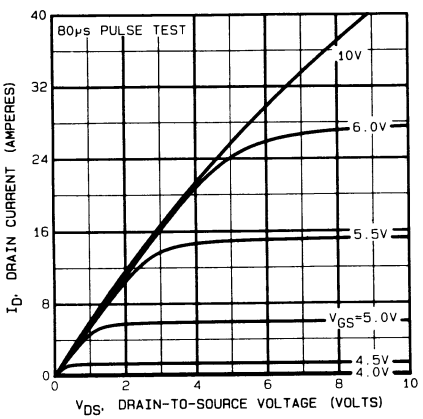


Fig. 3 - Typical saturation characteristics.

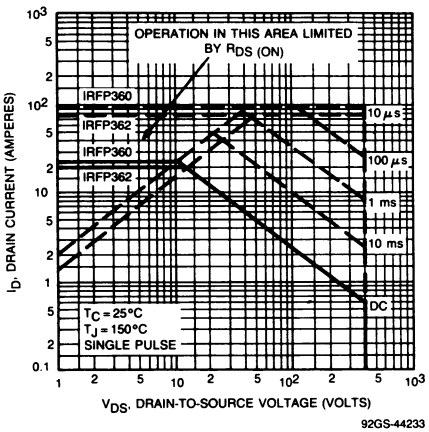


Fig. 4 - Maximum safe operating area.

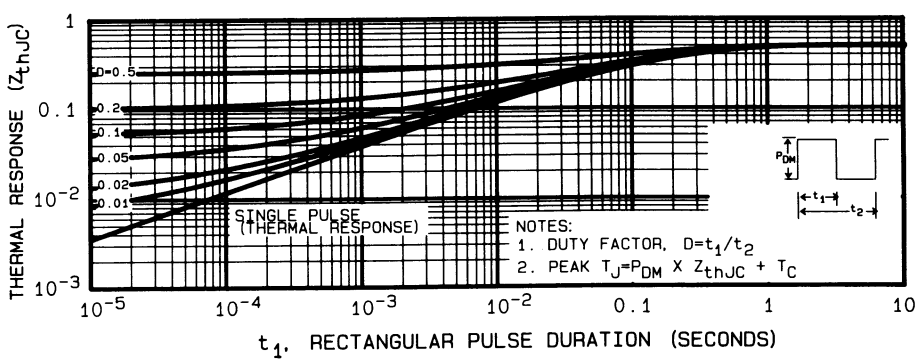


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

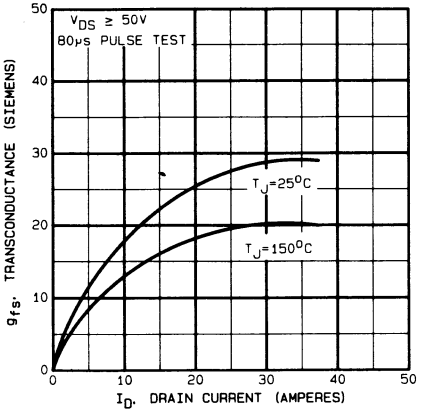


Fig. 6 - Typical transconductance vs. drain current.

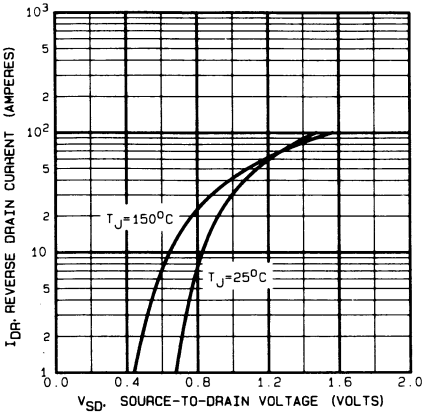


Fig. 7 - Typical source-drain diode forward voltage.

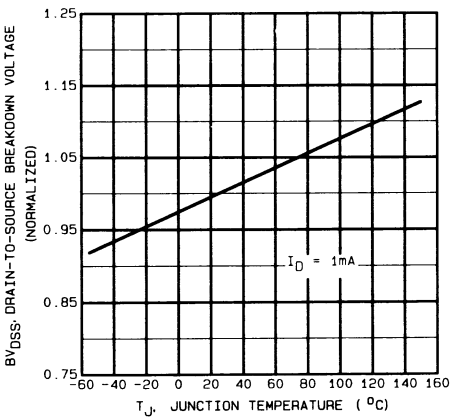


Fig. 8 - Breakdown voltage vs. temperature.

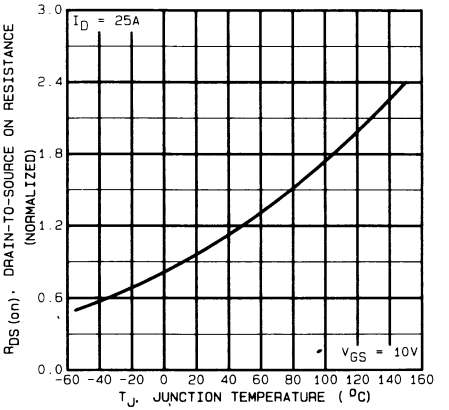


Fig. 9 - Normalized on-resistance vs. temperature.

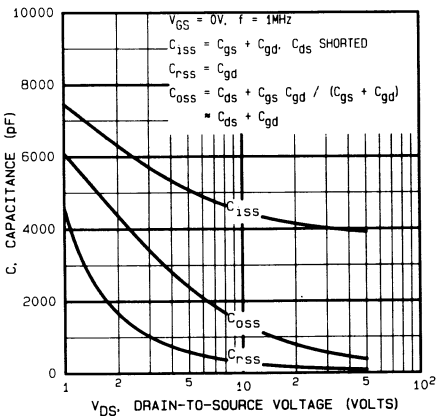


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

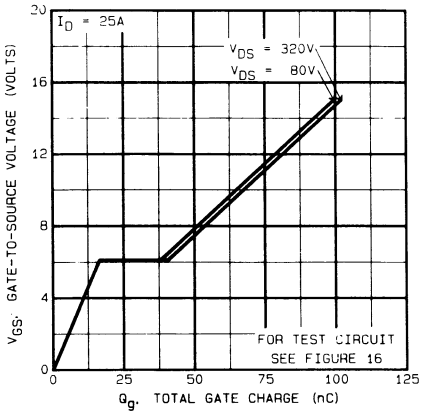


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

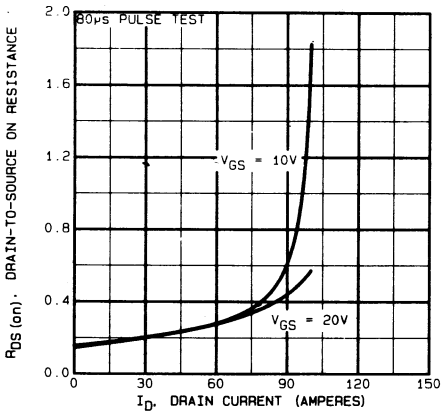


Fig. 12 - Typical on-resistance vs. drain current.

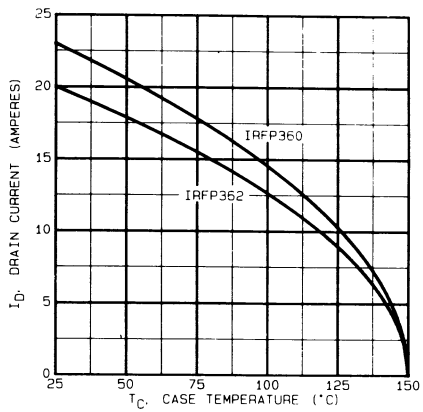


Fig. 13 - Maximum drain current vs. case temperature.

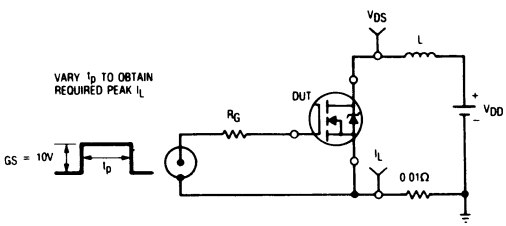


Fig. 14a - Unclamped inductive test circuit.

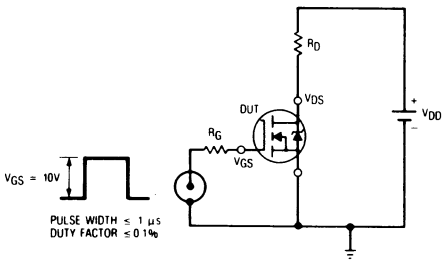


Fig. 15a - Switching time test circuit.

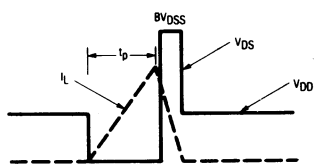


Fig. 14b - Unclamped inductive waveforms.

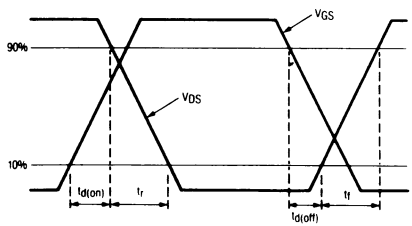


Fig. 15b - Switching time waveforms.

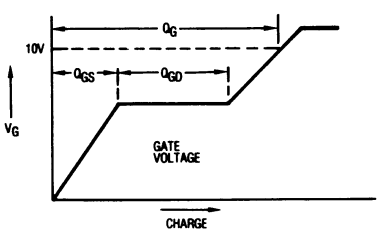


Fig. 16a - Basic gate charge waveform.

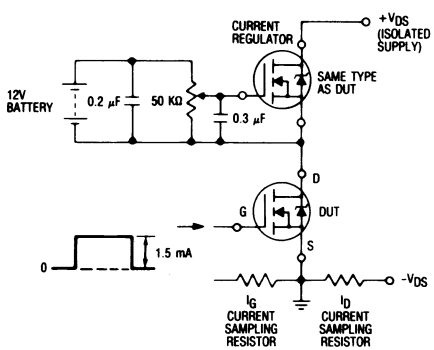


Fig. 16b - Gate charge test circuit.

HARRIS

IRFP460
IRFP462

N-Channel Power MOSFETs
Avalanche-Energy Rated

August 1991

Features

- 20A and 17A, 500V
- $r_{DS}(on)$ = 0.27Ω and 0.35Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

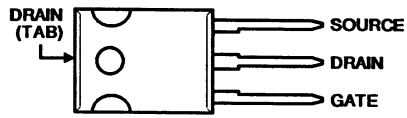
Description

The IRFP460 and IRFP462 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

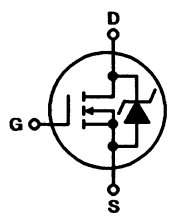
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFP460	IRFP462	UNITS
Continuous Drain Current				
T_C = +25°C	I_D	20	17	A
T_C = +100°C	I_D	12	11	A
Pulsed Drain Current (1)	I_{DM}	80	68	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	250	250	W
Linear Derating Factor		2.0	2.0	W/°C
Single Pulse Avalanche Energy Rating (2) See Figure 14	E_{AS}	960	960	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	°C

NOTES:

1. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
2. V_{DD} = 50V, starting T_J = +25°C, L = 4.3mH, R_{GS} = 25Ω, Peak I_L = 20A. See Fig. 14.
3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **2291.1**

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_J) = 25°C Unless Otherwise Specified*

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	ALL	500	–	–	V	V_{GS} = 0V, I_D = 250 μA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance ③	IRFP460	–	0.24	0.27	Ω	V_{GS} = 10V, I_D = 11A
		IRFP462	–	0.27	0.35		
$I_{D(on)}$	On-State Drain Current ③	IRFP460	20	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ Max. V_{GS} = 10V
		IRFP462	17				
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
g_{fs}	Forward Transconductance ③	ALL	13	19	–	S (℧)	V_{DS} = ≥ 50V, I_{DS} = 11A
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000		V_{DS} = 0.8 x Max. Rating V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	–	–	−500	nA	V_{GS} = −20V
Q_g	Total Gate Charge	ALL	–	120	190	nC	V_{GS} = 10V, I_D = 21A V_{DS} = 0.8 x Max. Rating See Fig. 16 (Independent of operating temperature)
Q_{gs}	Gate-to-Source Charge	ALL	–	18	—	nC	
Q_{gd}	Gate-to-Drain ("Miller") Charge	ALL	–	62	—	nC	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	23	35	ns	V_{DD} = 250V, I_D ≈ 21A, R_G = 4.3Ω R_D = 12Ω See Fig. 15 (Independent of operating temperature)
t_r	Rise Time	ALL	–	81	120	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	85	130	ns	
t_f	Fall Time	ALL	–	65	98	ns	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die. Modified MOSFET symbol showing the internal inductances
L_S	Internal Source Inductance	ALL	–	13	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad
C_{iss}	Input Capacitance	ALL	–	4100	–	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	ALL	–	480	–	pF	f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	ALL	–	84	–	pF	See Fig. 10
R_{thJC}	Junction-to-Case	ALL	–	–	0.50	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.10	–	°C/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free air operation
	Mounting Torque	ALL	–	–	10	in. • lbs	Standard 6-32 screw

① Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 5) Refer to current HEXFET reliability report

② @ V_{DD} = 50V, Starting T_J = 25°C, L = 4.3 mH, R_G = 25Ω, Peak I_L = 20A. See Fig. 14.

③ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	ALL	–	–	20	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier
I_{SM}	Pulsed Source Current (Body Diode) ①	ALL	–	–	80	A	
V_{SD}	Diode Forward Voltage ③	ALL	–	–	1.8	V	T_J = 25°C, I_S = 21A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	280	580	1200	ns	T_J = 25°C, I_F = 21A, di/dt = 100 A/μs
Q_{RR}	Reverse Recovery Charge	ALL	3.8	8.1	18	μC	
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D				

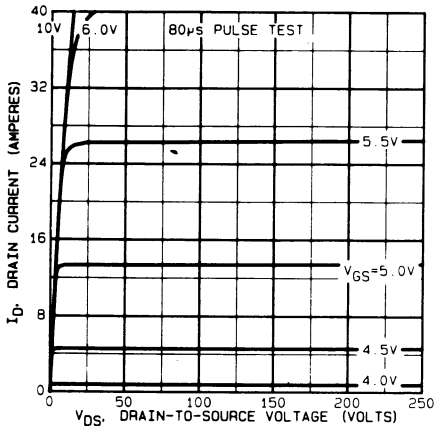


Fig. 1 - Typical output characteristics.

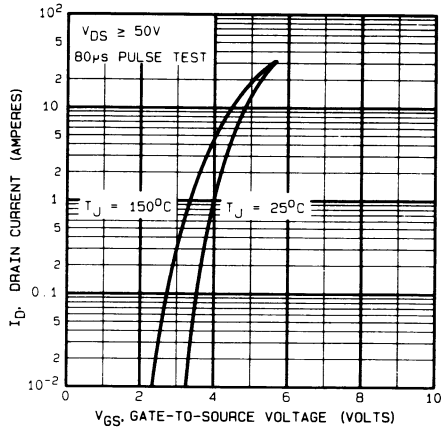


Fig. 2 - Typical transfer characteristics.

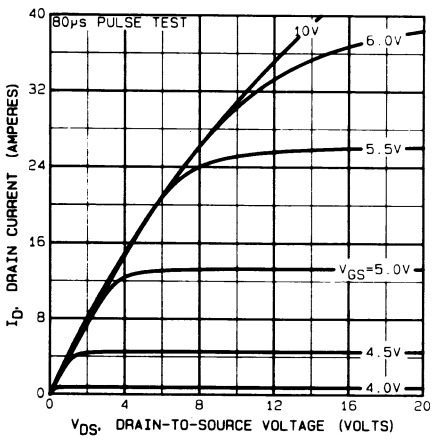


Fig. 3 - Typical saturation characteristics.

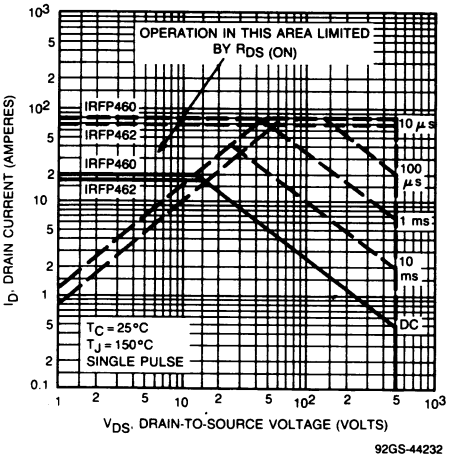


Fig. 4 - Maximum safe operating area.

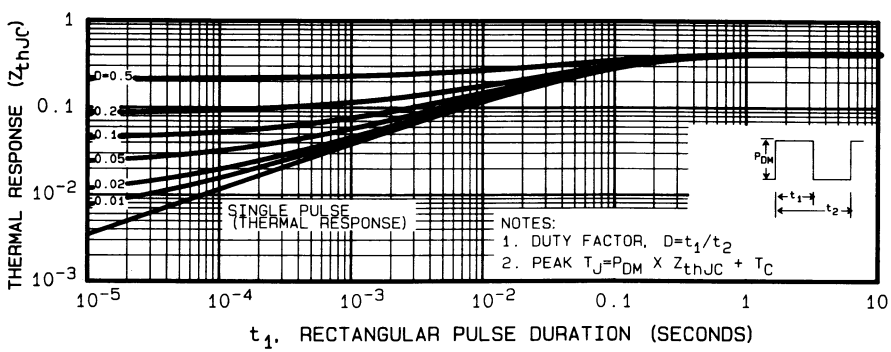


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

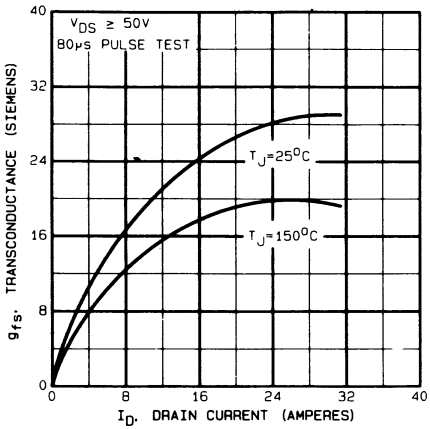


Fig. 6 - Typical transconductance vs. drain current.

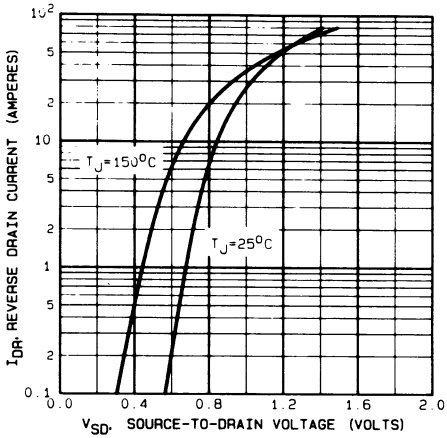


Fig. 7 - Typical source-drain diode forward voltage.

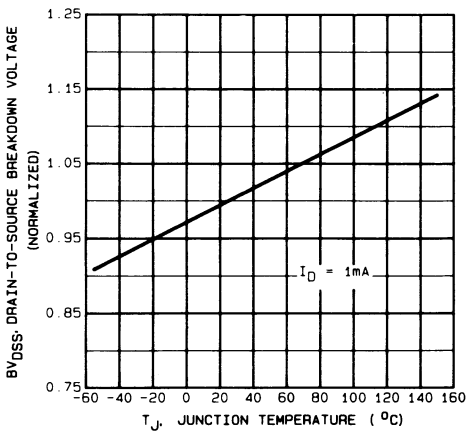


Fig. 8 - Breakdown voltage vs. temperature.

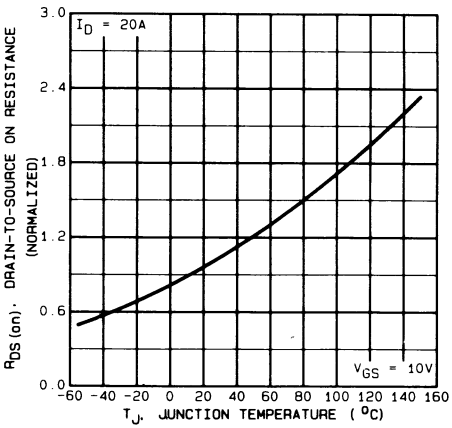


Fig. 9 - Normalized on-resistance vs. temperature.

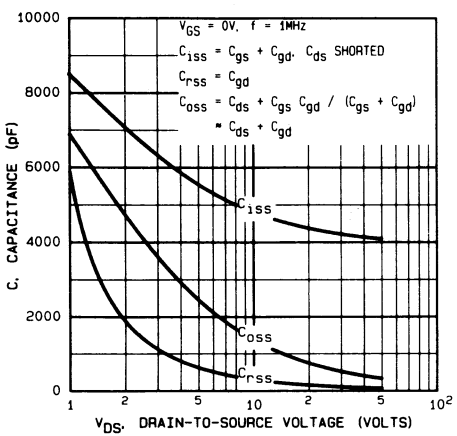


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

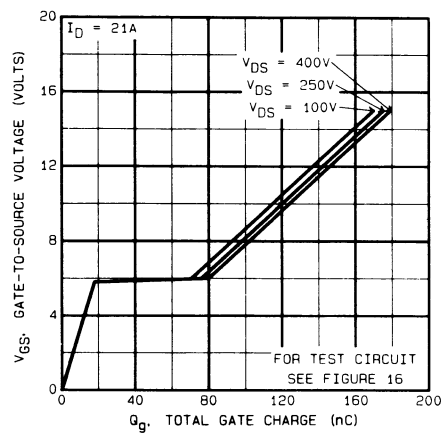


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

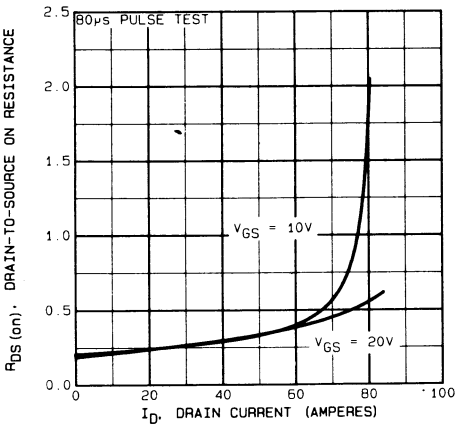


Fig. 12 - Typical on-resistance vs. drain current.

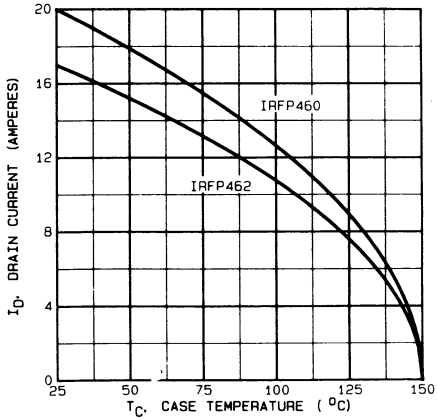


Fig. 13 - Maximum drain current vs. case temperature.

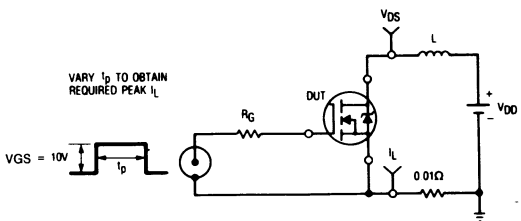


Fig. 14a - Unclamped inductive test circuit.

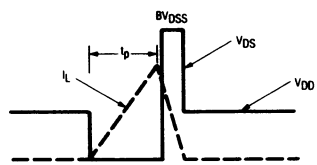


Fig. 14b - Unclamped inductive waveforms.

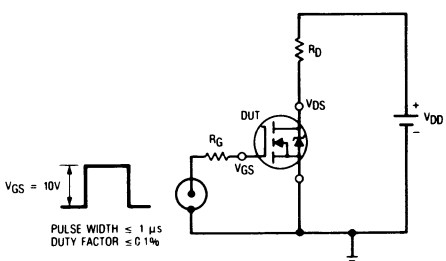


Fig. 15a - Switching time test circuit.

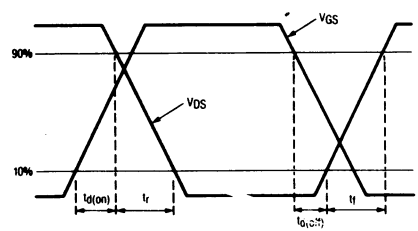


Fig. 15b - Switching time waveforms.

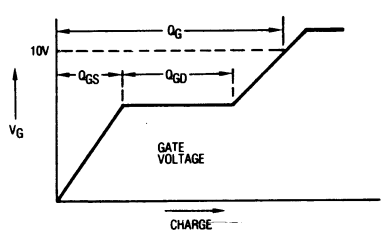


Fig. 16a - Basic gate charge waveform.

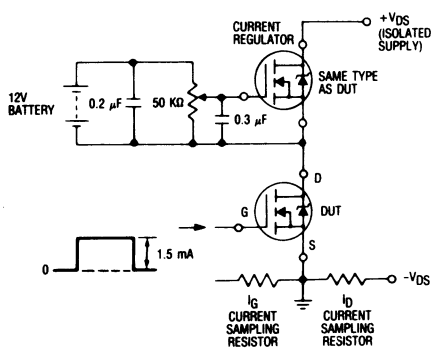


Fig. 16b - Gate charge test circuit.