IRF234, IRF235 IRF236, IRF237

N-Channel Power MOSFETs Avalanche-Energy Rated

May 1992

Features

- 8.1A and 6.5A, 275V - 250V
- $r_{DS}(on)$ = 0.45Ω and 0.68Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 275V, 250V Rating - 120V AC Line System Operation

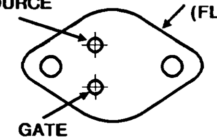
Description

The IRF234, IRF235, IRF236, and IRF237 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

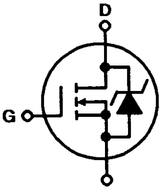
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		IRF234	IRF235	IRF236	IRF237	UNITS
Drain-Source Voltage (1)	V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	250	250	275	275	V
Continuous Drain Current						
T_C = +25°C	I_D	8.1	6.5	8.1	6.5	A
T_C = +100°C	I_D	5.1	4.1	5.1	4.1	A
Pulsed Drain Current (3)	I_{DM}	32	26	32	26	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
T_C = +25°C	P_D	75	75	75	75	W
Linear Derating Factor		0.6	0.6	0.6	0.6	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{AS}	180	180	180	180	mj
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

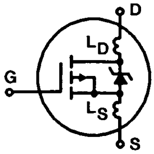
NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 4.5mH, R_{GS} = 25Ω, I_{PEAK} = 8.1A. See Figures 14 & 15.

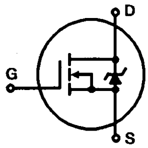
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **2208.2**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Drain-Source Breakdown Voltage IRF236, IRF237	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	275	-	-	V
IRF234, IRF235			250	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, I_D = -250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRF234, IRF236	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, V_{GS} = 10V	8.1	-	-	A
IRF235, IRF237			6.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF234, IRF236	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 4.1A	-	0.32	0.45	Ω
IRF235, IRF237			-	0.48	0.68	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} = 2 X V_{GS}, I_D = 4.1A	2.9	4.3	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	600	-	pF
Output Capacitance	C_{OSS}		-	180	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	52	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D = 8.1A, R_G = 12Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	9.1	14	ns
Rise Time	t_r		-	23	35	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	31	47	ns
Fall Time	t_f		-	19	29	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 8.1A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	24	35	nC
Gate-Source Charge	Q_{gs}		-	5.1	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	12	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of die. / Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{θJC}$		-	-	1.67	°C/W
Case-to-Sink	$R_{θCS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{θJA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	8.1	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	32	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 8.1A, V_{GS} = 0V	-	-	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 8.1A, dI_F/dt = 100A/μs	92	180	390	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 8.1A, dI_F/dt = 100A/μs	0.63	1.3	2.7	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 4.5mH, R_{GS} = 25Ω, I_{PEAK} = 8.1A (See Figures 14 & 15)

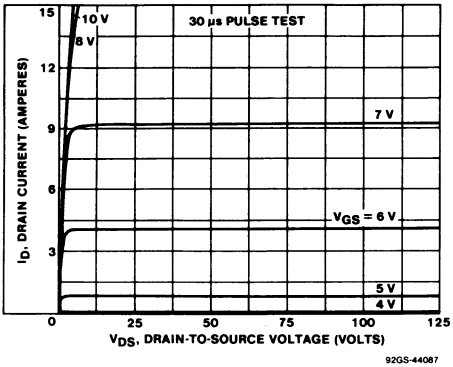


Fig. 1 - Typical output characteristics.

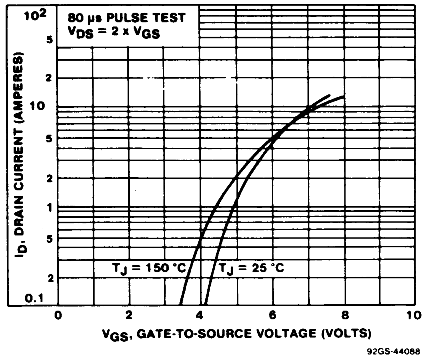


Fig. 2 - Typical transfer characteristics.

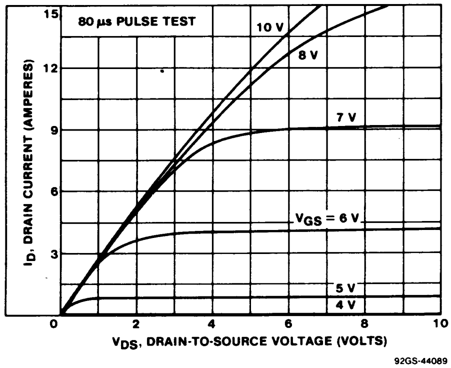


Fig. 3 - Typical saturation characteristics.

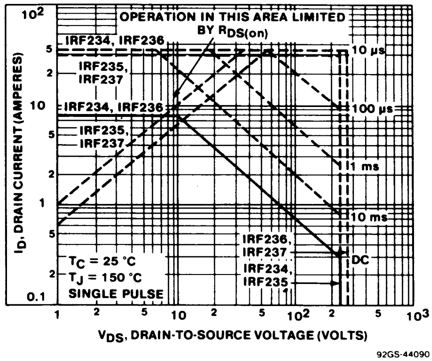


Fig. 4 - Maximum safe operating area.

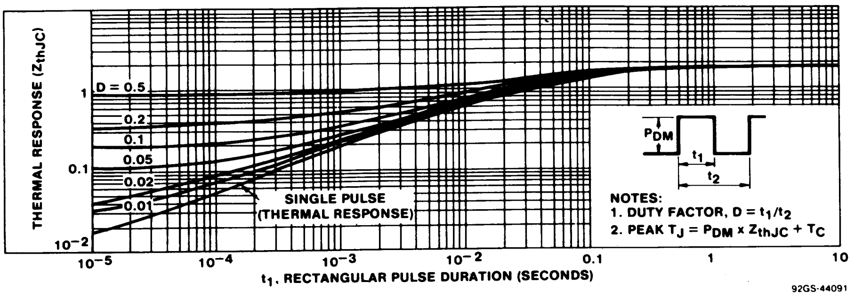


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

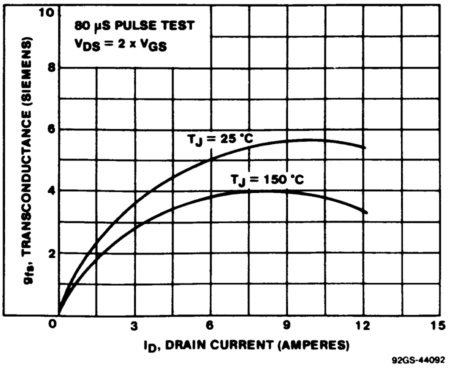


Fig. 6 - Typical transconductance vs. drain current.

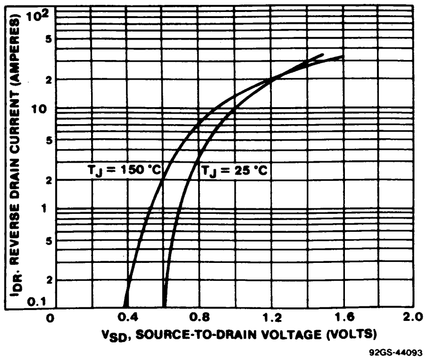


Fig. 7 - Typical source-drain diode forward voltage.

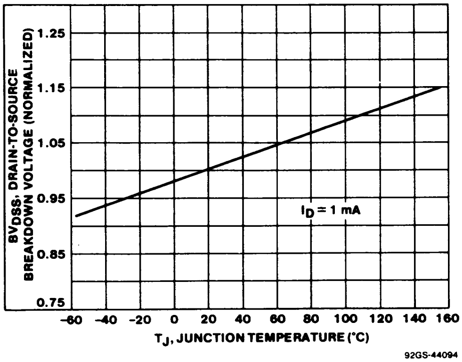


Fig. 8 - Breakdown voltage vs. temperature.

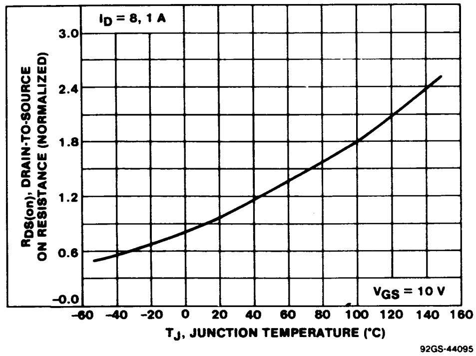


Fig. 9 - Normalized on-resistance vs. temperature.

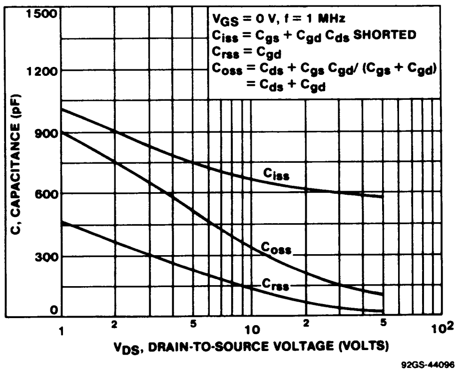


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

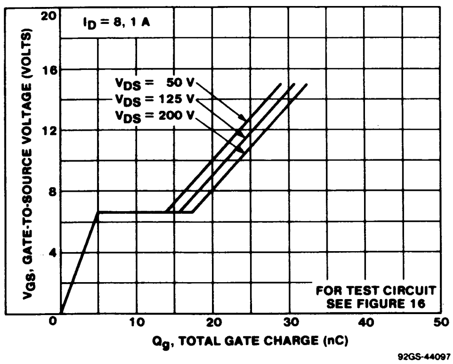


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

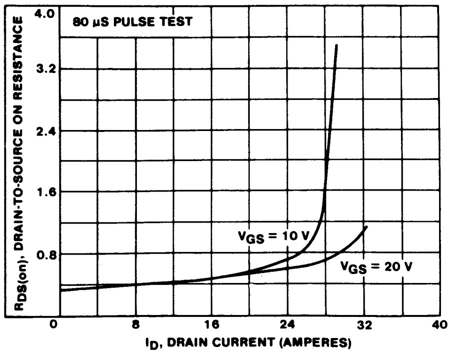


Figure 12. Typical On Resistance vs Drain Current

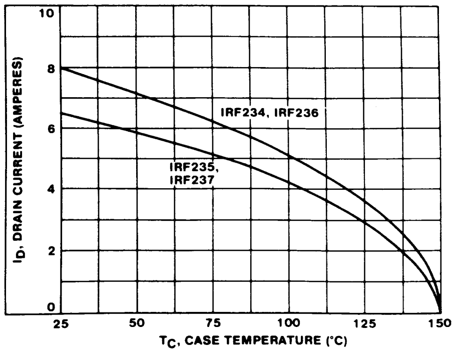


Figure 13. Maximum Drain Current vs Case Temperature

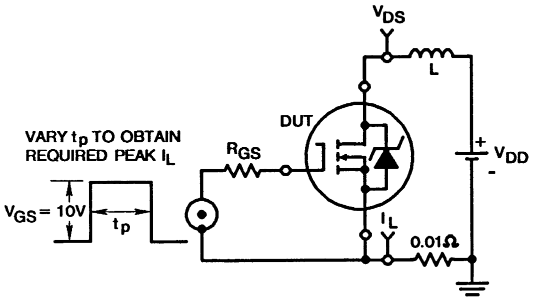


Figure 14. Unclamped Energy Test Circuit

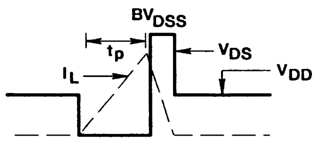


Figure 15. Unclamped Energy Waveforms

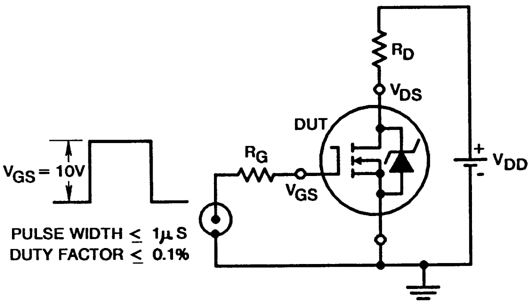


Figure16. Switching Time Test Circuit

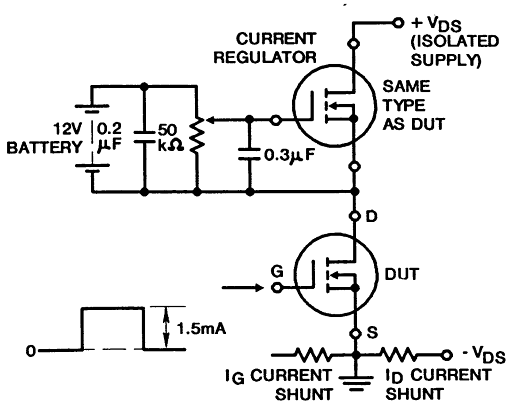


Figure 17. Gate Charge Test Circuit

4
N-CHANNEL
POWER MOSFETs

HARRIS

IRF244, IRF245
IRF246, IRF247

N-Channel Power MOSFETs
Avalanche Energy Rated

August 1991

Features

- 14A and 13A, 275V - 250V
- $r_{DS(on)} = 0.28\Omega$ and 0.34Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 275, 250V DC Rated - 120V AC Line System Operation

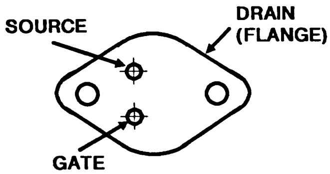
Description

The IRF244, IRF245, IRF246, and IRF247 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

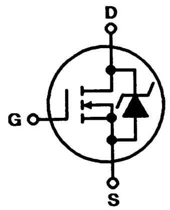
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$), Unless Otherwise Specified

		IRF244	IRF245	IRF246	IRF247	UNITS
Drain-Source Voltage (1)	V_{DS}	250	250	275	275	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$) (1)	V_{DGR}	250	250	275	275	V
Continuous Drain Current						
$T_C = +25^oC$	I_D	14	13	14	13	A
$T_C = +100^oC$	I_D	8.8	8.0	8.8	8.0	A
Pulsed Drain Current (3)	I_{DM}	56	52	56	52	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
$T_C = +25^oC$	P_D	125	125	125	125	W
Linear Derating Factor		1.0	1.0	1.0	1.0	W/^{o}C
Single Pulse Avalanche Energy Rating (4)	E_{as}	550	550	550	550	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^{o}C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	^{o}C

NOTES:

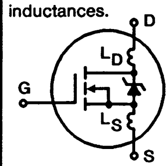
1. $T_J = +25^oC$ to $+150^oC$.
2. Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. $V_{DD} = 50V$, Starting $T_J = +25^oC$, $L = 4.5mH$, $R_G = 25\Omega$, Peak $I_L = 14A$ (See Figures 14 & 15).

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

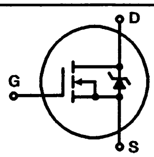
File Number **2209.1**

Specifications IRF244, IRF245, 1RF246, IRF247

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage IRF244, 1RF245	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	250	-	-	V
IRF246, IRF247			275	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRF244, IRF246	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, V_{GS} = 10V	14	-	-	A
1RF245, IRF247			13	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF244, IRF246	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 8A	-	0.20	0.28	Ω
1RF245. IRF247			-	0.24	0.34	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 8A	6.7	10	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	1300	-	pF
Output Capacitance	C_{OSS}		-	320	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	69	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D = 14A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	16	24	ns
Rise Time	t_r		-	67	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	53	80	ns
Fall Time	t_f		-	49	74	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 14A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	39	59	nC
Gate-Source Charge	Q_{gs}		-	6.6	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	20	-	nC
Internal Drain Inductance	L_D	Measured from the source lead, 6mm (0.25 in.) from package to center of die. / Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{θJC}$		-	-	1.0	°C/W
Case-to-Sink	$R_{θCS}$	Mounting surface flat, smooth and greased	-	0.5	-	°C/W
Junction-to-Ambient	$R_{θJA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	14	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	56	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 14A, V_{GS} = 0V	-	-	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 14A, dI_F/dt = 100A/μs	150	300	640	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 14A, dI_F/dt = 100A/μs	1.6	3.4	7.2	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, Starting T_J = +25°C, L = 4.5mH, R_G = 25Ω, Peak I_L = 14A (See Figures 14 & 15).

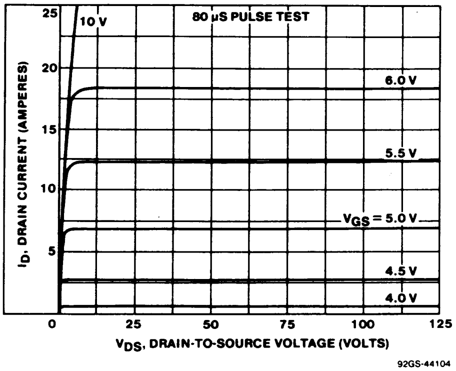


Fig. 1 - Typical output characteristics.

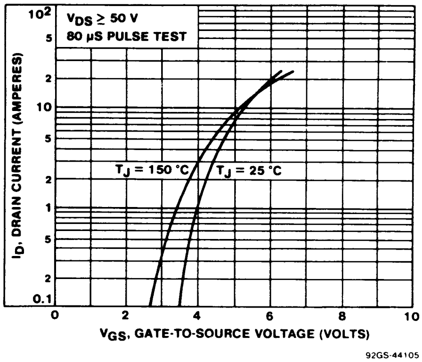


Fig. 2 - Typical transfer characteristics.

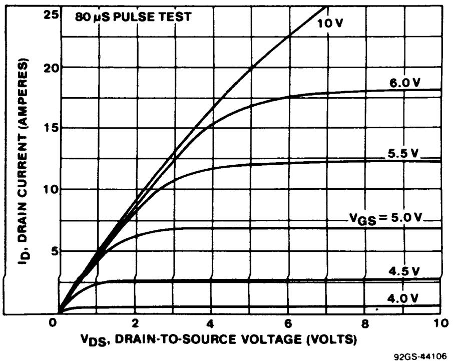


Fig. 3 - Typical saturation characteristics.

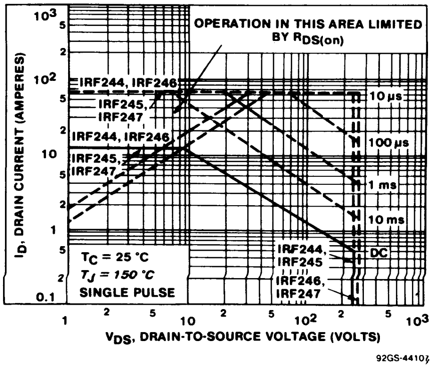


Fig. 4 - Maximum safe operating area.

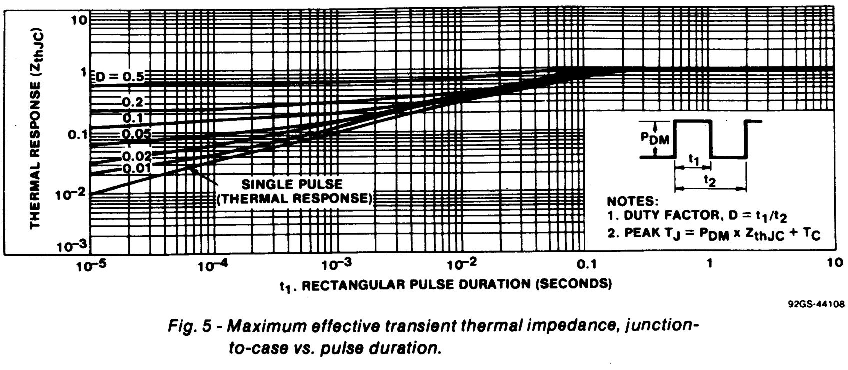


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

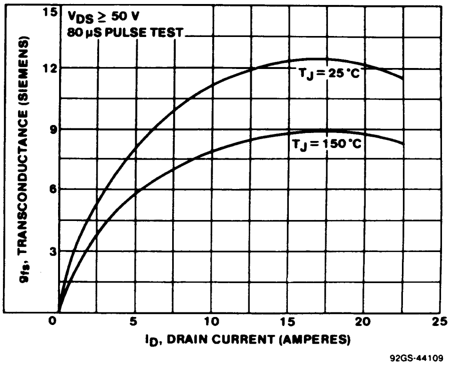


Fig. 6 - Typical transconductance vs. drain current.

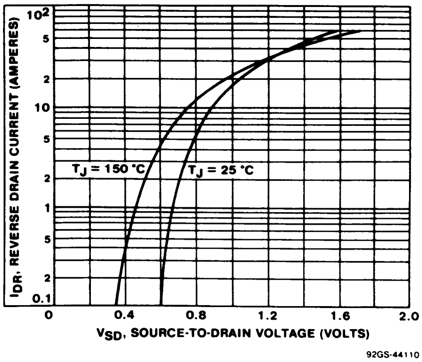


Fig. 7 - Typical source-drain diode forward voltage.

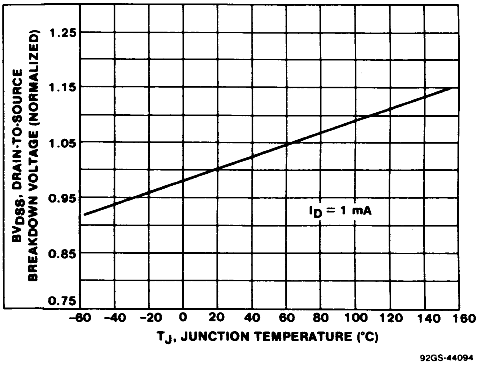


Fig. 8 - Breakdown voltage vs. temperature.

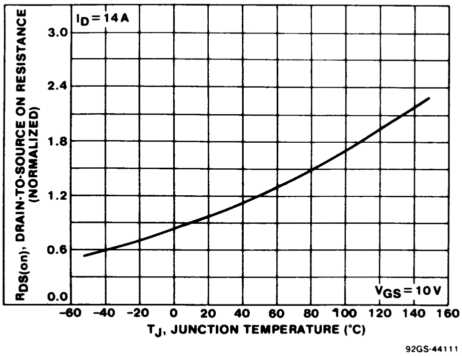


Fig. 9 - Normalized on-resistance vs. temperature.

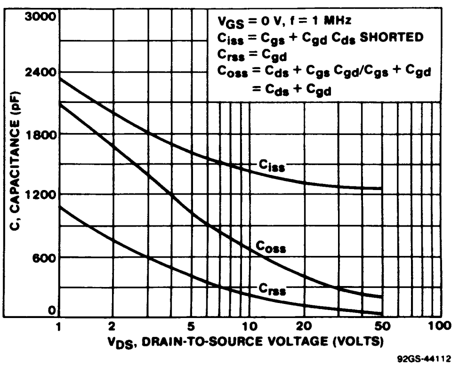


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

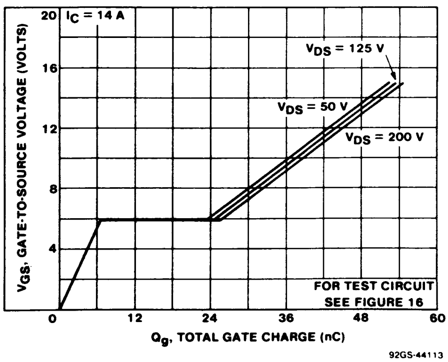


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

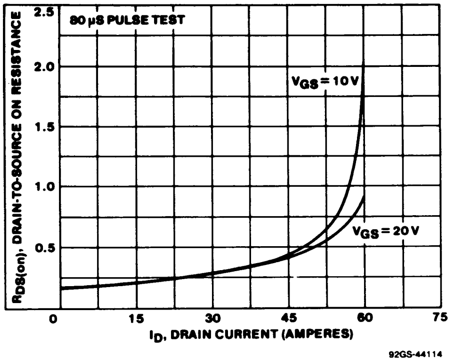


Figure 12. Typical On Resistance vs Drain Current

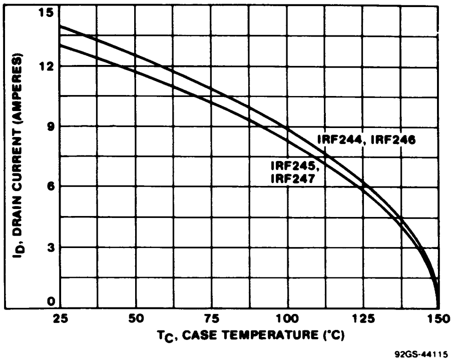


Figure 13. Maximum Drain Current vs Case Temperature

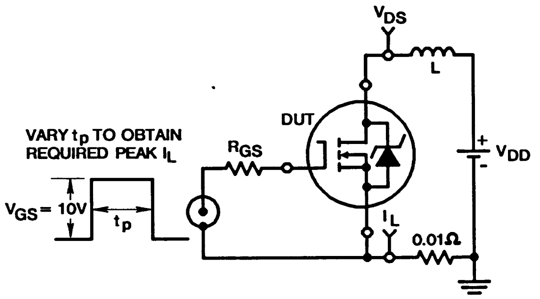


Figure 14. Unclamped Energy Test Circuit

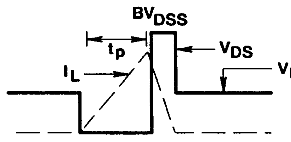


Figure 15. Unclamped Energy Waveforms

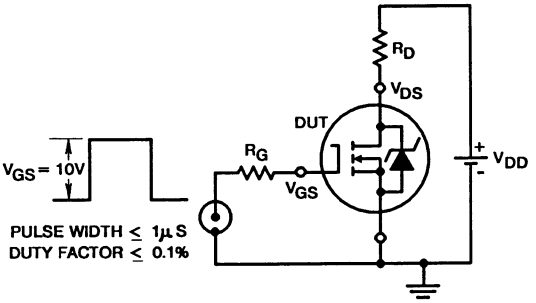


Figure16. Switching Time Test Circuit

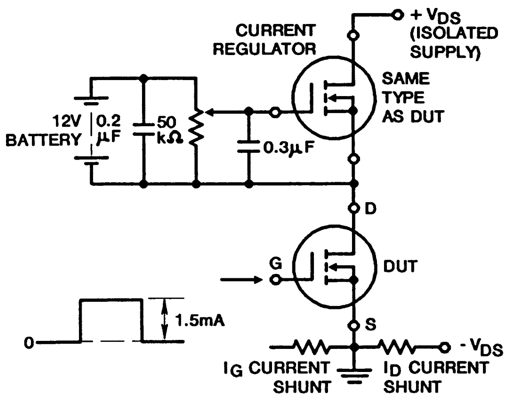


Figure 17. Gate Charge Test Circuit

IRF254, IRF255
IRF256, IRF257

N-Channel Power MOSFETs
Avalanche Energy Rated

August 1991

Features

- 22A and 20A, 275V - 250V
- $r_{DS(on)}$ = 0.14Ω and 0.17Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 275, 250V DC Rated - 120V AC Line System Operation

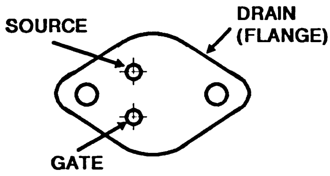
Description

The IRF254, IRF255, IRF256, and IRF257 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AE steel package.

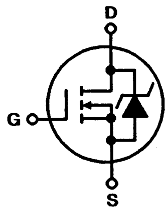
Package

TO-204AE
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRF254	IRF255	IRF256	IRF257	UNITS
Drain-Source Voltage (1)	V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	250	250	275	275	V
Continuous Drain Current						
T_C = +25°C	I_D	22	20	22	20	A
T_C = +100°C	I_D	14	12	14	12	A
Pulsed Drain Current (3)	I_{DM}	88	80	88	80	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
T_C = +25°C	P_D	150	150	150	150	W
Linear Derating Factor		1.2	1.2	1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{as}	1000	1000	1000	1000	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

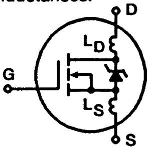
NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, Starting T_J = +25°C, L = 3.3mH, R_G = 25Ω, Peak I_L = 22A (See Figures 14 & 15).

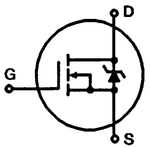
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **2300.2**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF254, 1RF255	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	250	-	-	V
IRF256, IRF257			275	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRF254, IRF256	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)\,Max}$, V_{GS} = 10V	22	-	-	A
1RF255, IRF257			20	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF254, IRF256	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 12A	-	0.11	0.14	Ω
1RF255. IRF257			-	0.14	0.17	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 12A	11	17	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	2700	-	pF
Output Capacitance	C_{OSS}		-	580	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	130	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D = 22A, R_G = 6.2Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	19	29	ns
Rise Time	t_r		-	84	130	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	75	110	ns
Fall Time	t_f		-	65	98	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 22A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	87	130	nC
Gate-Source Charge	Q_{gs}		-	14	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	73	-	nC
Internal Drain Inductance	L_D	Measured from the source lead, 6mm (0.25 in.) from package to center of die. — Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	13	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.10	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	22	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	88	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 22A, V_{GS} = 0V	-	-	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 22A, dI_F/dt = 100A/μs	150	310	650	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 22A, dI_F/dt = 100A/μs	1.9	4	8.4	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, Starting T_J = +25°C, L = 3.3mH, R_G = 25Ω, Peak I_L = 22A (See Figures 14 & 15).

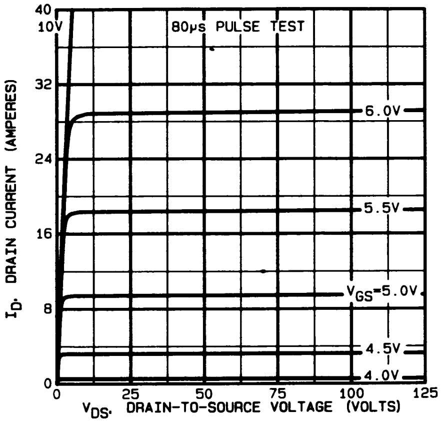


Fig. 1 - Typical output characteristics.

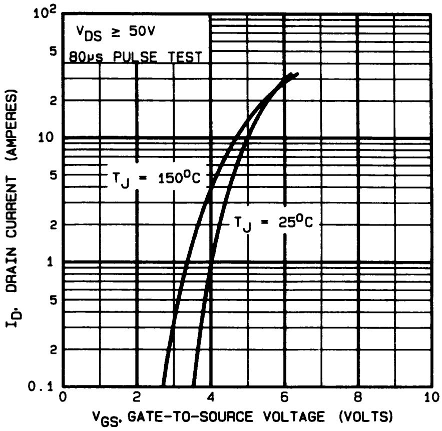


Fig. 2 - Typical transfer characteristics.

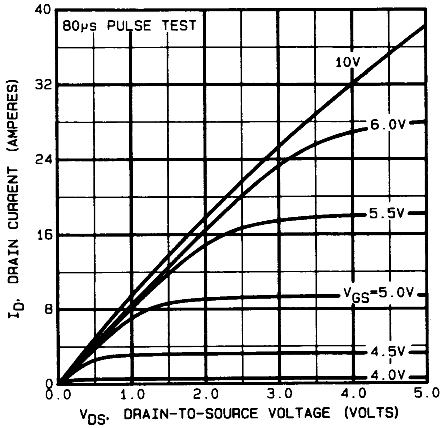


Fig. 3 - Typical saturation characteristics.

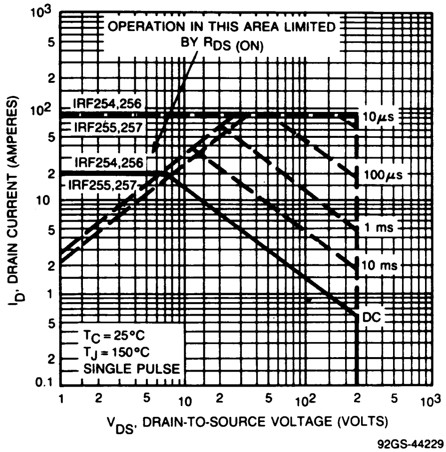


Fig. 4 - Maximum safe operating area.

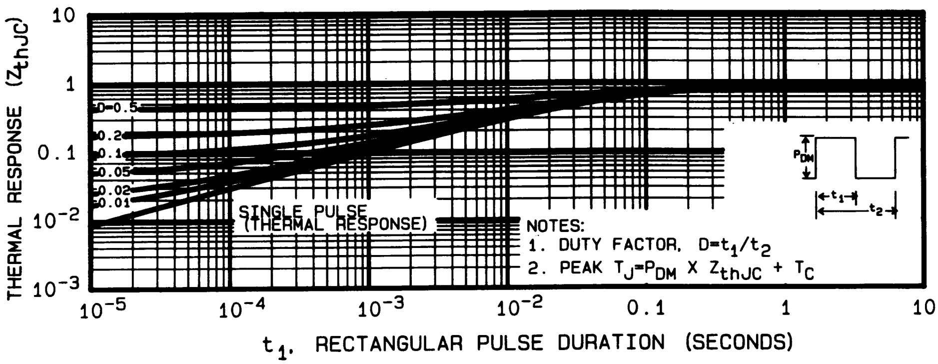


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

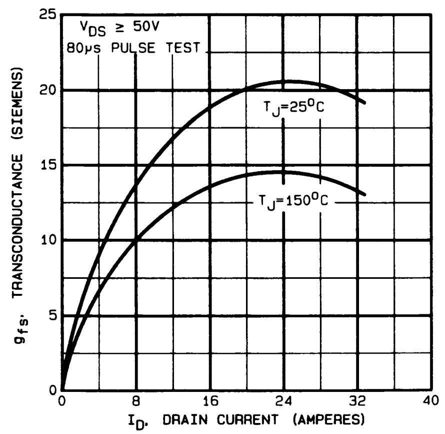


Fig. 6 - Typical transconductance vs. drain current.

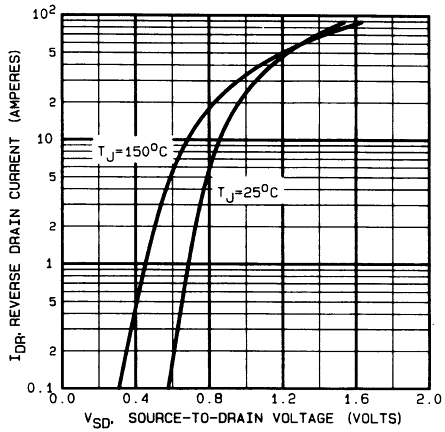


Fig. 7 - Typical source-drain diode forward voltage.

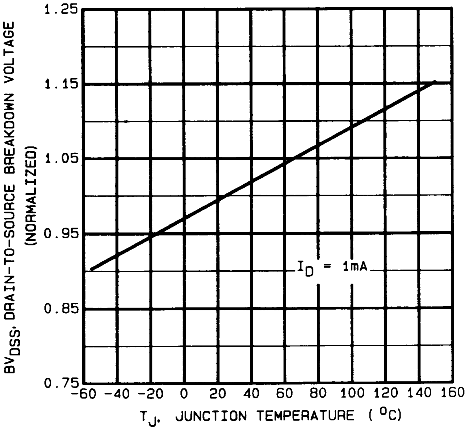


Fig. 8 - Breakdown voltage vs. temperature.

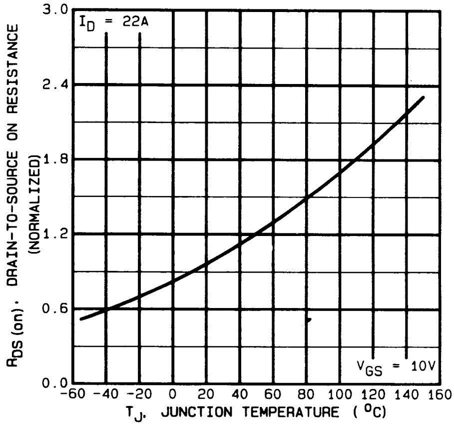


Fig. 9 - Normalized on-resistance vs. temperature.

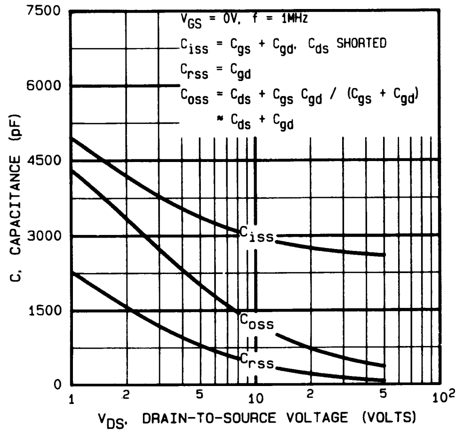


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

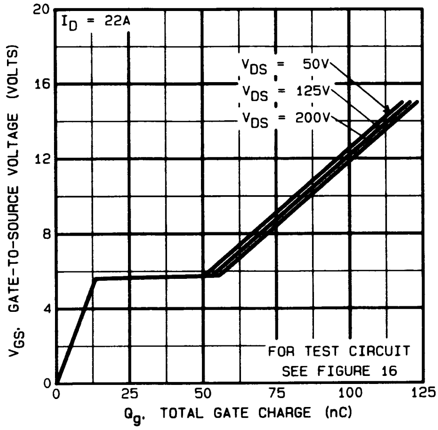


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

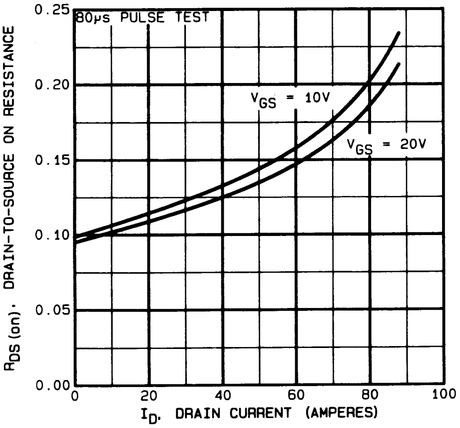


Figure 12. Typical On Resistance vs Drain Current

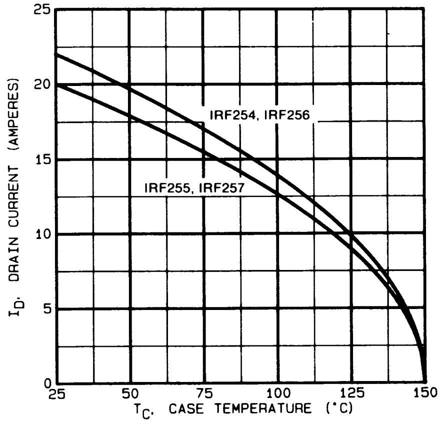


Figure 13. Maximum Drain Current vs Case Temperature

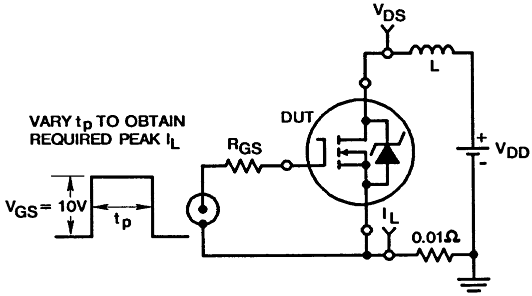


Figure 14. Unclamped Energy Test Circuit

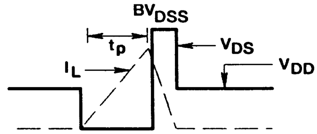


Figure 15. Unclamped Energy Waveforms

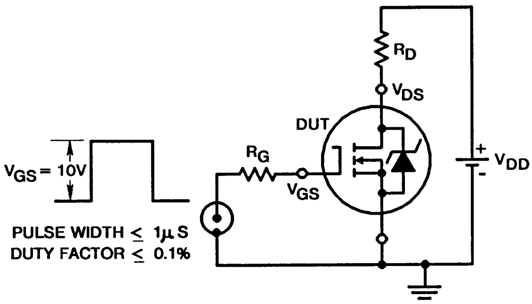


Figure16. Switching Time Test Circuit

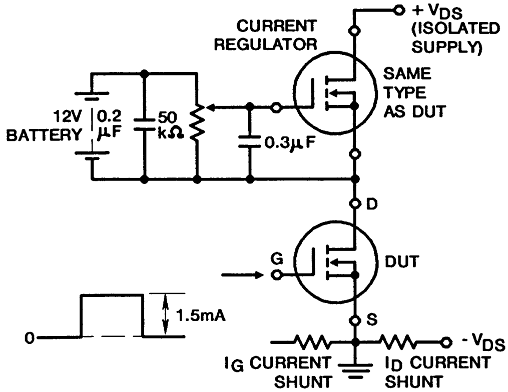


Figure 17. Gate Charge Test Circuit