FEATURES

- High h_{FE} at Low Current >200 @ 10 μA
- Low Output Capacitance <2.0 pf
- $I_{B_1} - I_{B_2}$ <2.5 nA
- Tight V_{BE} Tracking $<3.0\ \mu V/^{\circ}C$

GENERAL DESCRIPTION

Matched pairs for differential amplifiers.

DUAL MONOLITHIC MATCHED PNP SILICON PLANAR TRANSISTORS

IT130A IT130 IT131 IT132

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C

Maximum Power Dissipation

	TO-78		TO-71	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Total Dissipation at 25°C Case Temperature	0.4 Watt	0.75 Watt	0.3 Watt	0.5 Watt
Derating Factor	2.3mW/°C	4.3mW/°C	1.7mW/°C	2.9mW/°C

Maximum Voltage & Current for Each Transistor

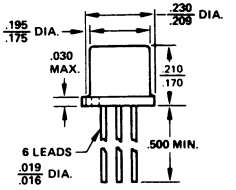
V_{CBO}	Collector to Base Voltage	45 V
V_{CEO}	Collector to Emitter Voltage	45 V
V_{EBO}	Emitter to Base Voltage	7.0 V
V_{CCO}	Collector to Collector Voltage	60 V
I_C	Collector Current	50 mA

ORDERING INFORMATION

TO78	TO71	WAFER	CHIP
IT130A	IT130A-TO71	IT130A/W	IT130A/D
IT130	IT130-TO71	IT130/W	IT130/D
IT131	IT131-TO71	IT131/W	IT131/D
IT132	IT132-TO71	IT132/W	IT132/D

PACKAGE DIMENSIONS

TO-71



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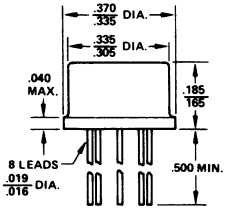
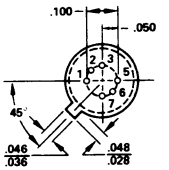
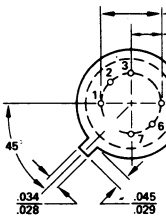
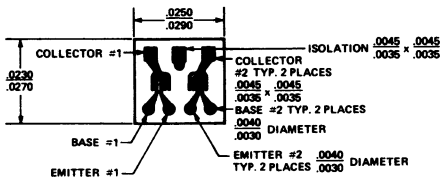






PIN	OUT
1	C_1
2	B_1
3	E_1
5	E_2
6	B_2
7	C_2

4503



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		IT130A		IT130		IT131		IT132		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	200		200		80		80			I_C = 10 μA, V_{CE} = 5.0 V
h_{FE}	DC Current Gain	225		225		100		100			I_C = 1.0 mA, V_{CE} = 5.0 V
h_{FE}(−55°C)	DC Current Gain	75		75		30		30			I_C = 10 μA, V_{CE} = 5.0 V
V_{BE}(ON)	Emitter-Base On Voltage		0.7		0.7		0.7		0.7	V	I_C = 10 μA, V_{CE} = 5.0 V
V_{CE}(SAT)	Collector Saturation Voltage		0.5		0.5		0.5		0.5	V	I_C = 0.5 mA, I_B = 0.05 mA
I_{CBO}	Collector Cutoff Current		−1.0		−1.0		−1.0		−1.0	nA	I_E = 0, V_{CB} = 45 V
I_{CBO}(+150°C)	Collector Cutoff Current		−10		−10		−10		−10	μA	I_E = 0, V_{CB} = 45 V
I_{EBO}	Emitter Cutoff Current		−1.0		−1.0		−1.0		−1.0	nA	I_C = 0, V_{EB} = 5.0 V
C_{OB}	Output Capacitance		2.0		2.0		2.0		2.0	pF	I_E = 0, V_{CB} = 5.0 V
C_{TE}	Emitter Transition Capacitance		2.5		2.5		2.5		2.5	pF	I_C = 0, V_{EB} = 0.5 V
$C_{C_1 \cdot C_2}$	Collector to Collector Capacitance		4.0		4.0		4.0		4.0	pF	V_{CC} = 0
$I_{C_1 \cdot C_2}$	Collector to Collector Leakage Current		10		10		10		10	nA	V_{CC} = ±60 V
V_{CEO}(SUST)	Collector to Emitter Sustaining Voltage	−45		−45		−45		−45		V	I_C = 1.0 mA, I_B = 0
f_T	Current Gain	5		5		4		4		MHz	I_C = 10 μA, V_{CE} = 5 V
	Bandwidth Product	110		110		90		90		MHz	I_C = 1 mA, V_{CE} = 5 V
$\lvert V_{BE_1} - V_{BE_2} \rvert$	Base Emitter Voltage Differential		1		2		3		5	mV	I_C = 10 μA, V_{CE} = 5.0 V
$\lvert I_{B_1} - I_{B_2} \rvert$	Base Current Differential		2.5		5		25		25	nA	I_C = 10 μA, V_{CE} = 5.0 V
$\lvert \Delta(V_{BE_1} - V_{BE_2}) \rvert$	Base-Emitter Voltage Differential Change with Temperature		3		5		10		20	μV/°C	T_A = −55°C to +125°C, I_C = 10 μA, V_{CE} = 5.0 V

NOTES:

(1) These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

(2) The lowest of two h_{FE} readings is taken as h_{FE_1} for purposes of this ratio.

FEATURES

- High Gain at Low Current – $h_{FE} \geq 200$ @ 1mA
- Low Output Capacitance – $C_{obo} < 3$ pf
- Tight I_B Match – $I_{B_1 - 2} < .25\ \mu A$ @ 1 mA – 5V
- Tight V_{BE} Tracking – $\Delta(V_{BE_1} - V_{BE_2}) \leq 3\ \mu V/°C$ −55°C to + 125°C
- Dielectrically isolated matched pairs for differential amplifiers.

DUAL MONOLITHIC PNP SILICON PLANAR TRANSISTORS

IT136 IT137 IT138 IT139

GENERAL DESCRIPTION

Dual monolithic PNP silicon planar transistors used for differential amplifier applications.

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C

Maximum Power Dissipation

	TO71		TO78	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Total Dissipation @ 25°C Case Temperature	0.3 Watt	0.5 Watt	0.4 Watt	0.75 Watt
Derating Factor	1.7mW/°C	2.9mW/°C	2.3mW/°C	4.3mW/°C

Maximum Voltage and Current for Each Transistor

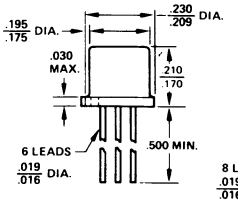
V_{CBO}	Collector to Base Voltage	60V	55V	45V
V_{CEO}	Collector to Emitter Voltage	60V	55V	45V
V_{EBO}	Emitter to Base Voltage (Note 2)	7V	7V	7V
V_{CCO}	Collector to Collector Voltage	70V	70V	70V
I_C	Collector Current	100mA	100mA	100mA

ORDERING INFORMATION

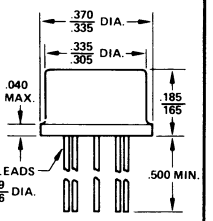
TO78	TO71	WAFER	CHIP
IT136	IT136-TO71	IT136/W	IT136/D
IT137	IT137-TO71	IT137/W	IT137/D
IT138	IT138-TO71	IT138/W	IT138/D
IT139	IT139-TO71	IT139/W	IT139/D

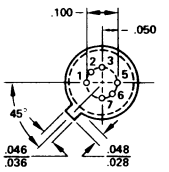
PACKAGE DIMENSIONS

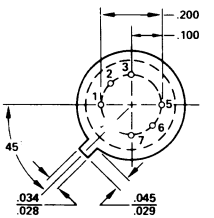
TO-71



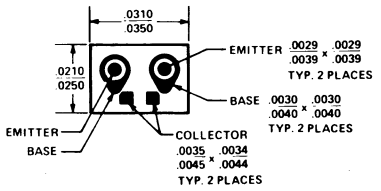
TO-78







1. Collector
2. Base
3. Emitter
5. Emitter
6. Base
7. Collector



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ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

PARAMETER		IT136		IT137		IT138		IT139		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	150		150		100		70			I_C = 10 μA, V_{CE} = 5V
h_{FE}	DC Current Gain	150	800	150	800	100	800	70	800		I_C = 1.0 mA, V_{CE} = 5V
h_{FE}	DC Current Gain	125	230	125		80		50			I_C = 10 mA, V_{CE} = 5V
h_{FE}	DC Current Gain	65		60		40		25			I_C = 50 mA, V_{CE} = 5V
h_{FE}(−55°C)	DC Current Gain	75		75		60		40			I_C = 1 mA, V_{CE} = 5V
$V_{BE(on)}$	Emitter - Base On Voltage		.9		.9		.9		.9	V	I_C = 10 mA, V_{CE} = 5V
			1.0		1.0		1.0		1.0	V	I_C = 50 mA, V_{CE} = 5V
$V_{CE(sat)}$	Collector Saturation Voltage		.3		.3		.3		.3	V	I_C = 1 mA, I_B = .1 mA
			.6		.6		.6		.6	V	I_C = 10 mA, I_B = 1 mA
I_{CBO}	Collector Cutoff Current		0.1		0.1		0.1		0.1*	nA	I_E = 0, V_{CB} = 45V, 30V*
I_{CBO}(+150°C)	Collector Cutoff Current		.1		0.1		0.1		0.1*	μA	I_E = 0, V_{CB} = 45V, 30V*
I_{EBO}	Emitter Cutoff Current		.1		0.1		0.1		0.1	nA	I_C = 0, V_{EB} = 5V
C_{obo}	Output Capacitance		3		3		3		3	pF	I_E = 0, V_{CB} = 20V