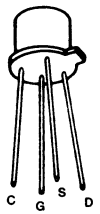
IT1700
P-Channel Enhancement Mode MOSFET General Purpose Amplifier

INTERSIL

FEATURES
- **Low ON-Resistance**
- **High Gain**
- **Low Noise Voltage**
- **High Input Impedance**
- **Low Leakage**

PIN CONFIGURATION

TO-72



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ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain-Source and Gate-Source Voltage ..... −40V
Peak Gate-Source Voltage (Note 1) ..... ±125V
Drain Current 50mA
Storage Temperature ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 375mW
Derate above 25°C ..... 3mW/°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ORDERING INFORMATION

TO-72
IT1700

ELECTRICAL CHARACTERISTICS (T_A = 25°C and V_{BS} = 0 unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0, I_D = −10μA	−40		V
BV_{SDS}	Source to Drain Breakdown Voltage	V_{GS} = 0, I_D = −10μA	−40		V
I_{GSS}	Gate Leakage Current		(See note 2)		
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0, V_{DS} = −20V		200	pA
I_{DSS} (150°C)	Drain to Source Leakage Current			0.4	μA
I_{SDS}	Source to Drain Leakage Current			400	pA
I_{SDS} (150°C)	Source to Drain Leakage Current			0.8	μA
V_{GS}(th)	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = −10μA	−2	−5	V
$r_{DS(on)}$	Static Drain to Source "on" Resistance	V_{GS} = −10V, V_{DS} = 0		400	ohms
I_{DS}(on)	Drain to Source "on" Current	V_{GS} = −10V, V_{DS} = −15V	2		mA
g_{fs}	Forward Transconductance Common Source	V_{DS} = −15V, I_D = −10mA f = 1kHz	2000	4000	μs
C_{iss}	Small Signal, Short Circuit, Common Source, Input Capacitance	V_{DS} = −15V, I_D = −10mA f = 1MHz (Note 3)		5	pF
C_{rss}	Small Signal, Short Circuit, Common Source, Reverse Transfer Capacitance	V_{DG} = −15V, I_D = 0 f = 1MHz (Note 3)		1.2	pF
C_{oss}	Small Signal, Short Circuit, Common Source, Output Capacitance	V_{DS} = −15V, I_D = −10mA f = 1MHz (Note 3)		3.5	pF

NOTES: 1. Device must not be tested at ±125V more than once nor longer than 300ms.
2. Actual gate current is immeasurable. Package suppliers are required to guarantee a package leakage of < 10pA. External package leakage is the dominant mode which is sensitive to both transient and storage environment, which cannot be guaranteed.
3. For design reference only, not 100% tested.

FEATURES

- High Input Impedance – 10^{15} ohms
- Low Leakage – $I_{DSS} \leq 200$ pA
- Low On-Resistance – $r_{DS(on)} \leq 400$ ohms
- Low Noise Voltage – e_n 150 nV/√Hz typical @ 100 Hz
- High Gain – $Y_{fs} \geq 2000 \leq 4000$ μmhos

P-CHANNEL ENHANCEMENT MODE MOS FET

IT1700

ABSOLUTE MAXIMUM RATINGS (Note 1)
@ 25°C (unless otherwise noted)

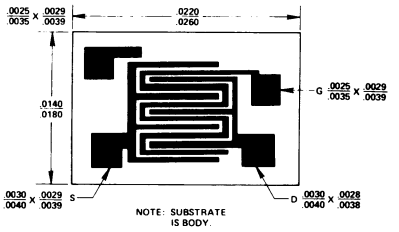
Maximum Temperatures	
Storage Temperature	-65°C to +200°C
Operating Junction Temperature	-55°C to +150°C
Lead Temperature (soldering, 10 second time limit)	+300°C
Maximum Power Dissipation	
Total Dissipation at 25°C Ambient Temperature	0.375 W
Linear Derating Factor at 25°C Ambient Temperature	3 mW/°C
Total Dissipation at 25°C Case Temperature	1.25 W
Linear Derating Factor at 25°C Case Temperature	10 mW/°C
Maximum Voltages and Current	
V_{DSS} Drain to Source and Body Voltage	-40 V
V_{SDS} Source to Drain and Body Voltage	-40 V
V_{GSS} Transient Gate to Source Voltage (Note 2)	±125 V
V_{GSS} Gate to Source Voltage	-40 V
$I_{D(on)}$ Drain Current	50 mA

ORDERING INFORMATION

TO72	WAFER	CHIP
IT1700	IT1700/W	IT1700/D

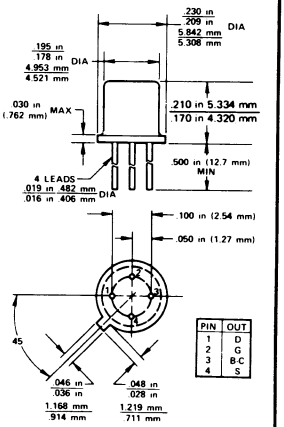
PACKAGE DIMENSIONS

1503



NOTE: SUBSTRATE IS BODY.

TO-72



PIN	OUT
1	D
2	G
3	B-C
4	S

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
BV_{DSS}	Drain to Source Breakdown Voltage	-40		V	V_{GS} = 0, I_D = -10 μA
BV_{SDS}	Source to Drain Breakdown Voltage	-40		V	V_{GS} = 0, I_D = -10 μA
I_{GSS}	Gate Leakage Current				(See Note 2)
I_{DSS}	Drain to Source Leakage Current		200	pA	V_{GS} = 0, V_{DS} = -20 V
I_{DSS} (150°C)	Drain to Source Leakage Current		0.4	μA	V_{GS} = 0, V_{DS} = -20 V
I_{SDS}	Source to Drain Leakage Current		400	pA	V_{GS} = 0, V_{DS} = -20 V
I_{SDS} (150°C)	Source to Drain Leakage Current		0.8	μA	V_{GS} = 0, V_{DS} = -20 V
$V_{GS(th)}$	Gate Threshold Voltage	-2	-5	V	V_{GS} = V_{DS}, I_D = -10 μA

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
$r_{DS(on)}$	Static Drain to Source "on" Resistance			400	ohms	V_{GS} = -10 V, V_{DS} = 0
$I_{DS(on)}$	Drain to Source "on" Current	2			mA	V_{GS} = -10 V, V_{DS} = -15 V
Y_{fs}	Forward Transconductance Common Source	2000		4000	μmhos	V_{DS} = -15 V, I_D = -10 mA f = 1 kHz
C_{iss}	Small Signal, Short Circuit, Common Source, Input Capacitance			5	pF	V_{DS} = -15 V, I_D = -10 mA f = 1 MHz
C_{rss}	Small Signal, Short Circuit, Common Source, Reverse Transfer Capacitance			1.2	pF	V_{DG} = -15 V, I_D = 0 f = 1 MHz
C_{oss}	Small Signal, Short Circuit, Common Source, Output Capacitance			3.5	pF	V_{DS} = -15 V, I_D = -10 mA f = 1 MHz
$\overline{e_n}$	Equivalent Input Noise Voltage		150		nV/√Hz	V_{DS} = -15 V, I_D = -1 mA f = 100 Hz; BW = Hz

NOTE:

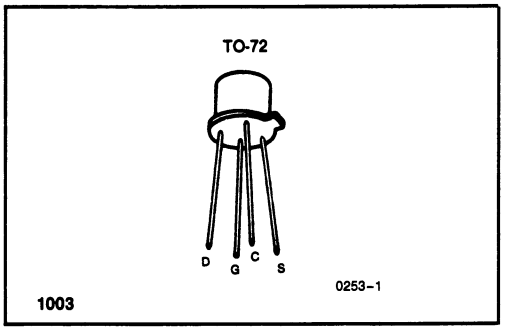
1. These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.
2. Actual gate current is immeasurable. Package suppliers are required to guarantee a package leakage of < 10 pA. External package leakage is the dominant mode which is sensitive to both transient and storage environment, which cannot be guaranteed.

IT1750
N-Channel Enhancement Mode MOSFET General Purpose Amplifier Switch

INTERSIL

FEATURES
- **Low ON Resistance**
- **Low C_{dg}**
- **High Gain**
- **Low Threshold Voltage**

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Drain-Source and Gate-Source Voltage 25V
Peak Gate-Source Voltage (Note 1) ..... ±125V
Drain Current 100mA
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 375mW
Derate above 25°C ..... 3mW/°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ORDERING INFORMATION

TO-72
IT1750

ELECTRICAL CHARACTERISTICS
(T_A = 25°C, Body connected to Source and V_{BS} = 0 unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 10\mu A$	0.50	3.0	V
I_{DSS}	Drain Leakage Current	$V_{DS} = 10V$, $V_{GS} = 0$		10	nA
I_{GSS}	Gate Leakage Current		See note 2.		
BV_{DSS}	Drain Breakdown Voltage	$I_D = 10\mu A$, $V_{GS} = 0$	25		V
$r_{DS(on)}$	Drain To Source on Resistance	$V_{GS} = 20V$		50	ohms
$I_{D(on)}$	Drain Current	$V_{DS} = V_{GS} = 10V$	10		mA
Y_{fs}	Forward Transadmittance	$V_{DS} = 10V$, $I_D = 10mA$, $f = 1kHz$	3,000		μs
C_{iss}	Total Gate Input Capacitance	$I_D = 10mA$, $V_{DS} = 10V$, $f = 1MHz$ (Note 3)		6.0	pF
C_{dg}	Gate to Drain Capacitance	$V_{DG} = 10V$, $f = 1MHz$ (Note 3)		1.6	pF

NOTES: 1. Devices must not be tested at ±125V more than once nor longer than 300ms.
2. Actual gate current is immeasurable. Package suppliers are required to guarantee a package leakage of <10pA. External package leakage is the dominant mode which is sensitive to both transient and storage environment, which cannot be guaranteed.
3. For design reference only, not 100% tested.

N-CHANNEL
ENHANCEMENT
MODE MOS FET

IT1750

FEATURES

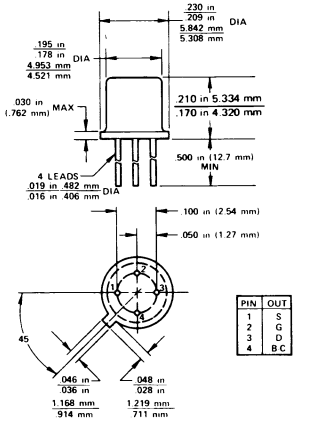
- Low On-Resistance – 50Ω
- Low Capacitance – 1.7 pF
- High Grain – 3,000 μmhos
- High Gate Breakdown Voltage – ±125V
- Low Threshold Voltage – 3 V

ORDERING INFORMATION

TO72	WAFER	CHIP
IT1750	IT1750/W	IT1750/D

PACKAGE DIMENSIONS

TO-72



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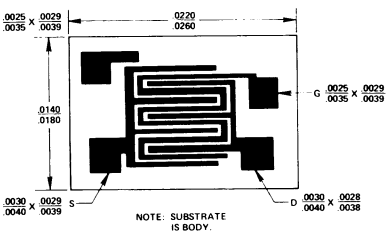

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures

Operating Junction Temperature	-55°C to +150°C

Maximum Power Dissipation

Total Dissipation at 25°C Ambient Temp.	0.375 W
Linear Derating Factor at 25°C Ambient Temp.	3 mW/°C

Maximum Voltages and Current

V_{DSS}	Drain to Source and Body Voltage	25 V
V_{GSS}	Transient Gate to Source Voltage	±125 V
$I_{D(on)}$	Drain Current	100 mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Body connected to Source unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS
$V_{GS(TH)}$	Gate to Source Threshold Voltage	0.50	1.5	3.0	V	$V_{DS} = V_{GS}$, I_D = 10 μA, V_{BS} = 0
I_{DSS}	Drain Leakage Current		0.1	10	nA	V_{DS} = 10 V, $V_{GS} = V_{BS}$ = 0
I_{GSS}	Gate Leakage Current					(See Note 2)
BV_{DSS}	Drain Breakdown Voltage	25			V	I_D = 10 μA, $V_{GS} = V_{BS}$ = 0
$R_{DS(on)}$	Drain To Source on Resistance		25	50	ohms	V_{GS} = 20 V, V_{BS} = 0
$I_{D(on)}$	Drain Current	10	50		mA	$V_{DS} = V_{GS}$ = 10 V, V_{BS} = 0
Y_{fs}	Forward Transadmittance	3,000			μmhos	V_{DS} = 10 V, I_D = 10 mA, f = 1 KHz, V_{BS} = 0
C_{iss}	Total Gate Input Capacitance		5.0	6.0	pF	I_D = 10 mA, V_{DS} = 10 V, f = 1 MHz, V_{BS} = 0
C_{dg}	Gate to Drain Capacitance		1.3	1.6	pF	V_{DG} = 10 V, V_{BS} = 0