Monolithic Dual Cascoded N-Channel JFET General Purpose Amplifier

calogic CORPORATION

IT500 – IT505

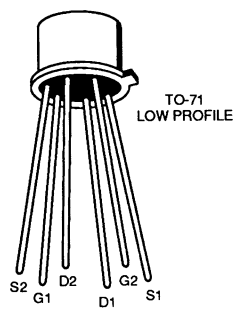
GENERAL DESCRIPTION

A low noise, low leakage FET that employs a cascode structure to accomplish very low I_G at high voltage levels, while giving high transconductance and very high common, mode rejection ratio.

FEATURES

- C_{MRR}>120dB
- I_G<5pA @ 50V_{DG}
- C_{rss}<0.5pF
- g_{os}>.025μs

PIN CONFIGURATION



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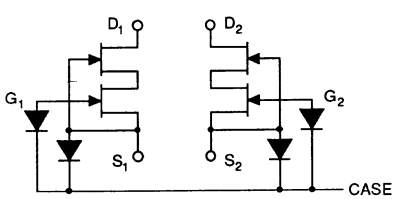
SCHEMATIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified)

Drain-Source and Drain-Gate Voltages (Note 1) 60V
Drain Current (Note 1) 50mA
Gate-Gate Voltage ..... ±60V
Storage Temperature ..... -65°C to +200°C
Operating Temperature ..... -55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

	One Side	Both Sides
Power Dissipation (Note 3)	250mW	500mW
Derate above 25°C	3.8mW/°C	7.7mW/°C

NOTE 1. Per transistor.

NOTE 2. Due to the non-symmetrical structure of these devices, the drain and source ARE NOT interchangeable.

NOTE 3. @85°C free air temp.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Part	Package	Temperature Range
IT500	Hermetic TO-71	-55°C to +150°C
IT501	Hermetic TO-71	-55°C to +150°C
IT502	Hermetic TO-71	-55°C to +150°C
IT503	Hermetic TO-71	-55°C to +150°C
IT504	Hermetic TO-71	-55°C to +150°C
IT505	Hermetic TO-71	-55°C to +150°C
XIT505	Sorted Chips in Carriers	-55°C to +150°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -20V, V_{DS} = 0, T_A = 125°C	
			-5	nA		
BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = -1μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.7	-4		V_{DS} = 20V, I_D = 1nA	
V_{GS}	Gate-Source Voltage	-0.2	-3.8			
I_G	Gate Operating Current		-5	pA	V_{DG} = 35V, I_D = 200μA, T_A = 125°C	
			-5	nA		
I_{DSS}	Saturation Drain Current (Note 1)	0.7	7	mA	V_{DS} = 20V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance (Note 1)	1000	4000	μs	V_{DS} = 20V, V_{GS} = 0	f = 1kHz
g_{fs}	Common-Source Forward Transconductance (Note 1)	500	1600		V_{DG} = 20V, I_D = 200μA	
g_{os}	Common-Source Output Conductance		1		V_{DS} = 20V, V_{GS} = 0	
g_{os}	Common-Source Output Conductance		0.025		V_{DS} = 20V, I_D = 200μA	
C_{g1g2}	Gate to Gate Capacitance (Note 4)		3.5	pF	V_{G1} = V_{G2} = 10V	f = 1MHz
C_{iss}	Common-Source Input Capacitance (Note 4)		7	pF	V_{DS} = 20V, V_{GS} = 0	
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 3, 4)		0.5			
NF	Spot Noise Figure (Note 4)		0.5	dB		f = 100Hz, R_G = 10MΩ
$\bar{e}_n$	Equivalent Input Noise Voltage (Note 4)		50	$\frac{\mu V}{\sqrt{Hz}}$		f = 10Hz
			15			f = 1kHz

SYMBOL	PARAMETER	IT500		IT501		IT502		IT503		IT504		IT505		UNITS	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current		5		5		5		5		10		15	nA	V_{DG} = 20V, I_D = 200μA, T_A = 125°C	
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 1)	0.95	1	0.95	1	0.95	1	0.95	1	0.90	1	0.85	1		V_{DS} = 20V, V_{GS} = 0	
g_{fs1} / g_{fs2}	Transconductance Ratio (Note 1)	0.97	1	0.97	1	0.95	1	0.95	1	0.90	1	0.85	1			f = 1kHz
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		5		5		10		15		25		50	mV		
$\frac{\Delta V_{GS1} - V_{GS2}}{\Delta T}$	Gate-Source Differential Voltage		5		10		20		40		100		200	μV/°C	V_{DG} = 20V I_D = 200μA	T_A = 25°C T_B = 125°C
	Change with Temp. (Note 2, 4)		5		10		20		40		100		200			T_A = -55°C T_B = 25°C
C_{MRR} (Note 5)	Common Mode Rejection Ratio (Note 4)	120		120		120		120		120		120		dB	Δ V_{DD} = 10V, I_D = 200μA	

NOTES: 1. Pulse test required, pulsewidth = 300μs, duty cycle ≤3%.
2. Measured at end points, T_A and T_B.
3. With case guarded C_{rss} is typically <0.15pF.
4. For design reference only, not 100% tested.
5. C_{MRR} = 20 $\log_{10}\Delta VDD / \Delta$ [Vgs1 - Vgs2], ΔV_{DD} = 10/ -20V.

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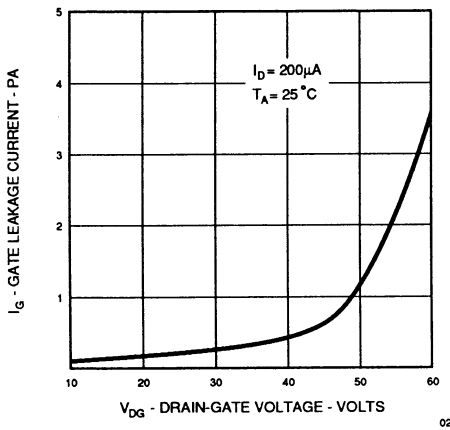
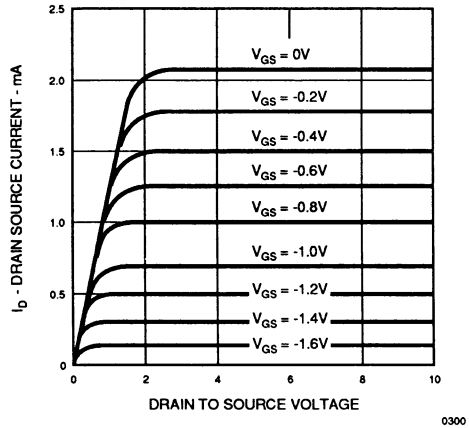
TYPICAL PERFORMANCE CHARACTERISTICS

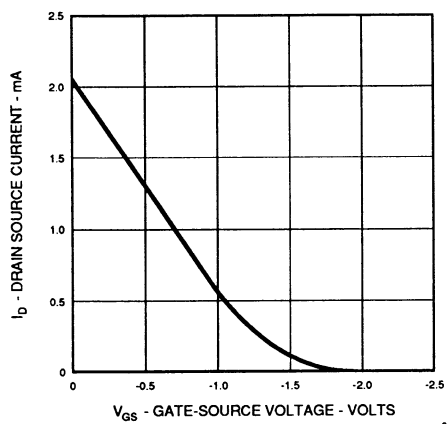
GATE LEAKAGE



OUTPUT CHARACTERISTICS



OUTPUT CHARACTERISTICS



TYPICAL CAPACITANCE VS. GATE-SOURCE VOLTAGE