IVN6657, IVN6658
n-Channel Enhancement-mode VMOS Power FETs

REPLACEMENTS FOR 2N6657,2N6658

FEATURES

- **High speed, high current switching**
- **Current sharing capability when paralleled**
- **Directly interface to CMOS, DTL, TTL logic**
- **simple DC biasing**
- **Extended safe operating area**
- **Inherently temperature stable**

APPLICATIONS

- **Switching power supplies**
- **DC to DC inverters**
- **CMOS and TTL to high current interface**
- **Line drivers**
- **Logic buffers**
- **Pulse amplifiers**

ABSOLUTE MAXIMUM RATINGS

(25°C unless otherwise noted)

Drain-source Voltage
- IVN6657 ..... 60V
- IVN6658 ..... 90V

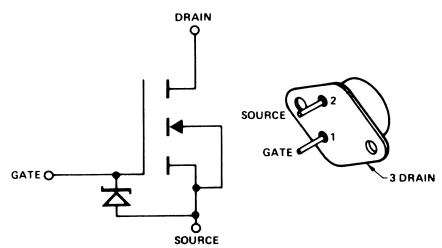
Drain-gate Voltage
- IVN6657 ..... 60V
- IVN6658 ..... 90V

Continuous Drain Current (see note 1) 2.4A
Peak Drain Current (see note 2) 3.0A
Continuous Forward Gate Current 2.0mA
Peak-gate Forward Current 100mA
Peak-gate Reverse Current 100mA
Gate-source Forward (Zener) Voltage ..... +15V
Gate-source Reverse (Zener) Voltage ..... –0.3V
Thermal Resistance, Junction to Case ..... 5.0°C/W
Continuous Device Dissipation at (or below)
25°C Case Temperature 25W
Linear Derating Factor ..... 200mW/°C
Operating Junction
Temperature Range ..... –55 to +150°C
Storage Temperature Range ..... –55 to +150°C
Lead Temperature
(1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $R_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

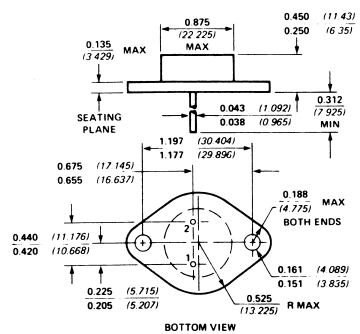
SCHEMATIC DIAGRAM



Body internally connected to source.
Drain common to case.

PACKAGE DIMENSIONS

PKG: JEDEC TO-3



Dimensions shown in inches and *(mm)*.

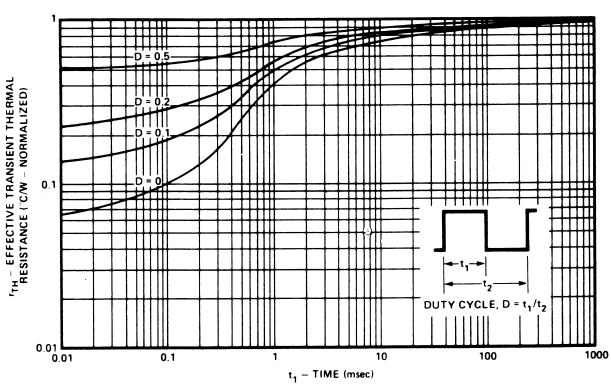
IVN6657, IVN6658

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

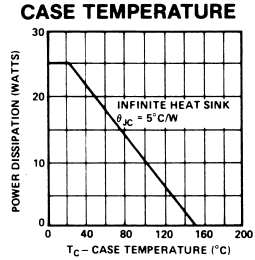
		CHARACTERISTIC		IVN6657			IVN6658			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DSS}	Drain Source Breakdown	60			90			V	V_{GS} = 0, I_D = 10μA	
2				80			90				V_{GS} = 0, I_D = 2.5mA	
3		$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	0.8		2.0		V_{DS} = V_{GS}, I_D = 1mA	
4		I_{GSS}	Gate-Body Leakage		0.5	100		0.5	100	nA	V_{GS} = 15V, V_{DS} = 0	
5						500			500		V_{GS} = 15V, V_{DS} = 0, T_A = 125°C (Note 2)	
6		I_{DSS}	Zero Gate Voltage Drain Current			10			10	μA	V_{DS} = Max. Rating, V_{GS} = 0	
7						500			500		V_{DS} = 0.80 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)	
8					100			100		nA	V_{DS} = 25V, V_{GS} = 0	
9		$I_{D\,on}$	ON-State Drain Current	1.0	2		1.0	2		A	V_{DS} = 25V, V_{GS} = 10V	
10		$V_{DS\,on}$	Drain-Source Saturation Voltage		0.3			0.4		V	V_{GS} = 5V, I_D = 0.1 Amp	
11					1.0	1.5		1.1	1.6		V_{GS} = 5V, I_D = 0.3 Amp	
12					0.9			1.3			V_{GS} = 10V, I_D = 0.5 Amp	
13					2.2	3.0		2.2	4.0		V_{GS} = 10V, I_D = 1.0 Amp	(Note 1)
14		$r_{DS\,on}$	Static Drain-Source ON-State Resistance		2.2	3.0		2.2	4.0	Ω	V_{GS} = 10V, I_D = 1.0 Amp	
15		$r_{ds\,on}$	Small-Signal Drain-Source ON-State Resistance		2.2	3.0		2.2	4.0		V_{GS} = 10V, I_D = 1.0, f = 1kHz	
16		g_{fs}	Forward Transconductance	170	250		170	250		mʊ	V_{DS} = 24V, I_D = 0.5 Amp	
17	DYNAMIC	C_{iss}	Input Capacitance			50			50	pF	V_{GS} = 0, V_{DS} = 24V, f = 1.0MHz	
18		C_{ds}	Drain-Source Capacitance			40			40			
19		C_{rss}	Reverse Transfer Capacitance			10			10		V_{GS} = 0, V_{DS} = 24V, f = 1.0MHz	
20						35			35		V_{GS} = 0, V_{DS} = 0, f = 1.0MHz	
21		$t_{d\,on}$	Turn-ON Delay Time		2	5		2	5	ns		(Note 2)
22		t_r	Rise Time		2	5		2	5			
23		$t_{d\,off}$	Turn-OFF Delay Time		2	5		2	5			
24		t_f	Fall Time		2	5		2	5			

Note 1. Pulse test — 80μsec pulse, 1% duty cycle.
Note 2. Sample test.

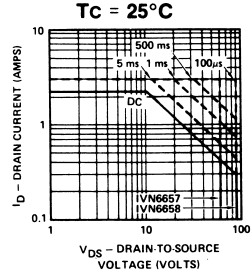
THERMAL RESPONSE



POWER DISSIPATION vs CASE TEMPERATURE



DC SAFE OPERATING REGION Tc = 25°C



IVN6660, IVN6661
n-Channel Enhancement-mode VMOS Power FETs

REPLACEMENTS FOR 2N6660, 2N6661

FEATURES

- **High speed, high current switching**
- **Current sharing capability when paralleled**
- **Directly interface to CMOS, DTL, TTL logic**
- **simple DC biasing**
- **Extended safe operating area**
- **Inherently temperature stable**

APPLICATIONS

- **Switching power supplies**
- **DC to DC inverters**
- **CMOS and TTL to high current interface**
- **Line drivers**
- **Logic buffers**
- **Pulse amplifiers**

ABSOLUTE MAXIMUM RATINGS

(25°C unless otherwise noted)

Drain-source Voltage
- IVN6660 ..... 60V
- IVN6661 ..... 90V

Drain-gate Voltage
- IVN6660 ..... 60V
- IVN6661 ..... 90V

Continuous Drain Current (see note 1) 1.2A
Peak Drain Current (see note 2) 3.0A
Continuous Forward Gate Current 2.0mA
Peak-gate Forward Current 100mA
Peak-gate Reverse Current 100mA
Gate-source Forward (Zener) Voltage ..... +15V
Gate-source Reverse (Zener) Voltage ..... –0.3V
Thermal Resistance, Junction to Case ..... 20°C/W
Continuous Device Dissipation at (or below)
- 25°C Case Temperature 6.25W

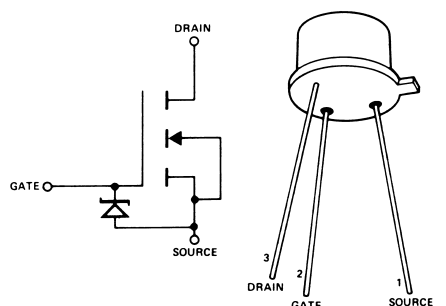
Linear Derating Factor ..... 50mW/°C
Operating Junction
- Temperature Range ..... –55 to +150°C

Storage Temperature Range ..... –55 to +150°C
Lead Temperature
- (1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $R_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

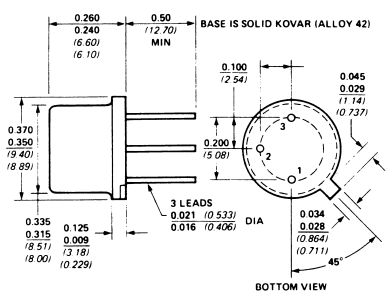
SCHEMATIC DIAGRAM



Body internally connected to source.
Drain common to case.

PACKAGE DIMENSIONS

PKG: JEDEC TO-39



Dimensions shown in inches and *(mm)*.

IVN6660, IVN6661

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		CHARACTERISTIC		IVN6660			IVN6661			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DSS}	Drain Source Breakdown	60			90			V	V_{GS} = 0, I_D = 10μA	
2				60			90				V_{GS} = 0, I_D = 2.5mA	
3		$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	0.8		2.0		V_{DS} = V_{GS}, I_D = 1mA	
4		I_{GSS}	Gate-Body Leakage		0.5	100		0.5	100	nA	V_{GS} = 15V, V_{DS} = 0	
5						500			500		V_{GS} = 15V, V_{DS} = 0, T_A = 125°C	(Note 2)
6		I_{DSS}	Zero Gate Voltage Drain Current			10			10	μA	V_{DS} = Max. Rating, V_{GS} = 0	
7						500			500		V_{DS} = 0.80 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)	
8					100			100		nA	V_{DS} = 25V, V_{GS} = 0	
9		$I_{D(on)}$	ON-State Drain Current	1.0	2		1.0	2		A	V_{DS} = 25V, V_{GS} = 10V	(Note 1)
10		$V_{DS(on)}$	Drain-Source Saturation Voltage		0.3			0.4		V	V_{GS} = 5V, I_D = 0.1 Amp	
11					1.0	1.5		1.1	1.6		V_{GS} = 5V, I_D = 0.3 Amp	
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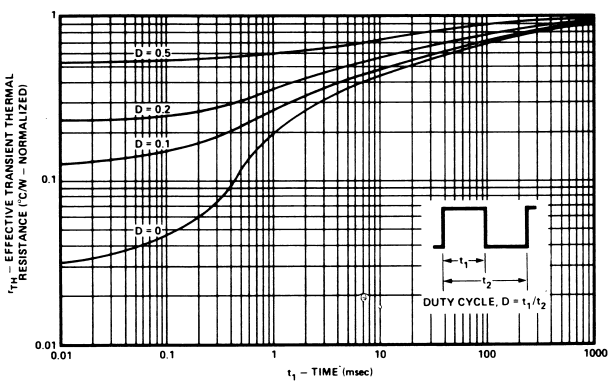
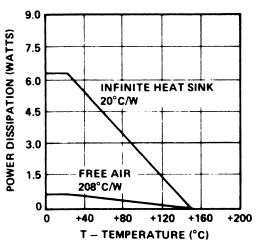
14		$r_{DS(on)}$	Static Drain-Source ON-State Resistance		2.2	3.0		2.2	4.0	Ω	V_{GS} = 10V, I_D = 1.0 Amp	
15	DYNAMIC	$r_{ds(on)}$	Small-Signal Drain-Source ON-State Resistance		2.2	3.0		2.2	4.0		V_{GS} = 10V, I_D = 1.0, f = 1kHz	
16		g_{fs}	Forward Transconductance	170	250		170	250		m℧	V_{DS} = 24V, I_D = 0.5 Amp	
17		C_{iss}	Input Capacitance			50			50	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0MHz	(Note 2)
18		C_{ds}	Drain-Source Capacitance			40			40			
19		C_{rss}	Reverse Transfer Capacitance			10			10		V_{GS} = 0, V_{DS} = 24V, f = 1.0MHz	
20						35			35		V_{GS} = 0, V_{DS} = 0, f = 1.0MHz	
21		$t_{d(on)}$	Turn-ON Delay Time		2	5		2	5	ns		
22		t_r	Rise Time		2	5		2	5			
23		$t_{d(off)}$	Turn-OFF Delay Time		2	5		2	5			
24		t_f	Fall Time		2	5		2	5			

Note 1. Pulse test — 80μsec pulse, 1% duty cycle. **Note 2.** Sample test.

THERMAL RESPONSE



POWER DISSIPATION vs CASE OR AMBIENT TEMPERATURE



DC SAFE OPERATING REGION
Tc = 25°C