ML101A & B MOS TRANSISTOR

ML102A & B MATCHED PAIR OF MOS TRANSISTORS

The ML101 is a single p-channel enhancement mode MOS transistor, incorporating a gate protection diode to obviate the need for special care in handling. It lacks, therefore, the extremely high input impedance of devices without this protection, such as the MT101.

The ML101A and B are both available in TO-18.

The ML102 is a matched pair of devices, similar to the ML101. The ML102A and B are both available in TO-5

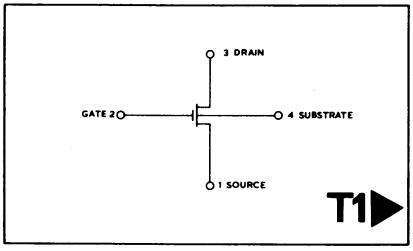


Fig. 1 ML101 circuit diagram

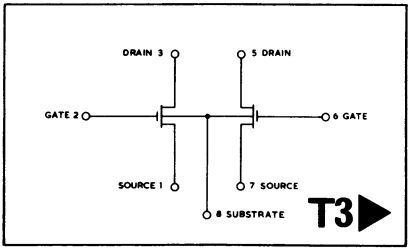


Fig. 2 ML102 circuit diagram

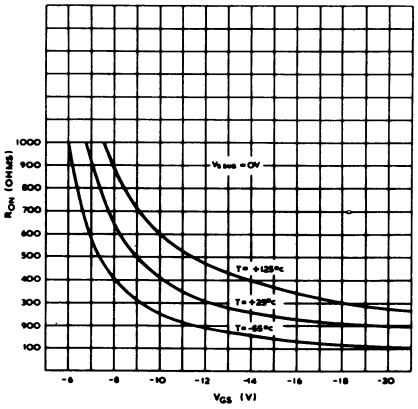


Fig. 3 Drain-source ON resistance v. gate-source voltage (typical)

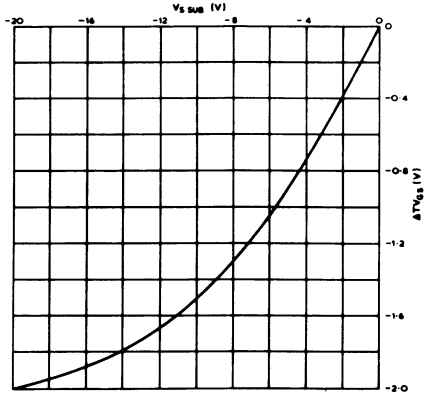


Fig. 4 Change of threshold voltage (ΔV_{GS}) v. source-substrate bias voltage (typical)

ELECTRICAL CHARACTERISTICS

Test conditions: Temperature = +22°C ±2°C

Characteristic	Symbol	Circuit	Value			Units	Test conditions
			Min.	Typ.	Max.		
*Gate threshold voltage	TV_{GS}	All types	3·8	5·1	6·5	V(neg.)	$V_{GS}=V_{DS}$ $I_D=10\mu A$
Drain-source ON resistance (−10V)	R_{ON}	All types		470	850	Ω	$V_{DS} \leqslant 100mV$ $V_{SSUB}=0V$ $V_{GS}=-10V$
Drain-source (−20V) ON resistance	R_{ON}	All types		200	350	Ω	$V_{DS} \leqslant 100mV$ $V_{SSUB}=0V$ $V_{GS}=-20V$
R_{ON} matching (Difference in R_{ON} between any two devices in same package)	ΔR_{ON}	All types		15	40	Ω	$V_{DS} \leqslant 100mV$ $V_{GS}=-20V$ $V_{SSUB}=0V$
Gate-source capacitance	C_{gs}	All types		3·5	5·3	pF	$V_{DS}=V_{GS}$ $I_D=1mA$ f=1MHz
Gate-drain capacitance	C_{gd}	All types		2·0		pF	$V_{DS}=V_{GS}$ $I_D=1mA$ f=1MHz
Drain-source capacitance	C_{ds}	All types		1·7		pF	$V_{DS}=V_{GS}=0V$
Drain-substrate capacitance	C_{dsub}	All types		4·0	6·0	pF	$V_{DSUB}=0V$ f=1MHz
Source-substrate capacitance	C_{ssub}	All types		5·1	7·7	pF	$V_{SSUB}=0$ f=1MHz
Drain-source leakage	I_{DS}	A types B types		0·2 1·0	0·5 20	nA nA	$V_{GS}=0V$ $V_{DS}=-20V$
Source-substrate leakage	I_{SSUB}	A types B types		0·3 2	2 20	nA nA	$V_{SSUB}=-20V$ $V_{GS}=0V$
Drain-substrate leakage	I_{DSUB}	A types B types		0·2 2	0·5 20	nA nA	$V_{DSUB}=-20V$ $V_{GS}=0V$
Gate-channel leakage (see operating notes)	I_{GCH}	A types B types			1 20	nA nA	$V_{GSUB}=-20V$ $V_{DSUB}=V_{SSUB}=0V$

*To avoid confusion, maximum and minimum values of negative quantities are taken as referring to the magnitude of a parameter and sign indicated in the units column.

OPERATING NOTES

The identification of the source and drain of this type of MOS transistor is purely arbitrary because of the symmetrical nature of its construction.

Gate-channel 'leakage' is a consequence of the gate protection device. When the device is turned on by negative gate voltage a current is also induced in a spurious MOST between the gate protection diode and the source-drain channel. Operation at lower gate voltages reduces the effect.

Cascaded amplifier stages using these MOS transistors may be directly coupled.

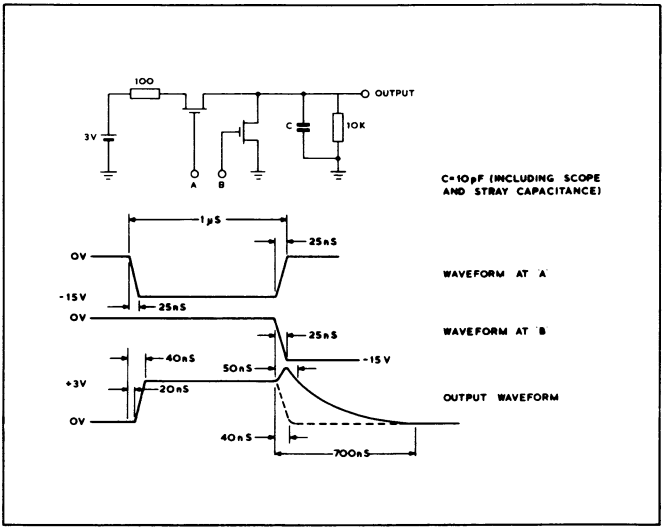


Fig. 5 Switching circuit typical waveforms

ABSOLUTE MAXIMUM RATINGS

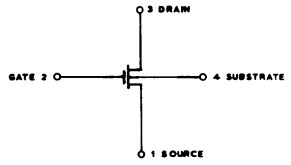
The absolute maximum ratings are limiting absolute values above which operating life may be shortened or satisfactory performance may be impaired.

Storage temperature	−55°C to +125°C
Chip temperature	+125°C
Chip-to-ambient thermal resistance	
ML101	486°C/W
ML102	250°C/W
Chip-to-case thermal resistance	
ML101	146°C/W
ML102	80°C/W
Gate breakdown voltage (10μA)	-40V
Gate- substrate positive voltage	0.3V
Drain-source breakdown voltage (10μA)	±40V
Drain (or source) -substrate breakdown voltage (10μA)	-40V
Drain (or source) -substrate positive voltage	0.3V
Drain current	20mA

ML111B STANDARD MOST

The ML111B (STANDARD MOST) is a small p-channel enhancement mode MOS transistor, suitable for use in a wide range of analogue switching applications. The device includes a gate protection diode to obviate the need for special care in handling.

The STANDARD MOST is incorporated on all Plessey MOSAIC devices for Q.A. purposes. It provides the basic characterization data for MOS process and all devices are subjected to burn-in for 100 hours at 125°C. As a result, the ML111B is a highly reliable MOS transistor with well-defined electrical characteristics.



The identification of the source and drain of this type of MOS transistor is purely arbitrary because of the symmetrical nature of its construction.

Fig. 1 ML111B Standard MOST

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting absolute values above which operating life may be shortened or satisfactory performance may be impaired.

Storage Temperature	−55°C to +125°C
Chip Temperature	+125°C
Chip-to-ambient thermal resistance	250°C/W
Chip-to-case thermal resistance	80°C/W
Input gate voltage, V_{GSUB}	−40V to 0V
Drain-source voltage, V_{DS}	−40V to +40V
Drain-substrate voltage, V_{DSUB}	−40V to 0V
Source-substrate voltage, V_{SSUB}	−40V to 0V

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ELECTRICAL CHARACTERISTICS (at 20°C)

Characteristic	Value			*Units	Test Conditions
	Min.	Typ.	Max.		
Gate Threshold Voltage	4		6.5	V(neg.)	V_{GS} =V_{DS} I_D =1.25μA
Drain-Source ON Resistance (−20V)	1	1.6	2.2	kΩ	V_{GS} =−20V I_D =−1.25μA V_{SSUB} =0V
Drain-Source ON Resistance (−10V)		3.2	6.4	kΩ	V_{GS} =−10V I_D =−1.25μA V_{SSUB} =0V
Gate-Source Capacitance		1	3	pF	V_{DS} =V_{GS} I_D =−1mA f =1MHz
Gate-Drain Capacitance		1	3	pF	V_{DS} =V_{GS} I_D =1mA f =1MHz
Drain-Source Capacitance		1	3	pF	V_{DS} =V_{GS}=0V f =1MHz
Drain-Substrate Capacitance Source-Substrate Capacitance		1.5	4	pF	V_{DSUB} =0 V_{SSUB} =0
Drain-Source Leakage		0.03	2·5	nA	V_{DS} =−20V V_{GS} =0V
Source-Substrate Leakage		0.08	2.5	nA	V_{SSUB} =−20V V_{GS} =0V
Drain-Substrate Leakage		0.08	2.5	nA	V_{DSUB} =−20V V_{GS} =0V
Gate-Channel Leakage		0.1	1	nA	V_{GSUB} =−20V V_{DSUB} =V_{SSUB}=0V

*To avoid confusion, maximum and minimum values of negative quantities are taken as referring to the magnitude of a parameter and sign indicated in the units column.

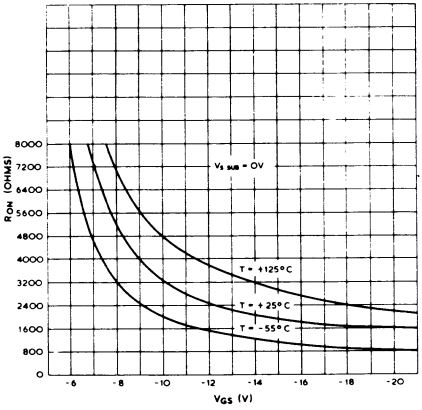

Fig. 2 Drain-source ON resistance versus gate-source voltage (typical)

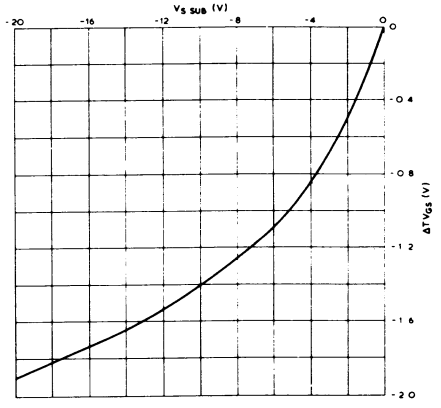

Fig. 3 Change of threshold voltage ΔTV_{GS} versus source-substrate bias voltage (typical)