MRF134

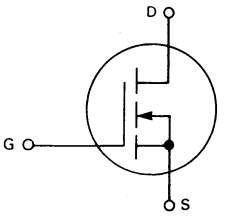
The RF TMOS Line

N-CHANNEL ENHANCEMENT-MODE
TMOS RF POWER FIELD-EFFECT TRANSISTOR

. . . designed for wideband large-signal amplifier and oscillator applications in the 2.0 to 400 MHz range.

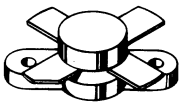
- Guaranteed 28 Volt, 150 MHz Performance
  - Output Power = 5.0 Watts
  - Minimum Gain = 11 dB
  - Efficiency — 55% (Typical)
- Small-Signal and Large-Signal Characterization
- Typical Performance at 400 MHz, 28 Vdc, 5.0 W
  - Output = 10.6 dB Gain
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Low Noise Figure — 2.0 dB (Typ) at 200 mA, 150 MHz
- Excellent Thermal Stability, Ideally Suited For Class A Operation

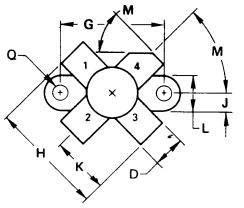
TMOS™

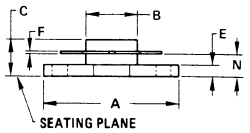


5.0 W 2.0-400 MHz

N-CHANNEL TMOS
BROADBAND RF POWER
FET







STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.29	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

CASE 211-07

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain — Source Voltage	V_{DSS}	65	Vdc
Drain — Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate — Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	0.9	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	17.5 0.10	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

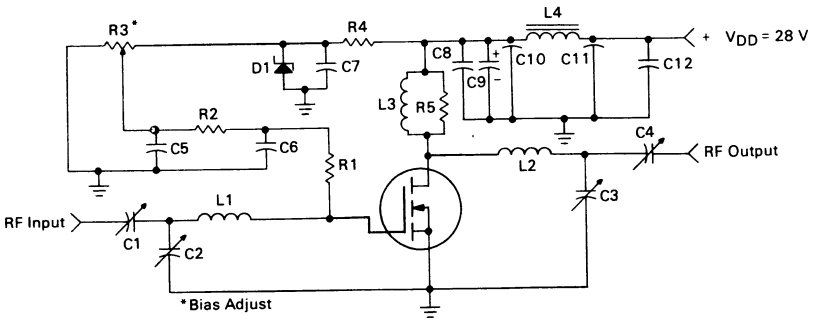
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	1.0	mAdc
Gate-Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (I_D = 10 mA, V_{DS} = 10 V)	$V_{GS(th)}$	1.0	3.5	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 100 mA)	g_{fs}	80	110	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	7.0	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	9.7	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	2.3	—	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure (V_{DS} = 28 Vdc, I_D = 200 mA, f = 150 MHz)	NF	—	2.0	—	dB
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 5.0 W, I_{DQ} = 50 mA) f = 150 MHz (Fig. 1) f = 400 MHz (Fig. 14)	G_{ps}	11 —	14 10.6	— —	dB
Drain Efficiency (Fig. 1) (V_{DD} = 28 Vdc, P_{out} = 5.0 W, f = 150 MHz, I_{DQ} = 50 mA)	η	50	55	—	%
Electrical Ruggedness (Fig. 1) (V_{DD} = 28 Vdc, P_{out} = 5.0 W, f = 150 MHz, I_{DQ} = 50 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			

FIGURE 1 — 150 MHz TEST CIRCUIT



C1, C4 — Arco 406, 15–115 pF
C2 — Arco 403, 3–35 pF
C3 — Arco 402, 1.5–20 pF
C5, C6, C7, C8, C12 — 0.1 μF Erie Redcap
C9 — 10 μF, 50 V
C10, C11 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener
L1 — 3 Turns, 0.310" ID, #18 AWG Enamel, 0.2" Long
L2 — 3-1/2 Turns, 0.310" ID, #18 AWG Enamel, 0.25" Long
L3 — 20 Turns, #20 AWG Enamel Wound on R5
L4 — Ferroxcube VK-200 — 19/4B
R1 — 68 Ω, 1.0 W Thin Film
R2 — 10 kΩ, 1/4 W
R3 — 10 Turns, 10 kΩ Beckman Instruments 8108
R4 — 1.8 kΩ, 1/2 W
R5 — 1.0 MΩ, 2.0 W Carbon
Board — G10, 62 mils

FIGURE 2 — OUTPUT POWER versus INPUT POWER

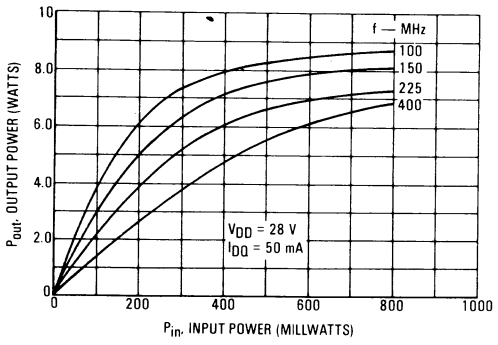


FIGURE 3 — OUTPUT POWER versus INPUT POWER

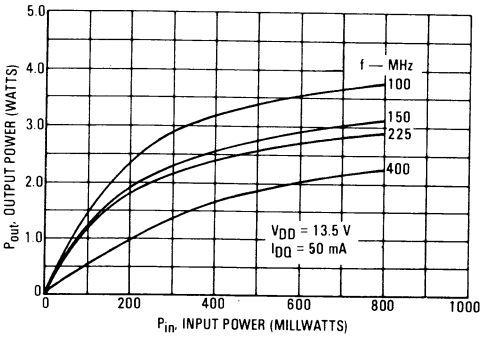


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 100 MHz

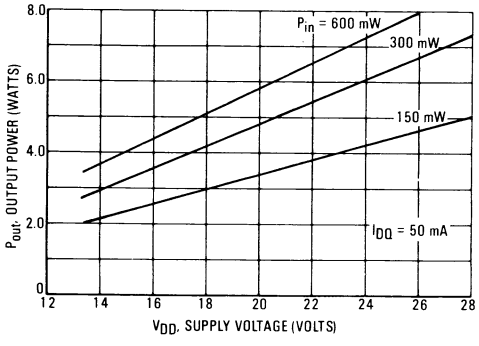


FIGURE 5 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 150 MHz

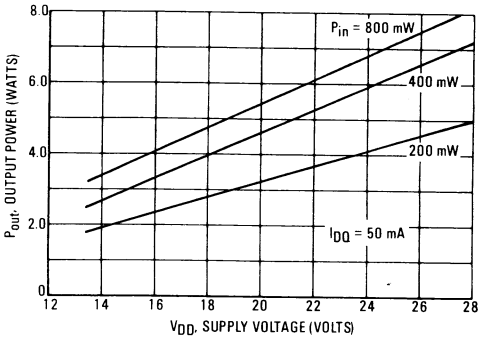


FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 225 MHz

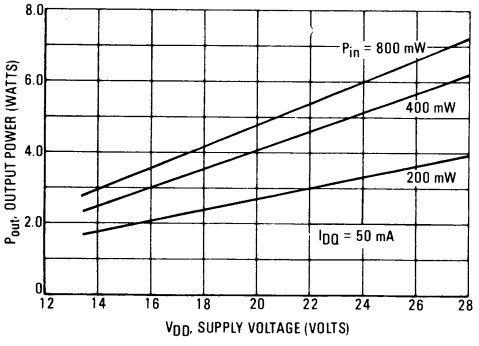


FIGURE 7 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 400 MHz

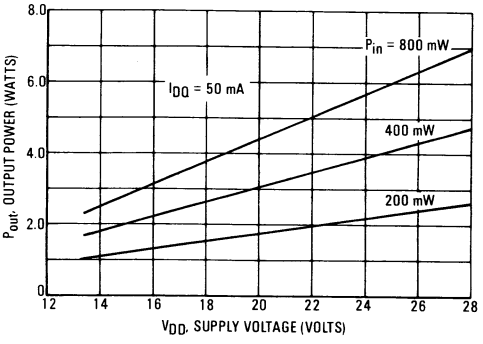


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FIGURE 8 — OUTPUT POWER versus GATE VOLTAGE

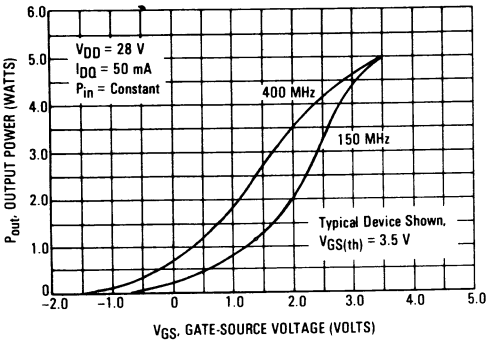


FIGURE 9 — DRAIN CURRENT versus GATE VOLTAGE (TRANSFER CHARACTERISTICS)

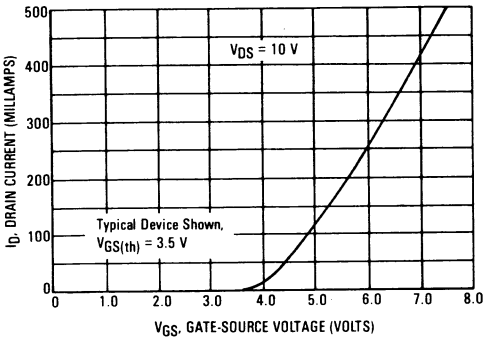


FIGURE 10 — GATE-SOURCE VOLTAGE versus CASE TEMPERATURE

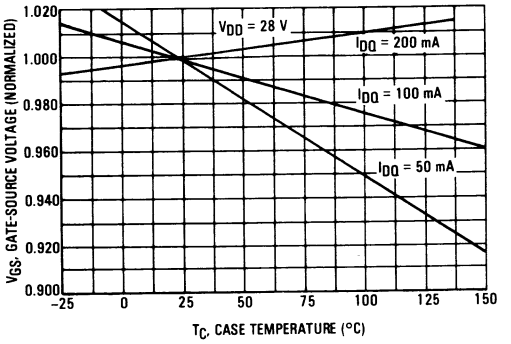


FIGURE 11 — MAXIMUM AVAILABLE GAIN versus FREQUENCY

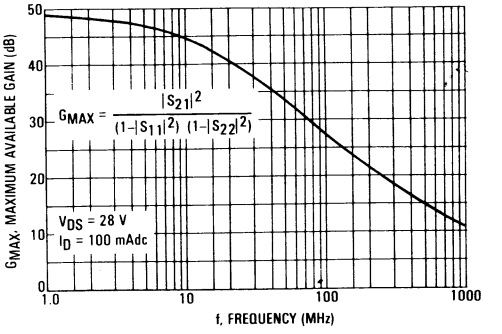


FIGURE 12 — CAPACITANCE versus VOLTAGE

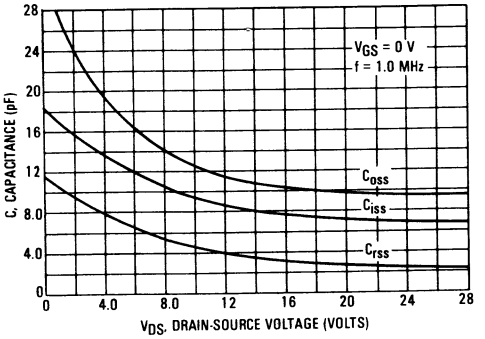


FIGURE 13 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

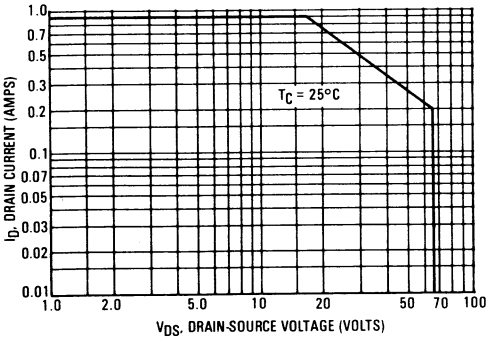
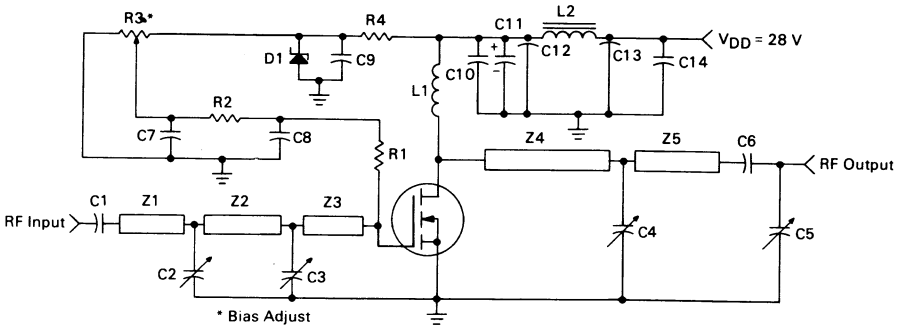


FIGURE 14 — 400 MHz TEST CIRCUIT



C1, C6 — 270 pF, ATC 100 mils
C2, C3, C4, C5 — 0-20 pF Johanson
C7, C9, C10, C14 — 0.1 μF Erie Redcap, 50 V
C8 — 0.001 μF
C11 — 10 μF, 50 V
C12, C13 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener
L1 — 6 Turns, 1/4" ID, #20 AWG Enamel
L2 — Ferroxcube VK-200 — 19/4B
R1 — 68 Ω, 1.0 W Thin Film
R2 — 10 kΩ, 1/4 W
R3 — 10 Turns, 10 kΩ Beckman Instruments 8108
R4 — 1.8 kΩ, 1/2 W
Z1 — 1.4" × 0.166" Microstrip
Z2 — 1.1" × 0.166" Microstrip
Z3 — 0.95" × 0.166" Microstrip
Z4 — 2.2" × 0.166" Microstrip
Z5 — 0.85" × 0.166" Microstrip
Board — Glass Teflon, 62 mils

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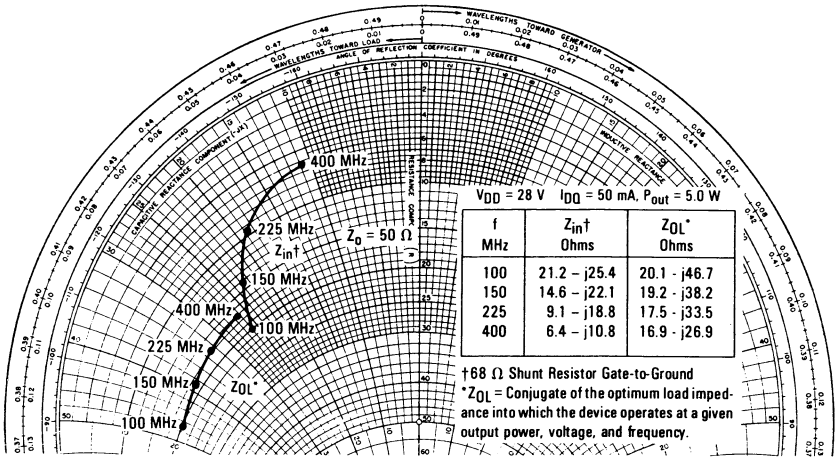
FIGURE 15 — LARGE-SIGNAL SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCES, Z_{in}†, Z_{OL}*



V_{DD} = 28 V I_{DQ} = 50 mA, P_{out} = 5.0 W

f MHz	Z_{in}† Ohms	Z_{OL}* Ohms
100	21.2 – j25.4	20.1 - j46.7
150	14.6 – j22.1	19.2 - j38.2
225	9.1 – j18.8	17.5 - j33.5
400	6.4 – j10.8	16.9 - j26.9

†68 Ω Shunt Resistor Gate-to-Ground
*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

FIGURE 16 — COMMON SOURCE SCATTERING PARAMETERS
V_{DS} = 28 V, I_D = 100 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
1.0	0.989	-1.0	11.27	179	0.0014	89	0.954	-1.0
2.0	0.989	-2.0	11.27	179	0.0028	89	0.954	-2.0
5.0	0.988	-5.0	11.26	176	0.0069	86	0.954	-4.0
10	0.985	-10	11.20	173	0.014	83	0.951	-9.0
20	0.977	-20	10.99	166	0.027	76	0.938	-18
30	0.965	-30	10.66	159	0.039	69	0.918	-26
40	0.950	-39	10.25	153	0.051	63	0.895	-34
50	0.931	-47	9.777	147	0.060	57	0.867	-42
60	0.912	-53	9.359	142	0.069	53	0.846	-49
70	0.892	-58	8.960	138	0.077	49	0.828	-56
80	0.874	-62	8.583	135	0.085	46	0.815	-62
90	0.855	-66	8.190	131	0.091	43	0.801	-68
100	0.833	-70	7.808	128	0.096	40	0.785	-74
110	0.827	-73	7.661	125	0.101	38	0.784	-77
120	0.821	-76	7.515	122	0.107	36	0.784	-82
130	0.814	-79	7.368	119	0.113	34	0.784	-85
140	0.808	-82	7.222	116	0.119	32	0.783	-88
150	0.802	-86	7.075	114	0.125	31	0.783	-90
160	0.788	-89	6.810	112	0.127	30	0.780	-92
170	0.774	-92	6.540	110	0.128	28	0.774	-94
180	0.763	-94	6.220	108	0.130	26	0.762	-98
190	0.751	-97	5.903	106	0.132	24	0.760	-100
200	0.740	-100	5.784	104	0.134	23	0.758	-103
225	0.719	-104	5.334	100	0.136	20	0.757	-107
250	0.704	-108	4.904	97	0.139	19	0.758	-110
275	0.687	-113	4.551	92	0.141	16	0.757	-114
300	0.673	-117	4.219	89	0.141	14	0.750	-117
325	0.668	-120	3.978	86	0.142	12	0.757	-120
350	0.669	-123	3.737	83	0.142	10	0.766	-121
375	0.662	-125	3.519	80	0.143	9.0	0.768	-123
400	0.654	-127	3.325	77	0.142	8.0	0.772	-124
425	0.650	-129	3.170	75	0.140	7.0	0.772	-125
450	0.638	-131	3.048	72	0.141	6.0	0.783	-125
475	0.614	-132	2.898	71	0.136	6.0	0.786	-126
500	0.641	-133	2.833	68	0.136	5.0	0.795	-127
525	0.638	-135	2.709	66	0.135	5.0	0.801	-127
550	0.633	-137	2.574	64	0.133	4.0	0.802	-128
575	0.628	-138	2.481	62	0.131	5.0	0.805	-128
600	0.625	-140	2.408	60	0.129	5.0	0.814	-128
625	0.619	-142	2.334	58	0.128	5.0	0.818	-129
650	0.617	-144	2.259	56	0.125	6.0	0.824	-130
675	0.618	-146	2.192	55	0.123	7.0	0.834	-130
700	0.619	-147	2.124	53	0.122	8.0	0.851	-131
725	0.618	-150	2.061	51	0.120	9.0	0.859	-132
750	0.614	-152	1.983	49	0.118	11	0.857	-133
775	0.609	-154	1.908	48	0.119	13	0.865	-133
800	0.562	-155	1.877	49	0.118	15	0.872	-133
825	0.587	-156	1.869	46	0.119	16	0.869	-134
850	0.593	-158	1.794	44	0.118	18	0.875	-135
875	0.597	-160	1.749	43	0.119	18	0.881	-135
900	0.598	-162	1.700	41	0.118	18	0.889	-136
925	0.592	-164	1.641	40	0.115	18	0.888	-138
950	0.588	-166	1.590	39	0.112	20	0.877	-138
975	0.586	-168	1.572	39	0.108	23	0.864	-137
1000	0.590	-171	1.551	37	0.107	28	0.863	-137

The Power RF characterization data were measured with a 68 ohm resistor shunting the MRF134 input port. The scattering parameters were measured on the MRF134 device alone with no external components.

FIGURE 17 — S_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 100 mA

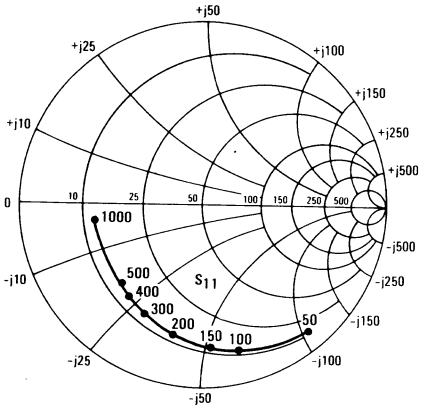


FIGURE 18 — S_{12}, REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 100 mA

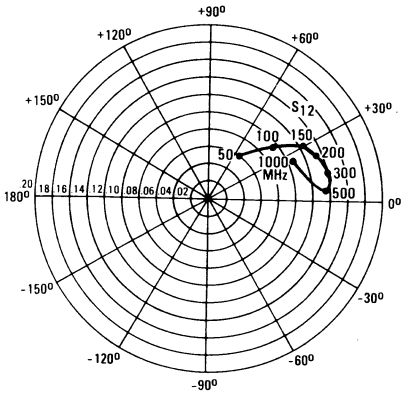


FIGURE 19 — S_{21}, FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 100 mA

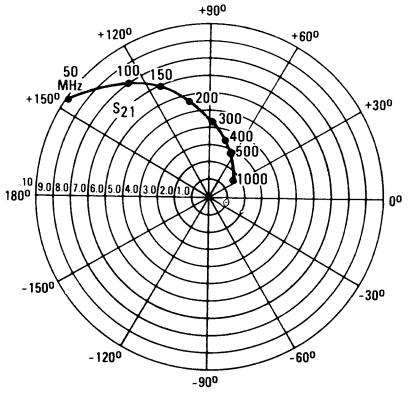
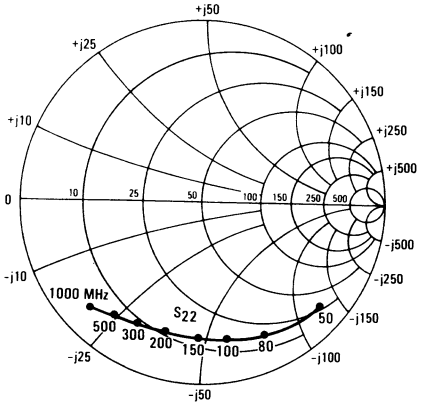


FIGURE 20 — S_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 100 mA



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DESIGN CONSIDERATIONS

The MRF134 is a TMOS RF power N-Channel enhancement mode field-effect transistor (FET) designed especially for VHF power amplifier and oscillator applications. Motorola TMOS FETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V-groove vertical power FETs.

Motorola Application Note AN-211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of TMOS RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF134 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF134 was characterized at I_{DQ} = 50 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF134 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC, and modulation systems. (See Figure 8.)

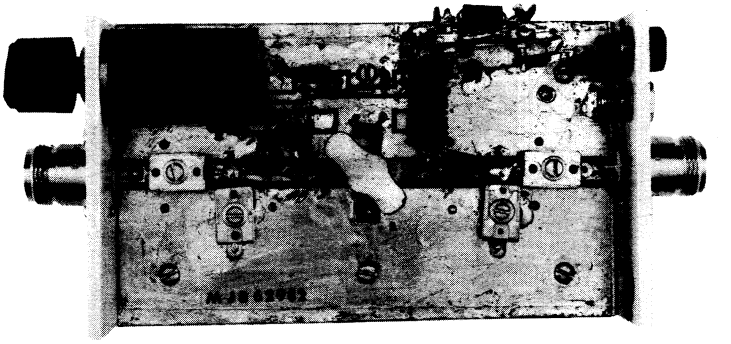
AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar VHF transistors are suitable for MRF134. See Motorola Application Note AN-721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of TMOS FETs helps ease the task of broadband network design. Both small signal scattering parameters and large signal impedances are provided. While the s-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of TMOS power FETs.

RF power FETs are triode devices and, therefore, not unilateral. This, coupled with the very high gain of the MRF134, yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The MRF134 was characterized with a 68-ohm input shunt loading resistor. Two port parameter stability analysis with the MRF134 s-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN-215A for a discussion of two port network theory and stability.

Input resistive loading is not feasible in low noise applications. The MRF134 noise figure data was generated in a circuit with drain loading and a low loss input network.

FIGURE 21 — 150 MHz TEST CIRCUIT



MRF136
MRF136Y

15 W, 30 W 2–400 MHz
N-CHANNEL
TMOS BROADBAND
RF POWER FETs

The RF TMOS Line

RF Power Field-Effect Transistors

N-Channel Enhancement Mode TMOS

. . . designed for wideband large-signal amplifier and oscillator applications in the 2 to 400 MHz range, in either single ended or push-pull configuration.

- Guaranteed 28 Volt, 150 MHz Performance

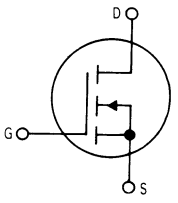
MRF136
Output Power = 15 Watts
Narrowband Gain = 16 dB (Typ)
Efficiency = 60% (Typical)

MRF136Y
Output Power = 30 Watts
Broadband Gain = 14 dB (Typ)
Efficiency = 54% (Typical)

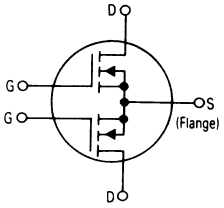
- Small-Signal and Large-Signal Characterization
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Space Saving Package For Push-Pull Circuit Applications — MRF136Y
- Excellent Thermal Stability, Ideally Suited For Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques

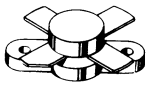
TMOS™

MRF136

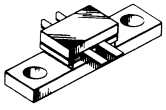


MRF136Y





MRF136
CASE 211-07



MRF136Y
CASE 319B-01

3

MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		MRF136	MRF136Y	
Drain-Source Voltage	V_{DSS}	65	65	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	65	65	Vdc
Gate-Source Voltage	V_{GS}	±40		Vdc
Drain-Current — Continuous	I_D	2.5	5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	55 0.314	100 0.571	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150		°C
Operating Junction Temperature	T_J	200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
		MRF136	MRF136Y	
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.2	1.75	°C/W

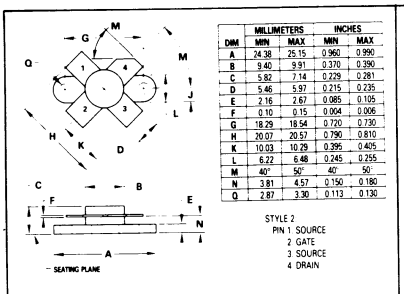
Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (NOTE 1)						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5 mA)		$V_{(BR)DSS}$	65	—	—	Vdc
Zero-Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)		I_{DSS}	—	—	2	mAdc
Gate-Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0)		I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS (NOTE 1)						
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 25 mA)		$V_{GS(th)}$	1	3	6	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 250 mA)		g_{fs}	250	400	—	mmhos
DYNAMIC CHARACTERISTICS (NOTE 1)						
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)		C_{iss}	—	24	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)		C_{oss}	—	27	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)		C_{rss}	—	5.5	—	pF
FUNCTIONAL CHARACTERISTICS (NOTE 2)						
Noise Figure (V_{DS} = 28 Vdc, I_D = 500 mA, f = 150 MHz)	MRF136	NF	—	1	—	dB
Common Source Power Gain (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 15 W, f = 150 MHz, I_{DQ} = 25 mA)	MRF136	G_{ps}	13	16	—	dB
Common Source Power Gain (Figure 2) (V_{DD} = 28 Vdc, P_{out} = 30 W, f = 150 MHz, I_{DQ} = 100 mA)	MRF136Y	G_{ps}	12	14	—	dB
Drain Efficiency (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 15 W, f = 150 MHz, I_{DQ} = 25 mA)	MRF136	η	50	60	—	%
Drain Efficiency (Figure 2) (V_{DD} = 28 Vdc, P_{out} = 30 W, f = 150 MHz, I_{DQ} = 100 mA)	MRF136Y	η	50	54	—	%
Electrical Ruggedness (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 15 W, f = 150 MHz, I_{DQ} = 25 mA, VSWR 30:1 at all Phase Angles)	MRF136	ψ	No Degradation in Output Power			
Electrical Ruggedness (Figure 2) (V_{DD} = 28 Vdc, P_{out} = 30 W, f = 150 MHz, I_{DQ} = 100 mA, VSWR 30:1 at all Phase Angles)	MRF136Y	ψ	No Degradation in Output Power			

Notes: 1. For MRF136Y, each side measured separately.
2. For MRF136Y measured in push-pull configuration.

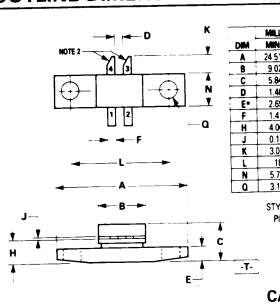
OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.29	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

STYLE 2
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

CASE 211-07

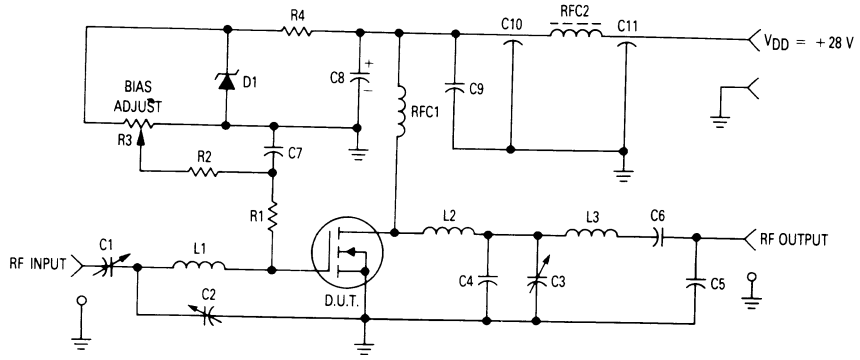


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.51	25.02	0.965	0.985
B	9.02	9.52	0.355	0.375
C	5.84	6.60	0.230	0.260
D	1.40	1.65	0.055	0.065
E*	2.69	2.94	0.106	0.116
F	1.4	1.65	0.055	0.065
H	4.06	4.31	0.160	0.170
J	0.10	0.15	0.004	0.006
K	3.05	3.55	0.120	0.140
L	18.42 BSC		0.725 BSC	
N	5.72	6.12	0.225	0.241
Q	3.18	3.42	0.125	0.135

STYLE 1:
PIN 1. GATE (INPUT)
2. GATE (INPUT)
3. DRAIN (OUTPUT)
4. DRAIN (OUTPUT)
SOURCE IS FLANGE

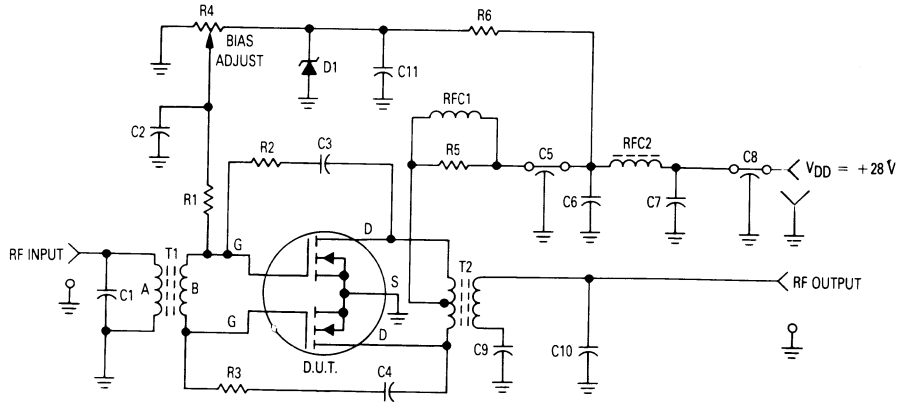
NOTES
1. POSITIONAL TOLERANCE FOR Q HOLES
⌖ ϕ0.15 (0.006 Ⓜ T A Ⓜ N Ⓜ
2. IDENTIFICATION NOTCH
1.0 mm (0.04) MINIMUM x 45°
3. DIMENSION D APPLIES 2 PLACES
DIMENSION K APPLIES 2 PLACES
DIMENSION Q APPLIES 2 PLACES
DIMENSION F APPLIES 4 PLACES
4. DIMENSIONS A AND N ARE DATUMS AND T IS A DATUM SURFACE
5. DIMENSION B APPLIES TO LEAD FRAME AND Bec
6. POSITIONAL TOLERANCE FOR F TERMINAL AND DIMENSION B
⌖ ϕ 38 (0.015) Ⓜ T A Ⓜ N Ⓜ
7. DIMENSIONING AND TOLERANCING PER Y14.5M 1982

CASE 319B-01



C1, C2 — Arco 406, 15–115 pF or Equivalent
C3 — Arco 404, 8–60 pF or Equivalent
C4 — 43 pF Mini-Unelco or Equivalent
C5 — 24 pF Mini-Unelco or Equivalent
C6 — 680 pF, 100 Mils Chip
C7 — 0.01 μF Ceramic
C8 — 100 μF, 40 V
C9 — 0.1 μF Ceramic
C10, C11 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener
L1 — 2 Turns, 0.29" ID, #18 AWG, 0.10" Long
L2 — 2 Turns, 0.23" ID, #18 AWG, 0.10" Long
L3 — 2-1/4 Turns, 0.29" ID, #18 AWG, 0.125" Long
RFC1 — 20 Turns, 0.30" ID, #20 AWG Enamel Closewound
RFC2 — Ferroxcube VK-200 — 19/4B
R1 — 27 Ω, 1 W Thin Film
R2 — 10 kΩ, 1/4 W
R3 — 10 Turns, 10 kΩ
R4 — 1.8 kΩ, 1/2 W
Board Material — 0.062" G10, 1 oz. Cu Clad, Double Sided

Figure 1. 150 MHz Test Circuit (MRF136)



C1 — 5 pF
C2, C3, C4, C6, C7, C9, C11 — 0.1 μF Ceramic
C5, C8 — 680 pF Feedthru
C10 — 15 pF
D1 — 1N4740 Motorola Zener
RFC1 — 17 Turns, #24 AWG Wound on R5
RFC2 — Ferroxcube VK-200-19/4B or Equivalent
R1 — 10 kΩ, 1/4 W
R2, R3 — 560 Ω, 1/2 W
R4 — 10 Turns, 10 kΩ
R5 — 56 kΩ, 1 W
R6 — 1.6 kΩ, 1/4 W
T1 — Primary Winding — 3 Turns #28 Enameled Wire.
— Secondary Winding — 2 Turns #28 Enameled Wire.
Both windings wound through a Fair/Rite Balun 65 core.
Part #2865002402.
T2 — 1:1 Transformer Wound Bifilar — 2 Turns Twisted Pair #24 Enameled Wire through a Indiana General Balun Q1 core. Part #18006-1-Q1. Primary winding center tapped.
Board Material — 0.062" G10, 1 oz. Cu Clad, Double Sided

Figure 2. 30–150 MHz Test Circuit (MRF136Y)

MRF136

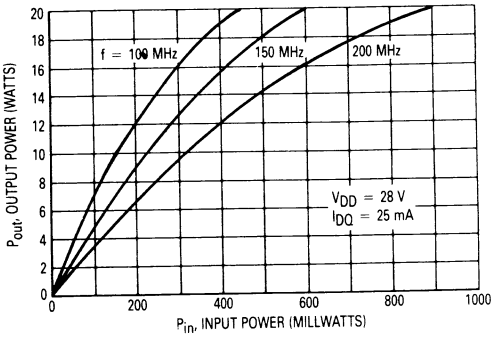


Figure 3. Output Power versus Input Power

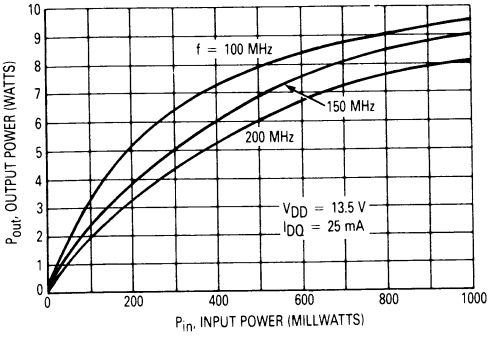


Figure 4. Output Power versus Input Power

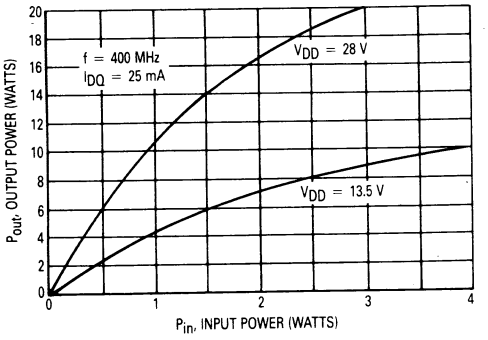


Figure 5. Output Power versus Input Power

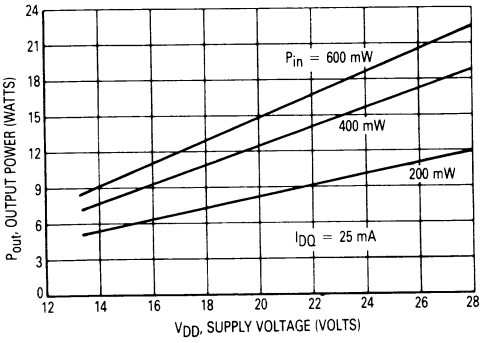


Figure 6. Output Power versus Supply Voltage
f = 100 MHz

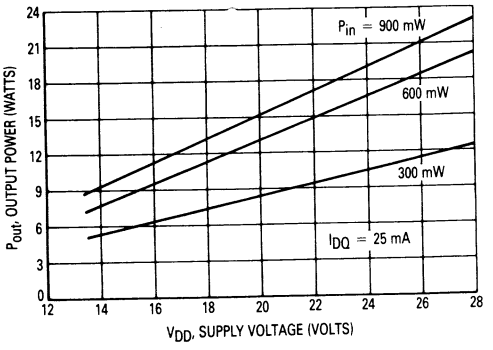


Figure 7. Output Power versus Supply Voltage
f = 150 MHz

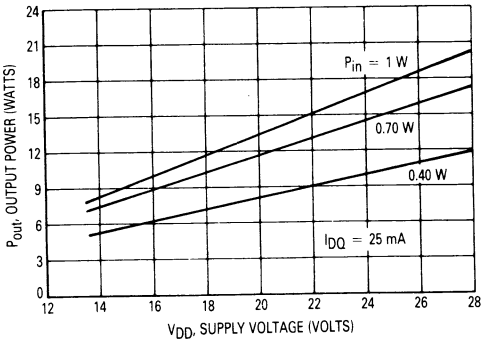


Figure 8. Output Power versus Supply Voltage
f = 200 MHz

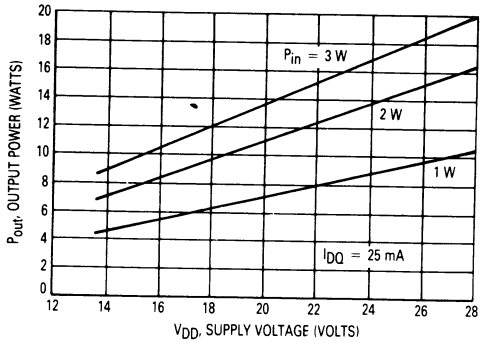


Figure 9. Output Power versus Supply Voltage
f = 400 MHz
MRF136

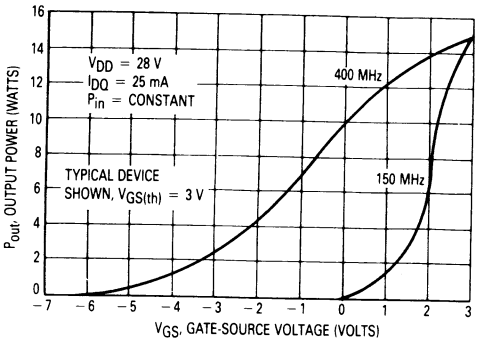


Figure 10. Output Power versus Gate Voltage
MRF136

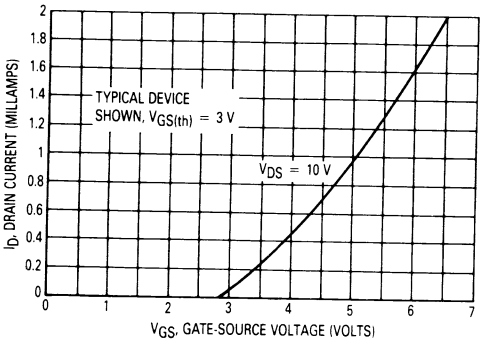


Figure 11. Drain Current versus Gate Voltage (Transfer Characteristics)*
MRF136/MRF136Y

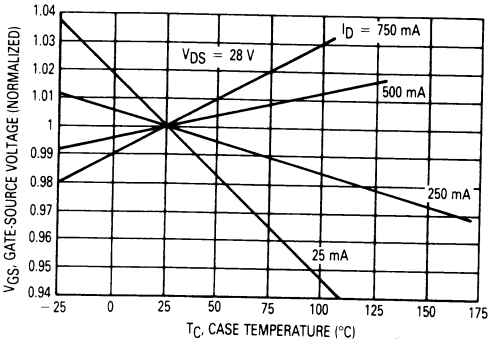


Figure 12. Gate-Source Voltage versus Case Temperature*
MRF136/MRF136Y

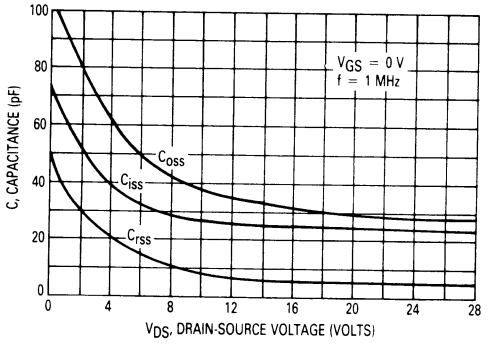


Figure 13. Capacitance versus Drain-Source Voltage*
MRF136/MRF136Y

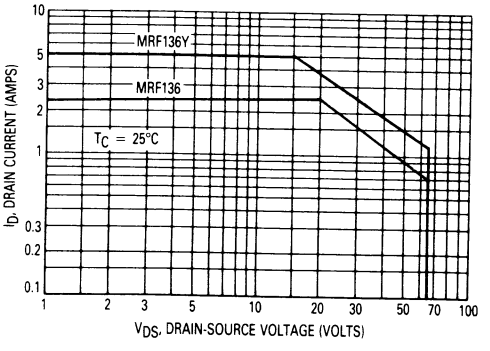


Figure 14. DC Safe Operating Area
MRF136/MRF136Y

*Data shown applies to MRF136 and each half of MRF136Y.

MRF136Y
TYPICAL PERFORMANCE IN BROADBAND TEST CIRCUIT
(Refer to Figure 2)

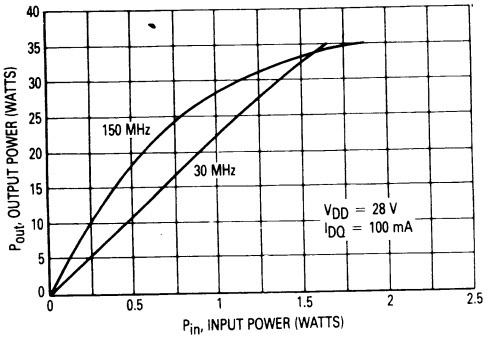


Figure 15. Output Power versus Input Power

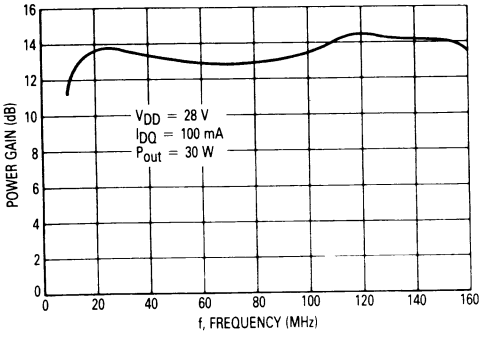


Figure 16. Power Gain versus Frequency

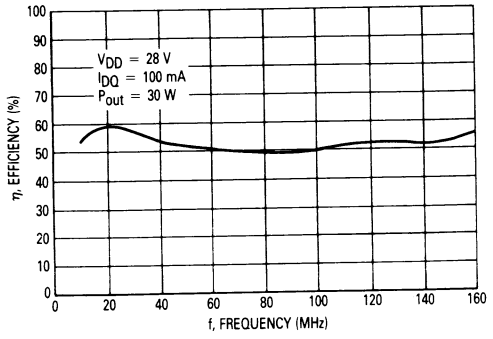


Figure 17. Drain Efficiency versus Frequency

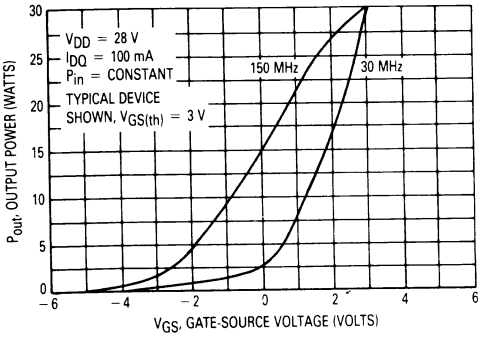


Figure 18. Output Power versus Gate Voltage

TYPICAL 400 MHz PERFORMANCE

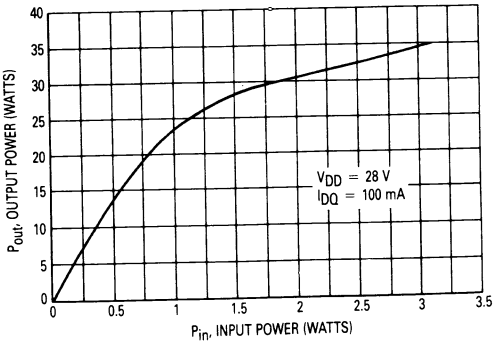


Figure 19. Output Power versus Input Power
f = 400 MHz

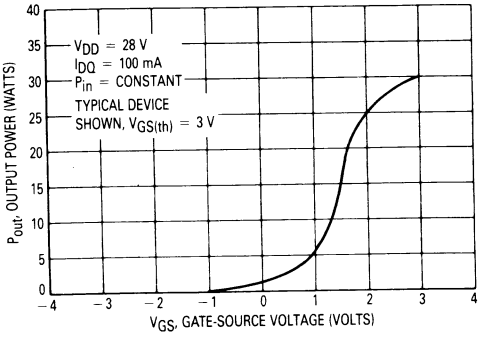


Figure 20. Output Power versus Gate Voltage
f = 400 MHz

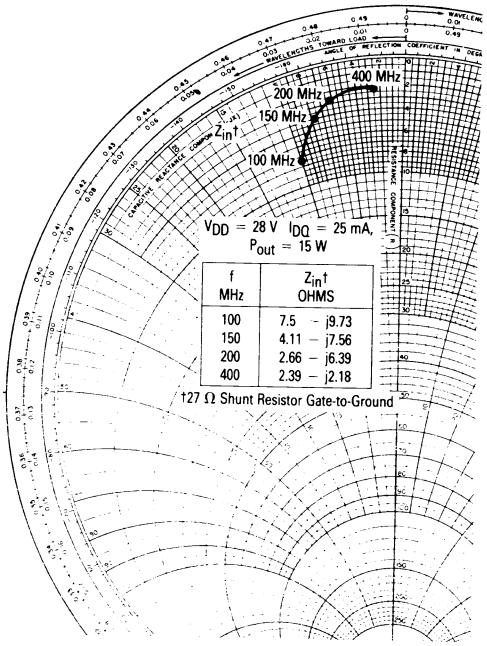


Figure 21. Large-Signal Series Equivalent Input Impedance, Z_{in}†
MRF136

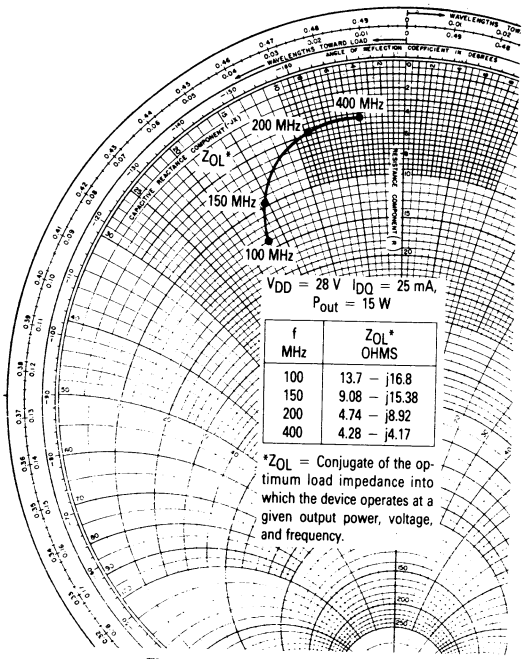


Figure 22. Large-Signal Series Equivalent Output Impedance, Z_{OL}*
MRF136

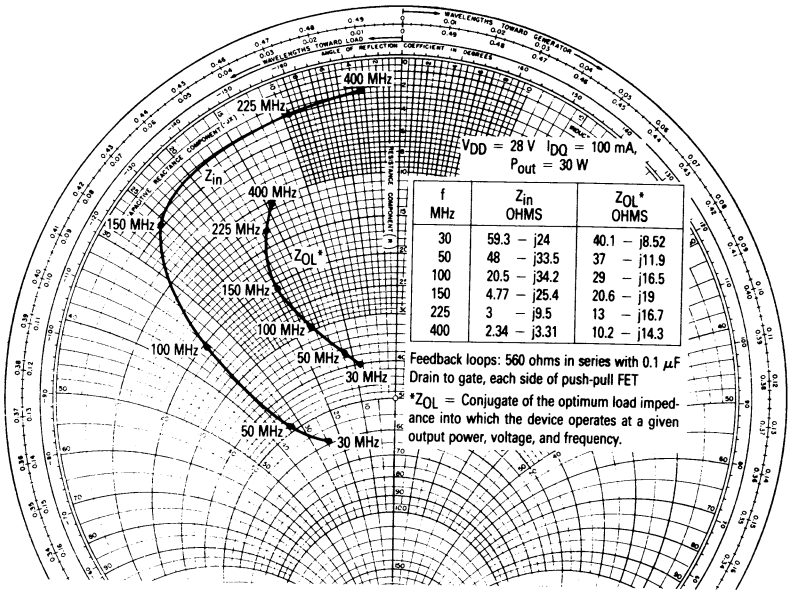


Figure 23. Input and Output Impedance
MRF136Y

MRF136

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
2.0	0.988	-11	41.19	173	0.006	67	0.729	-12
5.0	0.970	-27	40.07	164	0.014	62	0.720	-31
10	0.923	-52	35.94	149	0.026	54	0.714	-58
20	0.837	-88	27.23	129	0.040	36	0.690	-96
30	0.784	-111	20.75	117	0.046	27	0.684	-118
40	0.751	-125	16.49	108	0.048	22	0.680	-131
50	0.733	-135	13.41	103	0.050	19	0.679	-139
60	0.720	-142	11.43	99	0.050	16	0.678	-145
70	0.709	-147	9.871	96	0.050	14	0.679	-149
80	0.707	-152	8.663	93	0.051	13	0.683	-153
90	0.706	-155	7.784	91	0.051	13	0.682	-155
100	0.708	-157	7.008	88	0.051	13	0.680	-157
110	0.711	-159	6.435	86	0.051	14	0.681	-158
120	0.714	-161	5.899	85	0.051	15	0.682	-159
130	0.717	-163	5.439	82	0.052	16	0.684	-160
140	0.720	-164	5.068	80	0.052	17	0.684	-161
150	0.723	-165	4.709	80	0.052	18	0.686	-161
160	0.727	-166	4.455	78	0.052	18	0.690	-161
170	0.732	-167	4.200	77	0.052	18	0.694	-162
180	0.735	-168	3.967	75	0.052	19	0.699	-162
190	0.738	-169	3.756	74	0.052	19	0.703	-163
200	0.740	-170	3.545	73	0.052	20	0.706	-163
225	0.746	-171	3.140	69	0.053	22	0.717	-163
250	0.742	-172	2.783	67	0.053	25	0.724	-163
275	0.744	-173	2.540	64	0.054	27	0.724	-163
300	0.751	-174	2.323	60	0.055	29	0.736	-163
325	0.757	-175	2.140	58	0.058	32	0.749	-163
350	0.760	-176	1.963	54	0.059	35	0.758	-163
375	0.762	-177	1.838	52	0.062	38	0.768	-163
400	0.774	-179	1.696	50	0.065	41	0.783	-163
425	0.775	-179	1.590	48	0.068	43	0.793	-163
450	0.781	+179	1.493	46	0.071	46	0.805	-163
475	0.787	+177	1.415	43	0.074	47	0.813	-164
500	0.792	+176	1.332	40	0.079	48	0.825	-164
525	0.797	+175	1.259	38	0.083	50	0.831	-164
550	0.801	+175	1.185	37	0.088	51	0.843	-164
575	0.810	+174	1.145	36	0.094	52	0.855	-164
600	0.816	+173	1.091	34	0.101	52	0.869	-165
625	0.818	+171	1.041	32	0.106	53	0.871	-165
650	0.825	+170	0.994	30	0.112	53	0.884	-165
675	0.834	+169	0.962	29	0.119	53	0.890	-165
700	0.837	+168	0.922	27	0.127	53	0.906	-166
725	0.836	+167	0.879	25	0.133	52	0.909	-167
750	0.841	+166	0.838	25	0.140	53	0.917	-167
775	0.844	+165	0.824	24	0.148	52	0.933	-167
800	0.846	+163	0.785	21	0.154	50	0.941	-168

Figure 24. Common Source Scattering Parameters
V_{DS} = 28 V, I_D = 0.5 A

MRF136

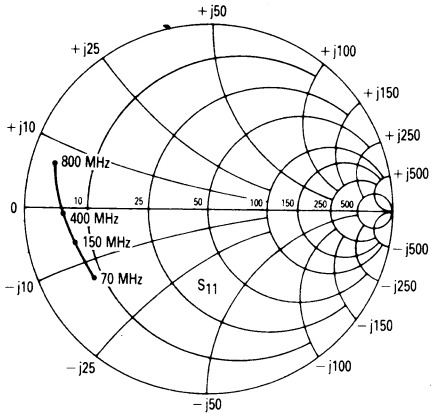


Figure 25. S_{11}, Input Reflection Coefficient versus Frequency
V_{DS} = 28 V I_D = 0.5 A

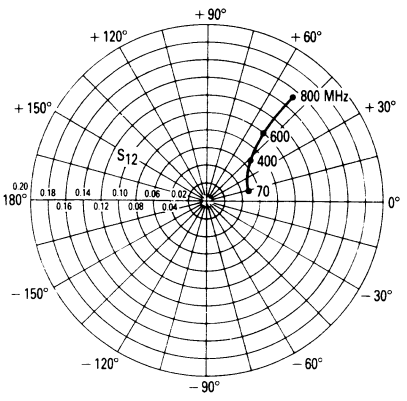


Figure 26. S_{12}, Reverse Transmission Coefficient versus Frequency
V_{DS} = 28 V I_D = 0.5 A

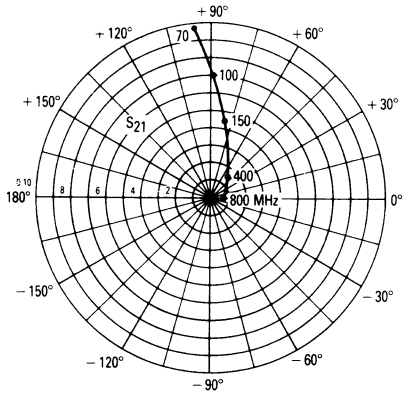


Figure 27. S_{21}, Forward Transmission Coefficient versus Frequency
V_{DS} = 28 V I_D = 0.5 A

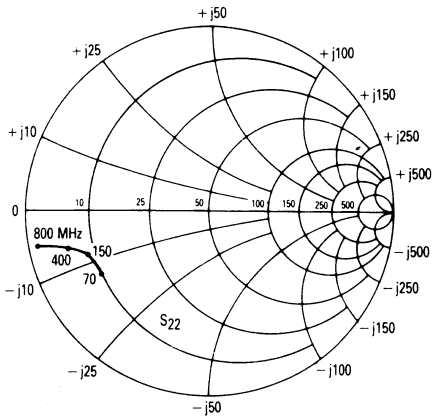


Figure 28. S_{22}, Output Reflection Coefficient versus Frequency
V_{DS} = 28 V I_D = 0.5 A

3

DESIGN CONSIDERATIONS

The MRF136 and MRF136Y are TMOS RF power N-Channel enhancement mode field-effect transistors (FETs) designed especially for HF and VHF power amplifier applications. Motorola TMOS FETs feature planar design for optimum manufacturability.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of TMOS RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF136 and MRF136Y are enhancement mode FETs and, therefore, do not conduct when drain voltage is applied without gate bias. A positive gate voltage causes drain current to flow (see Figure 11). RF power FETs require forward bias for optimum gain and power output. A Class AB condition with quiescent drain current (I_{DQ}) in the 25–100 mA range is sufficient for many applications. For special requirements such as linear amplification, I_{DQ} may have to be adjusted to optimize the critical parameters.

The MOS gate is a dc open circuit. Since the gate bias circuit does not have to deliver any current to the FET, a simple resistive divider arrangement may sometimes suffice for this function. Special applications may require more elaborate gate bias systems.

GAIN CONTROL

Power output of the MRF136 and MRF136Y may be controlled from rated values down to the milliwatt region (>20 dB reduction in power output with constant input power) by varying the dc gate voltage. This feature, not available in bipolar RF power devices, facilitates the incorporation of manual gain control, AGC/ALC, and modulation schemes into system designs. A full range of power output control may require dc gate voltage excursions into the negative region.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for the MRF136 and MRF136Y. See Motorola Application Note AN721, Impedance Matching Networks Applied to RF Power Transistors. Both small signal scattering parameters (MRF136 only) and large signal impedance parameters are provided. Large signal impedances should be used for network designs wherever possible. While the s parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is particularly useful at frequencies outside those presented in the large signal impedance plots.

RF power FETs are triode devices and are therefore not unilateral. This, coupled with their very high gain, yields a device capable of self oscillation. Stability may be achieved using techniques such as drain loading, input shunt resistive loading, or feedback. S parameter stability analysis can provide useful information in the selection of loading and/or feedback to insure stable operation. The MRF136 was characterized with a 27 ohm input shunt loading resistor, while the MRF136Y was characterized with a resistive feedback loop around each of its two active devices.

For further discussion of RF amplifier stability and the use of two port parameters in RF amplifier design, see Motorola Application Note AN215A on page 6-204 in the RF Device Data (DL110 Rev 1).

LOW NOISE OPERATION

Input resistive loading will degrade noise performance, and noise figure may vary significantly with gate driving impedance. A low loss input matching network with its gate impedance optimized for lowest noise is recommended.

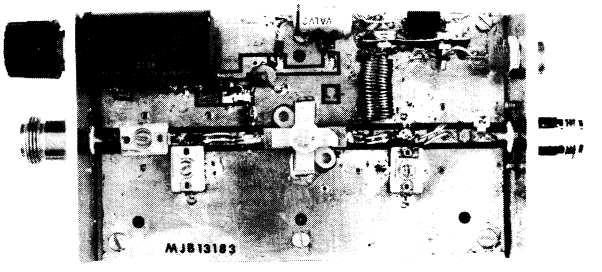


Figure 29. MRF136 Test Circuit

MRF137

The RF TMOS Line

30 W 2.0-400 MHz

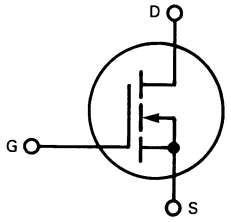
N-CHANNEL TMOS BROADBAND RF POWER FET

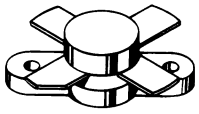
N-CHANNEL ENHANCEMENT-MODE TMOS RF POWER FIELD-EFFECT TRANSISTOR

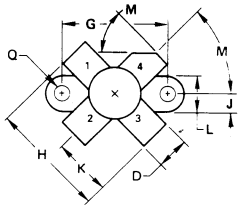
. . . designed for wideband large-signal output and driver stages in the 2.0 to 400 MHz range.

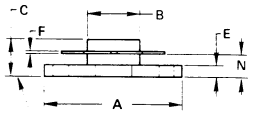
- Guaranteed 28 Volt, 150 MHz Performance
  Output Power = 30 Watts
  Minimum Gain = 13 dB
  Efficiency = 60% (Typical)
- Small-Signal and Large-Signal Characterization
- Typical Performance at 400 MHz, 28 Vdc, 30 W
  Output = 7.7 dB Gain
- 100% Tested for Load Mismatch at All Phase Angles with 30:1 VSWR
- Low Noise Figure — 1.5 dB (Typ) at 1.0 A, 150 MHz
- Excellent Thermal Stability, Ideally Suited for Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques

TMOS™









STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.29	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

CASE 211-07

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	5.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.571	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

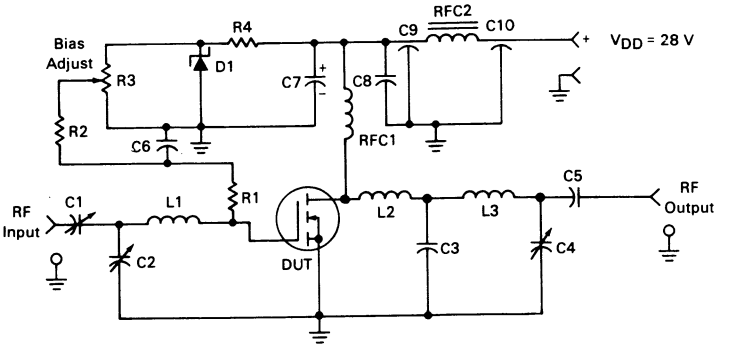
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	4.0	mAdc
Gate-Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 25 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 500 mA)	g_{fs}	500	750	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	48	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	54	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	11	—	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure (V_{DS} = 28 Vdc, I_D = 1.0 A, f = 150 MHz)	NF	—	1.5	—	dB
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 30 W, I_{DQ} = 25 mA) f = 150 MHz (Figure 1)	G_{ps}	13	16	—	dB
f = 400 MHz (Figure 14)		—	7.7	—	
Drain Efficiency (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 30 W, f = 150 MHz, I_{DQ} = 25 mA)	η	50	60	—	%
Electrical Ruggedness (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 30 W, f = 150 MHz, I_{DQ} = 25 mA, VSWR 30:1 at All Phase Angles)	ψ	No Degradation in Output Power			

FIGURE 1 — 150 MHz TEST CIRCUIT



C1 — Arco 406, 15–115 pF, or equivalent
C2 — Arco 403, 3.0–35 pF, or equivalent
C3 — 56 pF Mini-Unleco, or equivalent
C4 — Arco 404, 8.0–60 pF, or equivalent
C5 — 680 pF, 100 Mils Chip
C6 — 0.01 μF, 100 V, Disc Ceramic
C7 — 100 μF, 40 V
C8 — 0.1 μF, 50 V, Disc Ceramic
C9, C10 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener

L1 — 2 Turns, 0.29" ID, #18 AWG Enamel, Closewound
L2 — 1¼ Turns, 0.2" ID, #18 AWG Enamel, Closewound
L3 — 2 Turns, 0.2" ID, #18 AWG Enamel, Closewound
RFC1 — 20 Turns, 0.30" ID, #20 AWG Enamel, Closewound
RFC2 — Ferroxcube VK-200 — 19/4B
R1 — 10 kΩ, ½ W Thin Film
R2 — 10 kΩ, ¼ W
R3 — 10 Turns, 10 kΩ
R4 — 1.8 kΩ, ½ W
Board — G10, 62 Mils

FIGURE 2 — OUTPUT POWER versus INPUT POWER

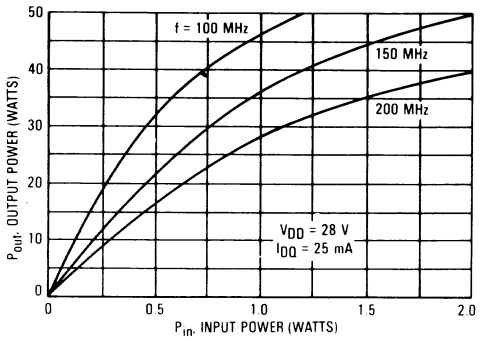


FIGURE 3 — OUTPUT POWER versus INPUT POWER

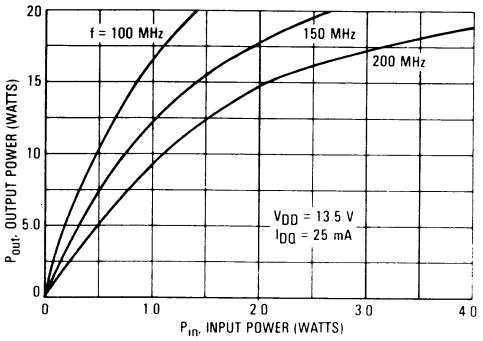


FIGURE 4 — OUTPUT POWER versus INPUT POWER

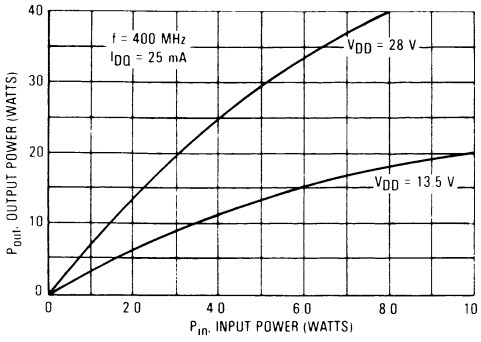


FIGURE 5 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 100 MHz

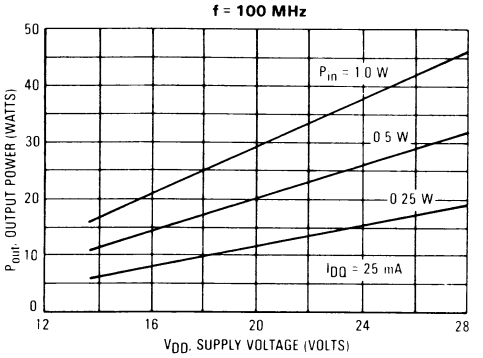


FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 150 MHz

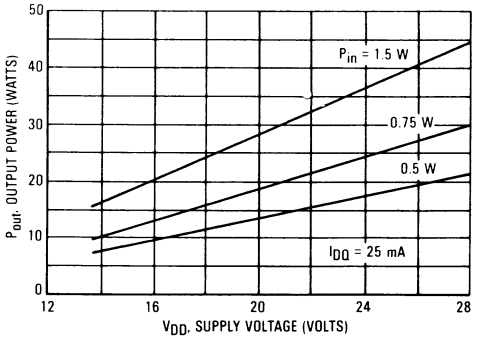


FIGURE 7 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 200 MHz

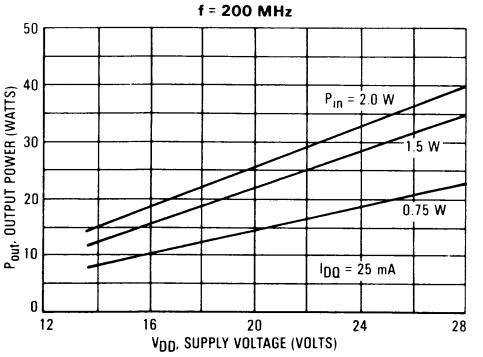


FIGURE 8 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 400 MHz

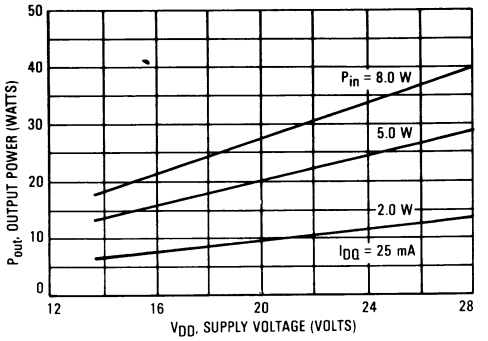


FIGURE 9 — OUTPUT POWER versus GATE VOLTAGE

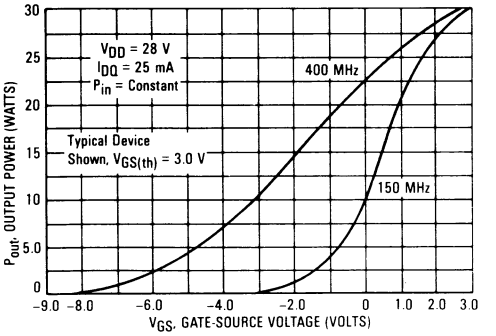


FIGURE 10 — DRAIN CURRENT versus GATE VOLTAGE
(TRANSFER CHARACTERISTICS)

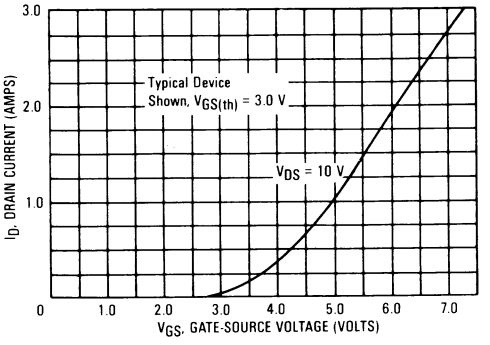


FIGURE 11 — GATE SOURCE VOLTAGE versus
CASE TEMPERATURE

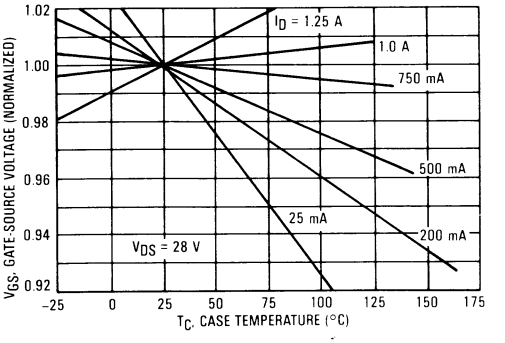


FIGURE 12 — CAPACITANCE versus
DRAIN-SOURCE VOLTAGE

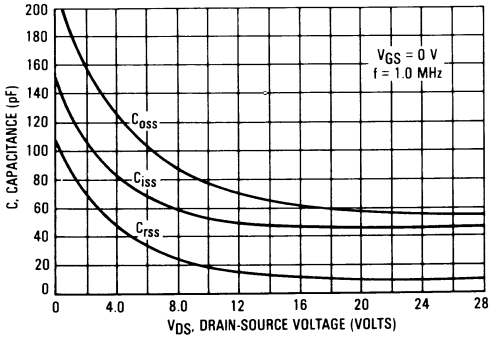


FIGURE 13 — DC SAFE OPERATING AREA

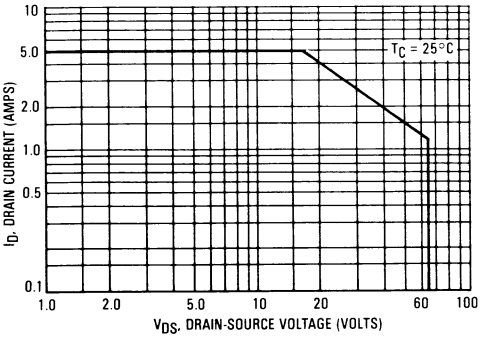
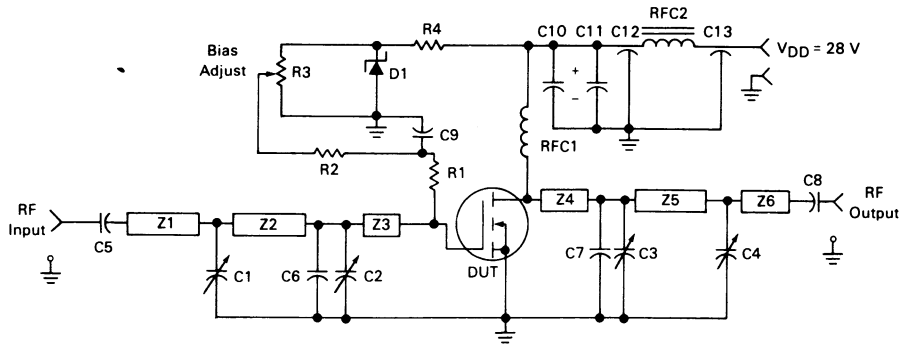
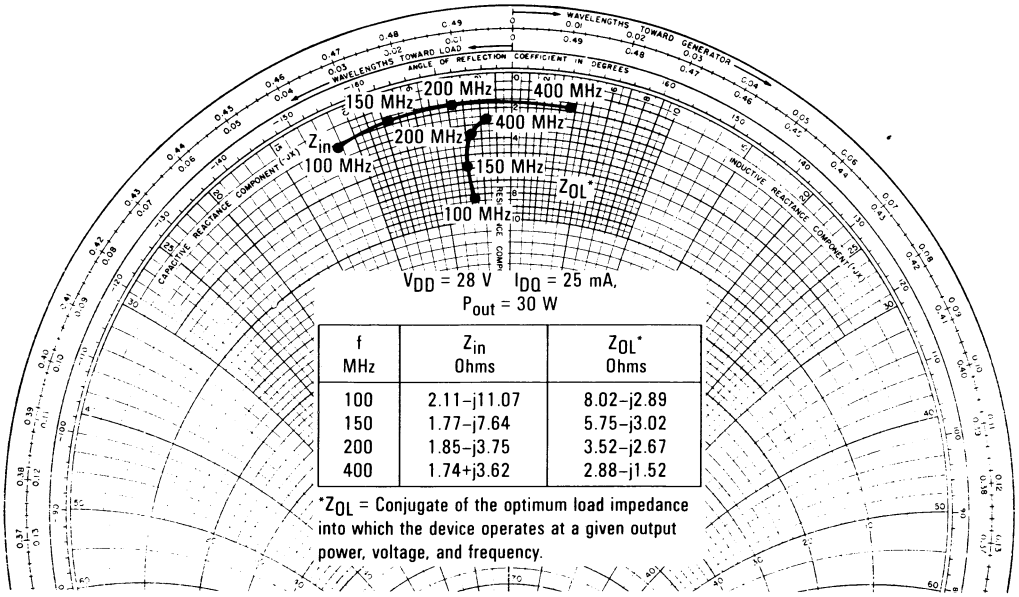


FIGURE 14 — 400 MHz TEST CIRCUIT



C1, C2, C3, C4 — 0-20 pF Johanson, or equivalent
C5, C8 — 270 pF, 100 Mil Chip
C6, C7 — 24 pF Mini-Unleco, or equivalent
C9 — 0.01 μF, 100 V, Disc Ceramic
C10 — 100 μF, 40 V
C11 — 0.1 μF, 50 V, Disc Ceramic
C12, C13 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener
R1, R2 — 10 kΩ, ¼ W
R3 — 10 Turns, 10 kΩ
R4 — 1.8 kΩ, ½ W
Z1 — 2.9" × 0.166" Microstrip
Z2, Z4 — 0.35" × 0.166" Microstrip
Z3 — 0.40" × 0.166" Microstrip
Z5 — 1.05" × 0.166" Microstrip
Z6 — 1.9" × 0.166" Microstrip
RFC1 — 6 Turns, 0.300" ID, #20 AWG Enamel, Closewound
RFC2 — Ferroxcube VK-200 — 19/4B
Board — Glass Teflon, 62 Mils

FIGURE 15 — LARGE-SIGNAL SERIES EQUIVALENT INPUT AND OUTPUT IMPEDANCE, Z_{in}, Z_{OL}^*



f MHz	Z_{in} Ohms	Z_{OL}^* Ohms
100	2.11–j11.07	8.02–j2.89
150	1.77–j7.64	5.75–j3.02
200	1.85–j3.75	3.52–j2.67
400	1.74+j3.62	2.88–j1.52

*Z_{OL}^* = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

FIGURE 16 — COMMON SOURCE SCATTERING PARAMETERS
50 Ω SYSTEM
V_{DS} = 28 V, I_D = 0.75 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
2.0	0.977	-32	59.48	163	0.011	67	0.661	-36
5.0	0.919	-70	48.67	142	0.024	44	0.692	-78
10	0.852	-109	33.50	122	0.032	29	0.747	-117
20	0.817	-140	19.05	106	0.037	16	0.768	-146
30	0.814	-153	13.11	99	0.038	14	0.774	-157
40	0.811	-159	9.88	95	0.038	13	0.782	-162
50	0.812	-164	7.98	92	0.038	12	0.787	-165
60	0.813	-166	6.66	89	0.038	12	0.787	-168
70	0.815	-168	5.708	86	0.038	11	0.787	-169
80	0.816	-170	5.003	84	0.038	11	0.787	-170
90	0.817	-171	4.560	83	0.038	12	0.787	-171
100	0.817	-172	4.170	81	0.039	13	0.787	-172
110	0.818	-173	3.670	80	0.039	13	0.788	-172
120	0.820	-173	3.420	79	0.039	13	0.788	-173
130	0.821	-173	3.170	79	0.039	13	0.788	-173
140	0.822	-174	2.980	78	0.039	13	0.788	-173
150	0.823	-175	2.826	77	0.039	14	0.788	-173
160	0.824	-175	2.650	76	0.039	14	0.790	-174
170	0.825	-176	2.438	75	0.039	14	0.792	-174
180	0.827	-176	2.325	73	0.039	15	0.793	-174
190	0.829	-177	2.175	72	0.039	16	0.796	-174
200	0.831	-177	2.084	71	0.039	16	0.799	-174
225	0.836	-178	1.824	69	0.039	18	0.805	-174
250	0.846	-178	1.621	66	0.039	21	0.816	-174
275	0.853	-179	1.462	64	0.039	23	0.822	-174
300	0.853	-179	1.319	61	0.040	25	0.833	-174
325	0.856	-179	1.194	59	0.040	27	0.828	-174
350	0.857	+179	1.089	56	0.040	30	0.842	-174
375	0.861	+179	1.014	54	0.042	32	0.849	-174
400	0.865	+178	0.927	51	0.043	35	0.856	-174
425	0.875	+178	0.876	49	0.045	37	0.866	-174
450	0.881	+178	0.810	46	0.046	40	0.870	-174
475	0.886	+177	0.755	44	0.046	43	0.875	-174
500	0.887	+177	0.694	41	0.051	43	0.888	-174
525	0.888	+176	0.677	39	0.052	43	0.890	-174
550	0.896	+176	0.625	36	0.055	45	0.898	-174
575	0.907	+175	0.603	34	0.058	45	0.913	-174
600	0.910	+175	0.585	32	0.061	45	0.918	-174
625	0.910	+174	0.563	30	0.065	45	0.945	-174
650	0.920	+174	0.543	28	0.069	46	0.952	-174
675	0.938	+173	0.533	26	0.074	47	0.974	-174
700	0.943	+171	0.515	24	0.078	47	0.958	-176
725	0.934	+170	0.491	22	0.079	46	0.953	-177
750	0.940	+170	0.475	22	0.084	48	0.943	-177
775	0.953	+169	0.477	21	0.090	48	0.957	-177
800	0.959	+168	0.467	17	0.093	48	0.957	-179

FIGURE 17 — S_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 0.75 A

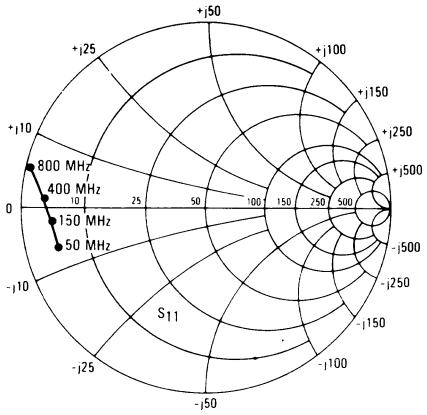


FIGURE 18 — S_{12}, REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 0.75 A

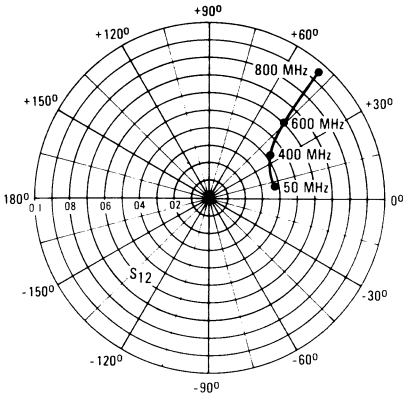


FIGURE 19 — S_{21}, FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 0.75 A

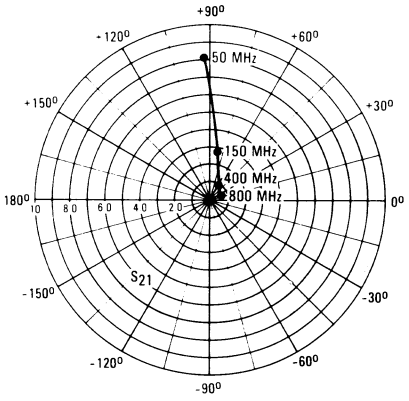
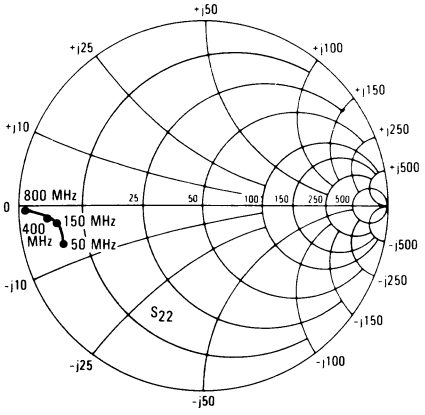


FIGURE 20 — S_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 0.75 A



3

DESIGN CONSIDERATIONS

The MRF137 is a TMOS RF power N-Channel enhancement mode field-effect transistor (FET) designed especially for VHF power amplifier applications. Motorola TMOS FETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V-groove vertical power FETs.

Motorola Application Note AN-211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of TMOS RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF137 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 10 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF137 was characterized at I_{DQ} = 25 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF137 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC, and modulation systems. (See Figure 9.)

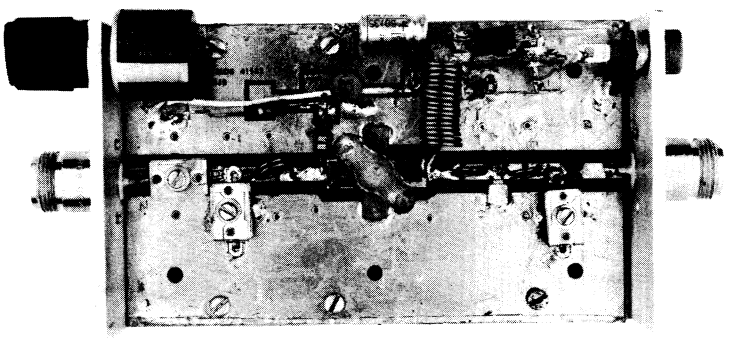
AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar VHF transistors are suitable for MRF137. See Motorola Application Note AN-721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of TMOS FETs helps ease the task of broadband network design. Both small signal scattering parameters and large signal impedances are provided. While the s-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of TMOS power FETs.

RF power FETs are triode devices and, therefore, not unilateral. This, coupled with the very high gain of the MRF137, yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. Two port parameter stability analysis with the MRF137 s-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN-215A for a discussion of two port network theory and stability.

3

FIGURE 21 — 150 MHz TEST CIRCUIT



MRF138

The RF TMOS Line

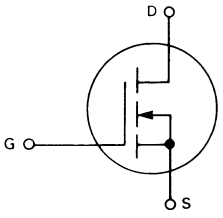
30 W 2.0-175 MHz

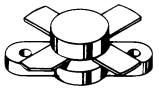
N-CHANNEL TMOS
LINEAR RF POWER
FET

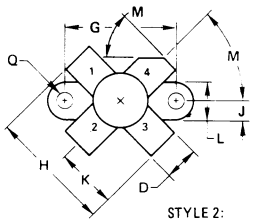
N-CHANNEL ENHANCEMENT-MODE TMOS RF POWER FIELD-EFFECT TRANSISTOR

. . . designed for power amplifier applications in industrial, commercial and amateur radio equipment to 175 MHz.

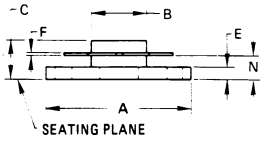
- Superior High Order IMD
- Specified 28 Volts, 30 MHz Characteristics
  - Output Power = 30 Watts
  - Power Gain = 17 dB (Typ)
  - Efficiency = 40% (Typ)
- $IMD_{(d3)}$ (30 W PEP) = -30 dB (Typ)
- $IMD_{(d11)}$ (30 W PEP) = -60 dB (Typ)
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR







STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.29	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

CASE 211-07

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	6.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.66	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	°C/W

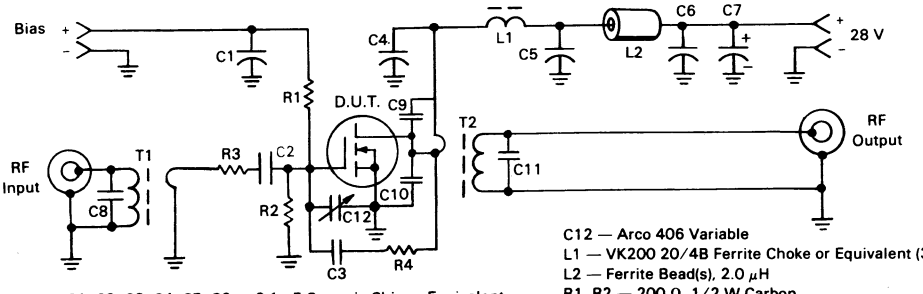
Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate-Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 10 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V, I_D = 2.5 A)	$V_{DS(on)}$	—	—	2.5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.5 A)	g_{fs}	0.8	1.2	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	—	55	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	70	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	14	—	pF
FUNCTIONAL TESTS (SSB)					
Common Source Amplifier Power Gain (V_{DD} = 28 V, P_{out} = 30 W (PEP), I_{DQ} = 100 mA) (30 MHz) (Fig. 1) (150 MHz) (Fig. 6)	G_{ps}	— —	17 14	— —	dB
Drain Efficiency (Figure 1) (V_{DD} = 28 V, f = 30 MHz, I_{DQ} = 100 mA) (30 W PEP) (30 W CW)	η	— —	40 50	— —	%
Intermodulation Distortion (Figure 1) (V_{DD} = 28 V, P_{out} = 30 W (PEP), f = 30; 30.001 MHz, I_{DQ} = 100 mA)	$IMD_{(d3)}$ $IMD_{(d11)}$	— —	-30 -60	— —	dB
Load Mismatch (Figure 1) (V_{DD} = 28 V, P_{out} = 30 W (PEP), f = 30; 30.001 MHz, I_{DQ} = 100 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			
CLASS A PERFORMANCE					
Intermodulation Distortion (1) and Power Gain (V_{DD} = 28 V, P_{out} = 10 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 1.0 A)	G_{PS} $IMD_{(d3)}$ $IMD_{(d9-13)}$	— — —	20 -50 -70	— — —	dB

(1) To MIL-STD-1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.

FIGURE 1 — 2-50 MHz BROADBAND TEST CIRCUIT



C1, C2, C3, C4, C5, C6 — 0.1 μF Ceramic Chip or Equivalent
C7 — 10 μF, 100 V Electrolytic
C8 — 10 pF Dipped Mica
C9 — 68 pF Dipped Mica
C10, C11 — 47 pF Dipped Mica
C12 — Arco 406 Variable
L1 — VK200 20/4B Ferrite Choke or Equivalent (3.0 μH)
L2 — Ferrite Bead(s), 2.0 μH
R1, R2 — 200 Ω, 1/2 W Carbon
R3 — 2.2 Ω, 1/2 W Carbon
R4 — 330 Ω, 1.0 W Carbon
T1 — 4:1 Impedance Transformer
T2 — 1:4 Impedance Transformer

FIGURE 2 — POWER GAIN versus FREQUENCY

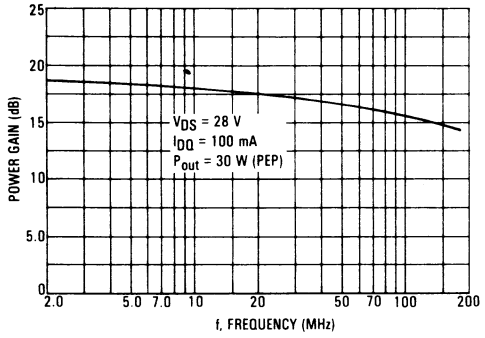


FIGURE 3 — OUTPUT POWER versus INPUT POWER

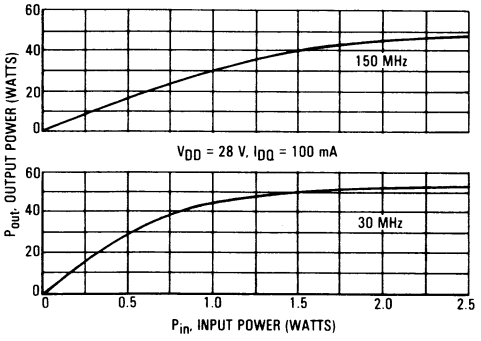


FIGURE 4 — IMD versus P_{out}

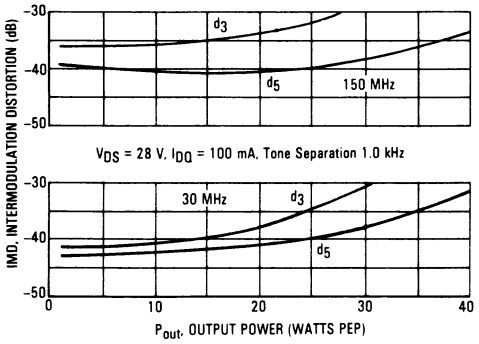


FIGURE 5 — COMMON SOURCE UNITY CURRENT GAIN FREQUENCY versus DRAIN CURRENT

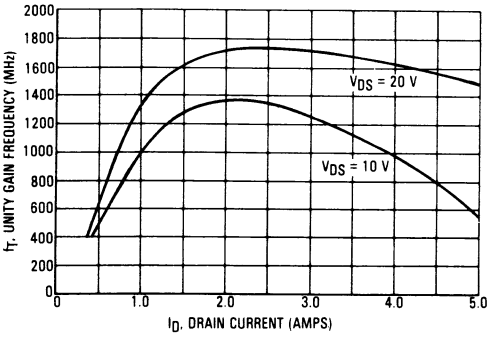
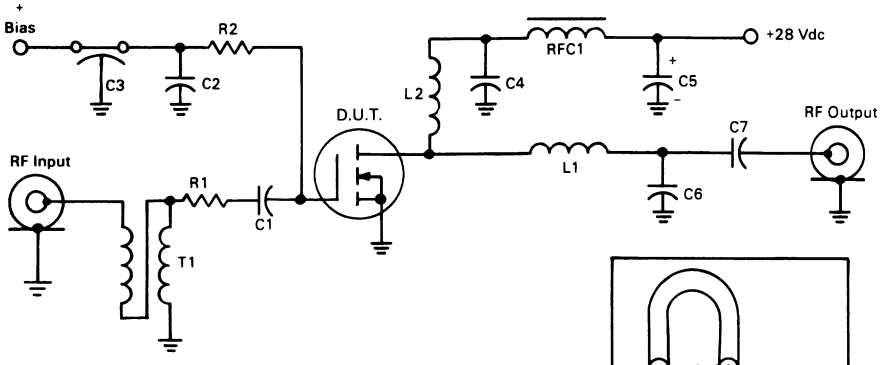


FIGURE 6 — 150 MHz TEST CIRCUIT



C1 — 91 pF Unelco Type MCM 01/010
C2, C4 — 0.1 μF Erie Red Cap
C3 — Allen Bradley 680 pF Feed Thru
C5 — 1.0 μF, 50 Vdc Electrolytic
C6 — Arco 402 Varible
C7 — Arco 404 Variable
L1 — 2 Turns # 18 AWG, 5/16" ID

L2 — 4 Turns # 18 AWG, 5/16" ID
R1 = 1.0 Ohm, 1/4 W Carbon
R2 — 2000 Ohm, 1/4 W Carbon
RFC1 — VK200 21/4B
T1 — 4:1 Transformer, 1.75" Subminiature Coaxial Cable

T1 — 4:1 Impedance Ratio Transformer, Line Impedance = 25 Ω

FIGURE 7 — GATE VOLTAGE versus DRAIN CURRENT

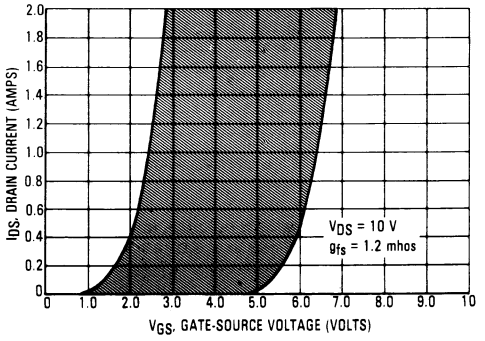


FIGURE 8 — DC SAFE OPERATING AREA

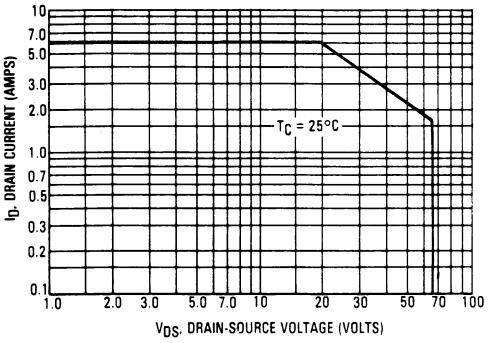


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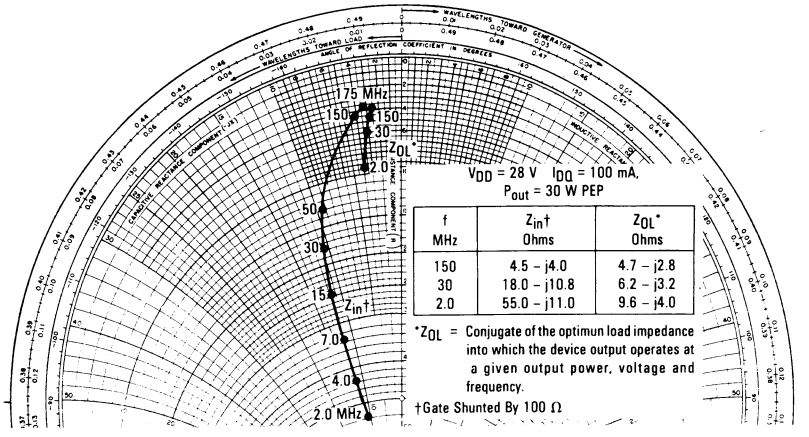
FIGURE 9 — LARGE-SIGNAL SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE, Z_{in}†, Z_{OL}*



f MHz	Z_{in}† Ohms	Z_{OL}* Ohms
150	4.5 – j4.0	4.7 – j2.8
30	18.0 – j10.8	6.2 – j3.2
2.0	55.0 – j11.0	9.6 – j4.0

*Z_{OL} = Conjugate of the optimun load impedance into which the device output operates at a given output power, voltage and frequency.

†Gate Shunted By 100 Ω

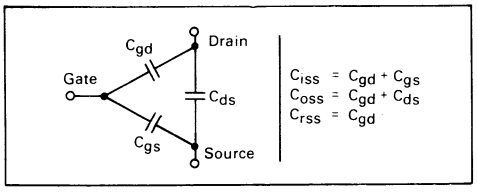
TMOS POWER FET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during the fabrication of the TMOS FET results in a junction capacitance from drain-to-source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the interterminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate-source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the TMOS FET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended.

3

EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{fe}	g_{fs}
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$	$r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$