**MOTOROLA**
**SEMICONDUCTOR**
**TECHNICAL DATA**

# MRF141

### The RF MOSFET Line

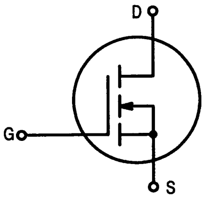
# RF Power Field-Effect Transistor

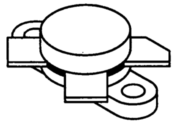
## N-Channel Enhancement-Mode MOSFET

**150 W, 28 V, 175 MHz**
**N-CHANNEL**
**BROADBAND**
**RF POWER MOSFET**

. . . designed for broadband commercial and military applications at frequencies to 175 MHz. The high power, high gain and broadband performance of this device makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance at 30 MHz, 28 V:
  Output Power — 150 W
  Gain — 18 dB (22 dB Typ)
  Efficiency — 40%
- Typical Performance at 175 MHz, 50 V:
  Output Power — 150 W
  Gain — 13 dB
- Low Thermal Resistance
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability





**CASE 211-11, STYLE 2**

**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DSS}$ | 65 | Vdc |
| Drain-Gate Voltage | $V_{DGO}$ | 65 | Vdc |
| Gate-Source Voltage | $V_{GS}$ | ±40 | Vdc |
| Drain Current — Continuous | $I_D$ | 16 | Adc |
| Total Device Dissipation @ $T_C = 25°C$<br>Derate above 25°C | $P_D$ | 300<br>1.71 | Watts<br>W/°C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Operating Junction Temperature | $T_J$ | 200 | °C |

**THERMAL CHARACTERISTICS**

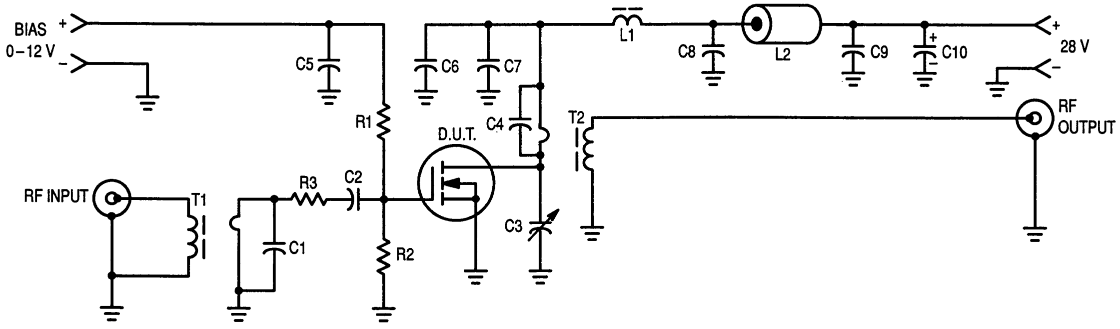
| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 0.6 | °C/W |

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS (1)** | | | | | |
| Drain-Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 100 mA) | $V_{(BR)DSS}$ | 65 | — | — | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 28 V, $V_{GS}$ = 0) | $I_{DSS}$ | — | — | 5.0 | mAdc |
| Gate-Body Leakage Current ($V_{GS}$ = 20 V, $V_{DS}$ = 0) | $I_{GSS}$ | — | — | 1.0 | µAdc |
| **ON CHARACTERISTICS (1)** | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = 10 V, $I_D$ = 100 mA) | $V_{GS(th)}$ | 1.0 | 3.0 | 5.0 | Vdc |
| Drain-Source On-Voltage ($V_{GS}$ = 10 V, $I_D$ = 10 A) | $V_{DS(on)}$ | — | — | 1.5 | Vdc |
| Forward Transconductance ($V_{DS}$ = 10 V, $I_D$ = 5.0 A) | $g_{fs}$ | 5.0 | 7.0 | — | mhos |
| **DYNAMIC CHARACTERISTICS (1)** | | | | | |
| Input Capacitance ($V_{DS}$ = 28 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{iss}$ | — | 350 | — | pF |
| Output Capacitance ($V_{DS}$ = 28 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{oss}$ | — | 420 | — | pF |
| Reverse Transfer Capacitance ($V_{DS}$ = 28 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{rss}$ | — | 40 | — | pF |
| **FUNCTIONAL TESTS** | | | | | |
| Common Source Amplifier Power Gain, f = 30; 30.001 MHz<br>($V_{DD}$ = 28 V, $P_{out}$ = 150 W (PEP), $I_{DQ}$ = 250 mA) f = 175 MHz | $G_{ps}$ | 16<br>— | 20<br>10 | —<br>— | dB |
| Drain Efficiency ($V_{DD}$ = 28 V, $P_{out}$ = 150 W (PEP), f = 30; 30.001 MHz, $I_{DQ}$ = 250 mA, $I_D$ (Max) = 5.95 A) | η | 40 | 45 | — | % |
| Intermodulation Distortion (1)<br>($V_{DD}$ = 28 V, $P_{out}$ = 150 W (PEP), f = 30 MHz, f2 = 30.001 MHz, $I_{DQ}$ = 250 mA) | $IMD_{(d3)}$<br>$IMD_{(d11)}$ | —<br>— | −30<br>−60 | −28<br>— | dB |
| Load Mismatch ($V_{DD}$ = 28 V, $P_{out}$ = 150 W (PEP), f1 = 30; 30.001 MHz, $I_{DQ}$ = 250 mA, VSWR 30:1 at all Phase Angles) | ψ | No Degradation in Output Power | | | |
| **CLASS A PERFORMANCE** | | | | | |
| Intermodulation Distortion (1) and Power Gain<br>($V_{DD}$ = 28 V, $P_{out}$ = 50 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, $I_{DQ}$ = 4.0 A) | $G_{PS}$<br>$IMD_{(d3)}$<br>$IMD_{(d9-13)}$ | —<br>—<br>— | 23<br>−50<br>−75 | —<br>—<br>— | dB |

NOTE:
1. To MIL-STD-1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.



C1 — 820 pF Dipped Mica
C2, C5, C6, C7, C8, C9 — 0.1 µF Ceramic Chip or Monolythic with Short Leads
C3 — Arco 469
C4 — 560 pF Unencapsulated Mica or Dipped Mica with Short Leads
C10 — 10 µF/100 V Electrolytic

L1 — VK200/4B Ferrite Choke or Equivalent, 3.0 µH
L2 — Ferrite Bead(s), 2.0 µH
R1, R2 — 51 Ω/1.0 W Carbon
R3 — 1.0 Ω/1.0 W Carbon
T1 — 16:1 Broadband Transformer
T2 — 1:25 Broadband Transformer
Board Material — 0.062″ Fiberglass (G10), 1 oz. Copper Clad, 2 Sides, $\varepsilon_r$ = 5

**Figure 1. 30 MHz Test Circuit**

## TYPICAL CHARACTERISTICS

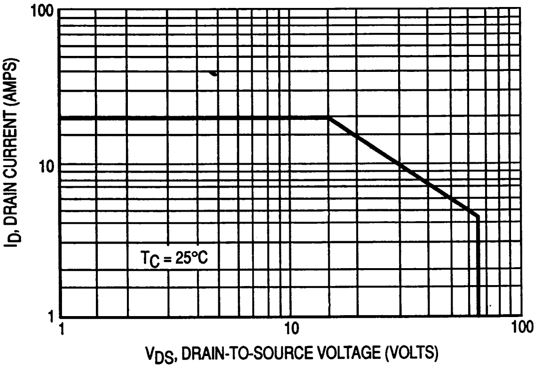


Figure 2. DC Safe Operating Area

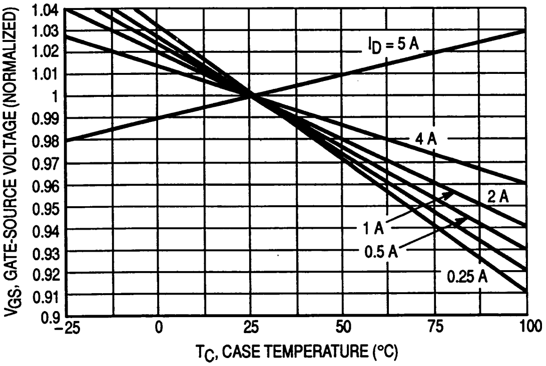


Figure 3. Gate-Source Voltage versus Case Temperature

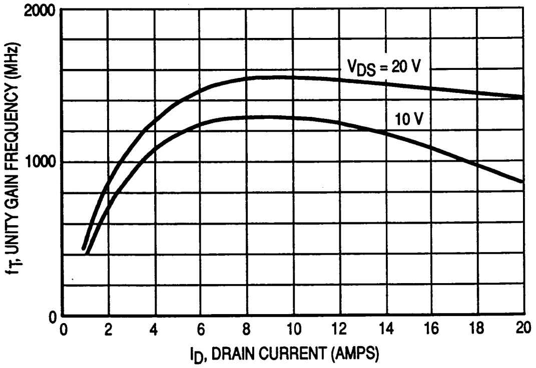


Figure 4. Common Source Unity Gain Frequency versus Drain Current

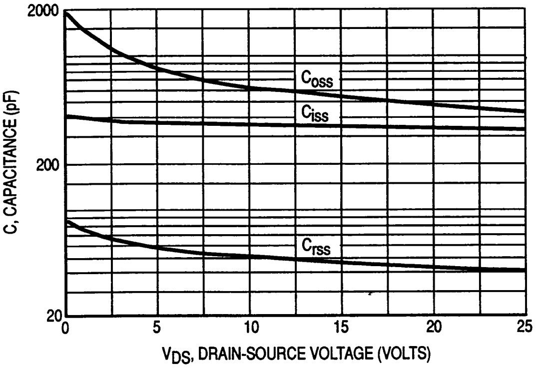


Figure 5. Capacitance versus Drain-Source Voltage

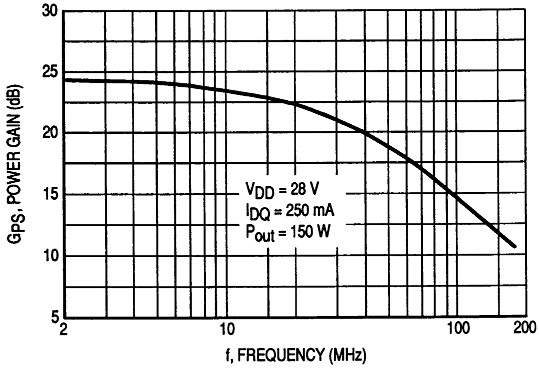


Figure 6. Power Gain versus Frequency

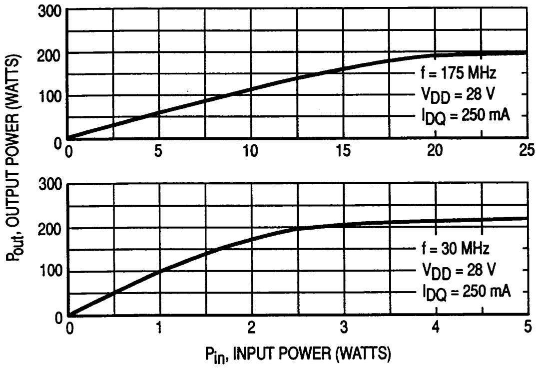


Figure 7. Output Power versus Input Power

## TYPICAL CHARACTERISTICS

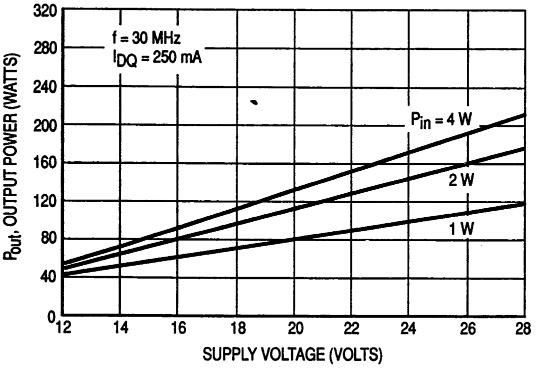


**Figure 8. Output Power versus Supply Voltage**

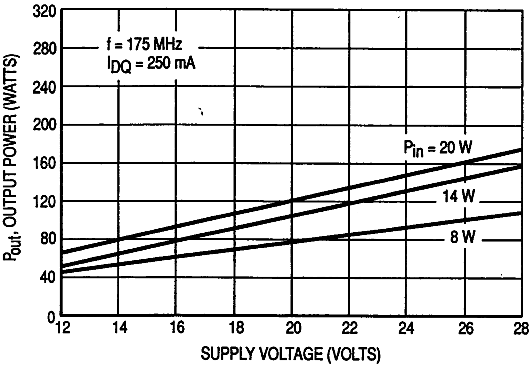
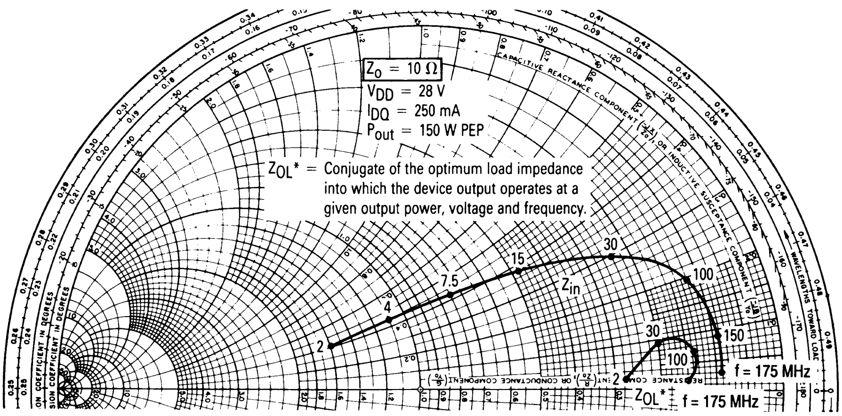


**Figure 9. Output Power versus Supply Voltage**



$Z_{OL}$* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

**Figure 10. Input and Output Impedances**

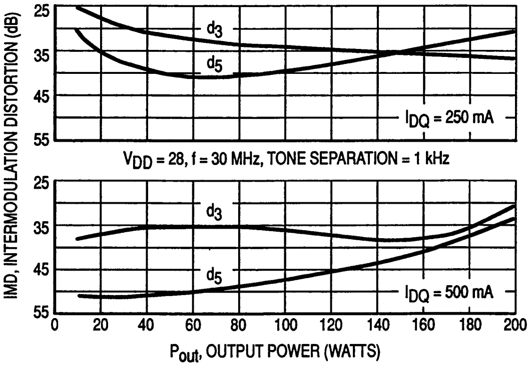


**Figure 11. IMD versus $P_{out}$ (PEP)**

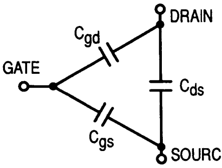
## RF POWER MOSFET CONSIDERATIONS

### MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal anode gate structure determines the capacitors from gate-to-drain ($C_{gd}$), and gate-to-source ($C_{gs}$). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain-to-source ($C_{ds}$).

These capacitances are characterized as input ($C_{iss}$), output ($C_{oss}$) and reverse transfer ($C_{rss}$) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The $C_{iss}$ can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



$C_{iss} = C_{gd} = C_{gs}$
$C_{oss} = C_{gd} = C_{ds}$
$C_{rss} = C_{gd}$

### LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 4 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to $f_T$ for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

### DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate-source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

### GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of $10^9$ ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage, $V_{GS(th)}$.

**Gate Voltage Rating** — Never exceed the gate voltage rating. Exceeding the rated $V_{GS}$ can result in permanent damage to the oxide layer in the gate region.

**Gate Termination** — The gate of this device is essentially capacitor. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage build-up on the input capacitor due to leakage currents or pickup.

**Gate Protection** — This device does not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate-to-source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

### HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with a grounded iron.

### DESIGN CONSIDERATIONS

The MRF141 is an RF Power, MOS, N-channel enhancement mode field-effect transistor (FET) designed for HF and VHF power amplifier applications.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power MOSFETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal.

### DC BIAS

The MRF141 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current ($I_{DQ}$) is not critical for many applications. The MRF141 was characterized at $I_{DQ}$ = 250 mA, each side, which is the suggested minimum value of $I_{DQ}$. For special applications such as linear amplification, $I_{DQ}$ may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias sytem.

### GAIN CONTROL

Power output of the MRF141 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

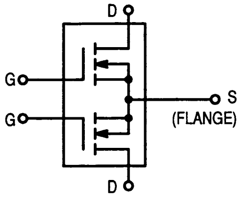
**MOTOROLA**
**SEMICONDUCTOR**
**TECHNICAL DATA**

# MRF141G

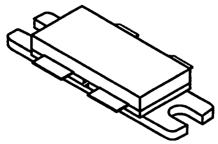
### The RF MOSFET Line
# RF Power Field-Effect Transistor
## N-Channel Enhancement-Mode MOSFET

. . . designed for broadband commercial and military applications at frequencies to 175 MHz. The high power, high gain and broadband performance of this device makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance at 175 MHz, 28 V:
  Output Power — 300 W
  Gain — 12 dB (14 dB Typ)
  Efficiency — 50%
- Low Thermal Resistance — 0.35°C/W
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability



**300 W, 28 V, 175 MHz**
**N-CHANNEL**
**BROADBAND**
**RF POWER MOSFET**



**CASE 375, STYLE 2**

**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DSS}$ | 65 | Vdc |
| Drain-Gate Voltage | $V_{DGO}$ | 65 | Vdc |
| Gate-Source Voltage | $V_{GS}$ | ±40 | Vdc |
| Drain Current — Continuous | $I_D$ | 32 | Adc |
| Total Device Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 500<br>2.85 | Watts<br>W/°C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Operating Junction Temperature | $T_J$ | 200 | °C |

**THERMAL CHARACTERISTICS**

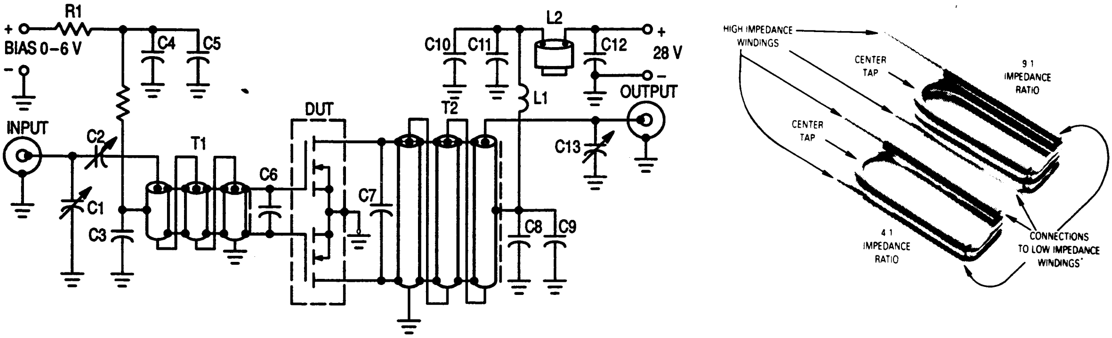
| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 0.35 | °C/W |

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** (1) | | | | | |
| Drain-Source Breakdown Voltage<br>($V_{GS}$ = 0, $I_D$ = 100 mA) | $V_{(BR)DSS}$ | 65 | — | — | Vdc |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 28 V, $V_{GS}$ = 0) | $I_{DSS}$ | — | — | 5.0 | mAdc |
| Gate-Body Leakage Current<br>($V_{GS}$ = 20 V, $V_{DS}$ = 0) | $I_{GSS}$ | — | — | 1.0 | μAdc |
| **ON CHARACTERISTICS** (1) | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = 10 V, $I_D$ = 100 mA) | $V_{GS(th)}$ | 1.0 | 3.0 | 5.0 | Vdc |
| Drain-Source On-Voltage<br>($V_{GS}$ = 10 V, $I_D$ = 10 A) | $V_{DS(on)}$ | — | — | 1.5 | Vdc |
| Forward Transconductance<br>($V_{DS}$ = 10 V, $I_D$ = 5.0 A) | $g_{fs}$ | 5.0 | 7.0 | — | mhos |
| **DYNAMIC CHARACTERISTICS** (1) | | | | | |
| Input Capacitance<br>($V_{DS}$ = 28 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{iss}$ | — | 350 | — | pF |
| Output Capacitance<br>($V_{DS}$ = 28 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{oss}$ | — | 420 | — | pF |
| Reverse Transfer Capacitance<br>($V_{DS}$ = 28 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{rss}$ | — | 40 | — | pF |
| **FUNCTIONAL TESTS** (2) | | | | | |
| Common Source Amplifier Power Gain<br>($V_{DD}$ = 28 V, $P_{out}$ = 300 W, $I_{DQ}$ = 500 mA, f = 175 MHz) | $G_{ps}$ | 12 | 14 | — | dB |
| Drain Efficiency<br>($V_{DD}$ = 28 V, $P_{out}$ = 300 W, f = 175 MHz, $I_D$ (Max) = 21.4 A) | $\eta$ | 45 | 55 | — | % |
| Load Mismatch<br>($V_{DD}$ = 28 V, $P_{out}$ = 300 W, $I_{DQ}$ = 500 mA, f = 175 MHz, VSWR 5:1 at all Phase Angles) | $\psi$ | No Degradation in Output Power | | | |

NOTES:
1. Each side measured separately.
2. Measured in push-pull configuration.



C1 — Arco 402, 1.5–20 pF
C2 — Arco 406, 15–115 pF
C3, C4, C8, C9, C10 — 1000 pF Chip
C5, C11 — 0.1 µF Chip
C6 — 330 pF Chip
C7 — 200 pF and 180 pF Chips in Parallel
C12 — 0.47 µF Ceramic Chip, Kemet 1215 or Equivalent
C13 — Arco 403, 3.0–35 pF
L1 — 10 Turns AWG #16 Enameled Wire, Close Wound, 1/4″ I.D.
L2 — Ferrite Beads of Suitable Material for 1.5–2.0 µH Total Inductance
R1 — 100 Ohms, 1/2 W
R2 — 1.0 kOhm, 1/2 W

T1 — 9:1 RF Transformer. Can be made of 15–18 Ohms Semirigid Co-Ax, 62–90 Mils O.D.
T2 — 1:9 RF Transformer. Can be made of 15–18 Ohms Semirigid Co-Ax, 70–90 Mils O.D.

Board Material — 0.062″ Fiberglass (G10), 1 oz. Copper Clad, 2 Sides, $\varepsilon_r = 5$

NOTE: For stability, the input transformer T1 must be loaded with ferrite toroids or beads to increase the common mode inductance. For operation below 100 MHz. The same is required for the output transformer.

See pictures for construction details.

Unless Otherwise Noted, All Chip Capacitors are ATC Type 100 or Equivalent.

**Figure 1. 175 MHz Test Circuit**

## TYPICAL CHARACTERISTICS

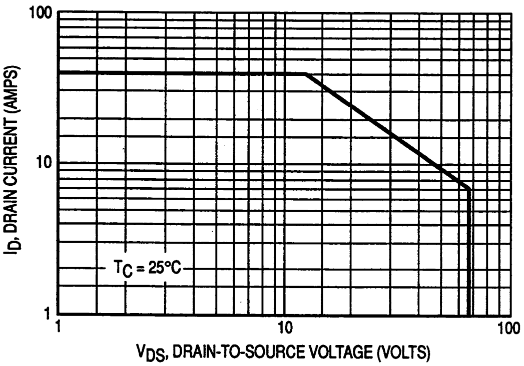


**Figure 2. DC Safe Operating Area**

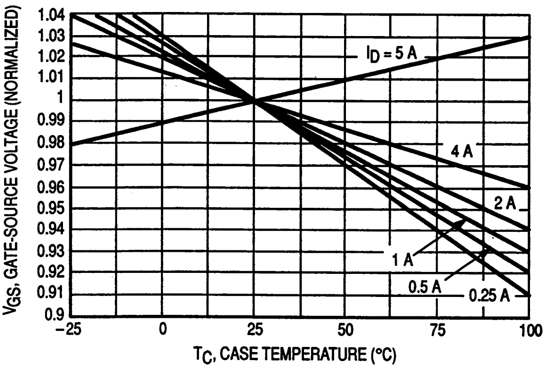
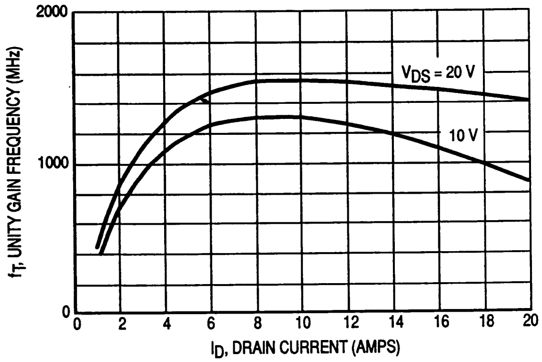


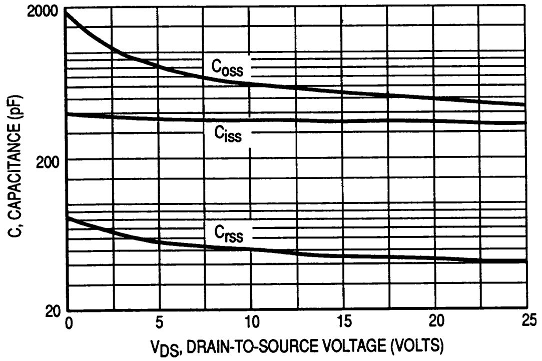
**Figure 3. Gate-Source Voltage versus Case Temperature**

## TYPICAL CHARACTERISTICS



NOTE: Data shown applies to each half of MRF141G.

**Figure 4. Common Source Unity Gain Frequency versus Drain Current**



NOTE: Data shown applies to each half of MRF141G.

**Figure 5. Capacitance versus Drain-Source Voltage**

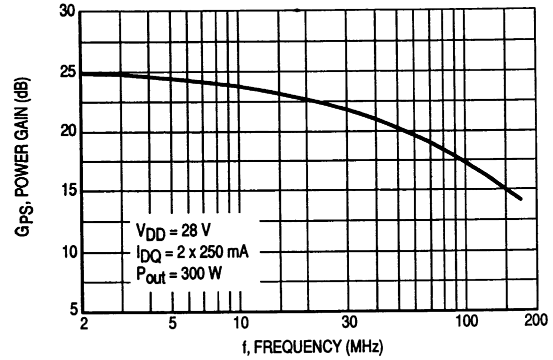


**Figure 6. Power Gain versus Frequency**

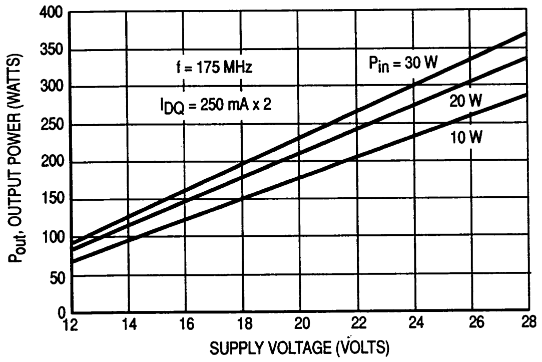
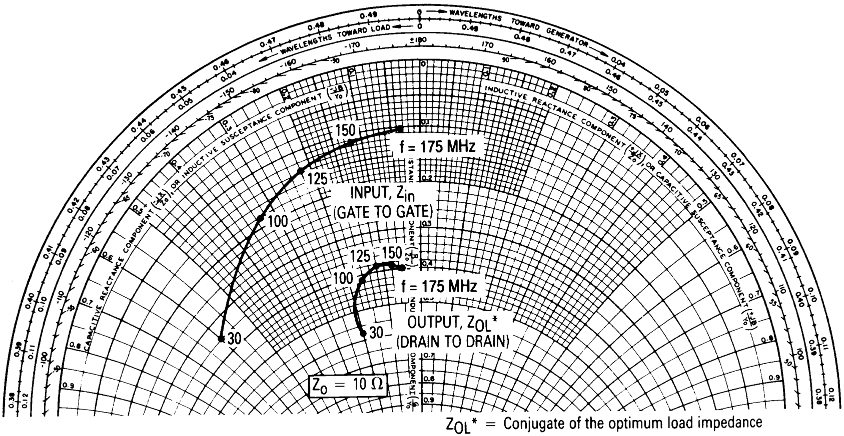


**Figure 7. Output Power versus Supply Voltage**



$Z_{OL}$* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

**Figure 8. Input and Output Impedances**

# RF POWER MOSFET CONSIDERATIONS

## MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal anode gate structure determines the capacitors from gate-to-drain ($C_{gd}$), and gate-to-source ($C_{gs}$). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain-to-source ($C_{ds}$).

These capacitances are characterized as input ($C_{iss}$), output ($C_{oss}$) and reverse transfer ($C_{rss}$) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The $C_{iss}$ can be specified in two ways:

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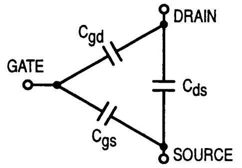
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



$C_{iss} = C_{gd} = C_{gs}$
$C_{oss} = C_{gd} = C_{ds}$
$C_{rss} = C_{gd}$

## LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 4 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to $f_T$ for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

## DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate-source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

## GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of $10^9$ ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage, $V_{GS(th)}$.

**Gate Voltage Rating** — Never exceed the gate voltage rating. Exceeding the rated $V_{GS}$ can result in permanent damage to the oxide layer in the gate region.

**Gate Termination** — The gate of this device is essentially capacitor. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage build-up on the input capacitor due to leakage currents or pickup.

**Gate Protection** — This device does not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate-to-source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

## HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with a grounded iron.

## DESIGN CONSIDERATIONS

The MRF141G is an RF Power, MOS, N-channel enhancement mode field-effect transistor (FET) designed for HF and VHF power amplifier applications.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power MOSFETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal.

## DC BIAS

The MRF141G is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current ($I_{DQ}$) is not critical for many applications. The MRF141G was characterized at $I_{DQ} = 250$ mA, each side, which is the suggested minimum value of $I_{DQ}$. For special applications such as linear amplification, $I_{DQ}$ may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias sytem.

## GAIN CONTROL

Power output of the MRF141G may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

**MOTOROLA**
**SEMICONDUCTOR**
**TECHNICAL DATA**

# MRF151

### The RF MOSFET Line

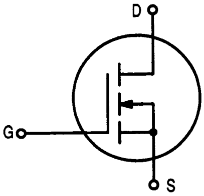
# RF Power Field-Effect Transistor

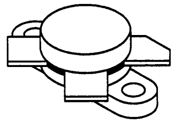
## N-Channel Enhancement-Mode MOSFET

. . . designed for broadband commercial and military applications at frequencies to 175 MHz. The high power, high gain and broadband performance of this device makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance at 30 MHz, 50 V:
  Output Power — 150 W
  Gain — 18 dB (22 dB Typ)
  Efficiency — 40%
- Typical Performance at 175 MHz, 50 V:
  Output Power — 150 W
  Gain — 13 dB
- Low Thermal Resistance
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability

**150 W, 50 V, 175 MHz**
**N-CHANNEL**
**BROADBAND**
**RF POWER MOSFET**





**CASE 211-11, STYLE 2**

**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DSS}$ | 125 | Vdc |
| Drain-Gate Voltage | $V_{DGO}$ | 125 | Vdc |
| Gate-Source Voltage | $V_{GS}$ | ±40 | Vdc |
| Drain Current — Continuous | $I_D$ | 16 | Adc |
| Total Device Dissipation @ $T_C = 25°C$<br>Derate above 25°C | $P_D$ | 300<br>1.71 | Watts<br>W/°C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Operating Junction Temperature | $T_J$ | 200 | °C |

**THERMAL CHARACTERISTICS**

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 0.6 | °C/W |

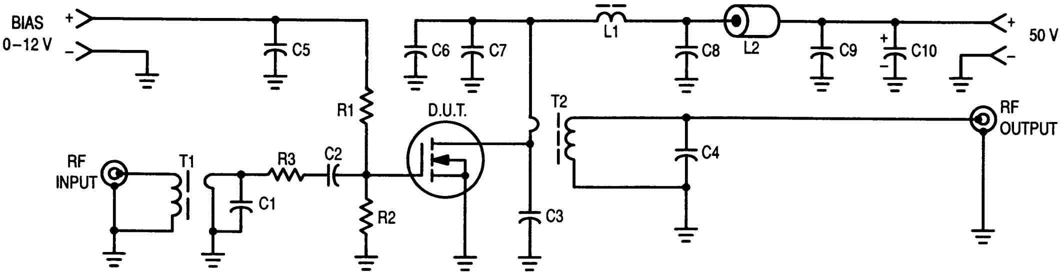
NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain-Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 100 mA) | $V_{(BR)DSS}$ | 125 | — | — | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 50 V, $V_{GS}$ = 0) | $I_{DSS}$ | — | — | 5.0 | mAdc |
| Gate-Body Leakage Current ($V_{GS}$ = 20 V, $V_{DS}$ = 0) | $I_{GSS}$ | — | — | 1.0 | µAdc |
| **ON CHARACTERISTICS** | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = 10 V, $I_D$ = 100 mA) | $V_{GS(th)}$ | 1.0 | 3.0 | 5.0 | Vdc |
| Drain-Source On-Voltage ($V_{GS}$ = 10 V, $I_D$ = 10 A) | $V_{DS(on)}$ | — | — | 5.0 | Vdc |
| Forward Transconductance ($V_{DS}$ = 10 V, $I_D$ = 5.0 A) | $g_{fs}$ | 5.0 | 7.0 | — | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance ($V_{DS}$ = 50 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{iss}$ | — | 350 | — | pF |
| Output Capacitance ($V_{DS}$ = 50 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{oss}$ | — | 225 | — | pF |
| Reverse Transfer Capacitance ($V_{DS}$ = 50 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{rss}$ | — | 20 | — | pF |
| **FUNCTIONAL TESTS** | | | | | |
| Common Source Amplifier Power Gain, f = 30; 30.001 MHz<br>($V_{DD}$ = 50 V, $P_{out}$ = 150 W (PEP), $I_{DQ}$ = 250 mA) f = 175 MHz | $G_{ps}$ | 18<br>— | 22<br>13 | —<br>— | dB |
| Drain Efficiency ($V_{DD}$ = 50 V, $P_{out}$ = 150 W (PEP), f = 30; 30.001 MHz, $I_D$ (Max) = 3.75 A) | η | 40 | 45 | — | % |
| Intermodulation Distortion (1) ($V_{DD}$ = 50 V, $P_{out}$ = 150 W (PEP), f = 30 MHz, f2 = 30.001 MHz, $I_{DQ}$ = 250 mA) | $IMD_{(d3)}$<br>$IMD_{(d11)}$ | —<br>— | −32<br>−60 | −30<br>— | dB |
| Load Mismatch ($V_{DD}$ = 50 V, $P_{out}$ = 150 W (PEP), f1 = 30; 30.001 MHz, $I_{DQ}$ = 250 mA, VSWR 30:1 at all Phase Angles) | ψ | No Degradation in Output Power | | | |
| **CLASS A PERFORMANCE** | | | | | |
| Intermodulation Distortion (1) and Power Gain ($V_{DD}$ = 50 V, $P_{out}$ = 50 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, $I_{DQ}$ = 3.0 A) | $G_{PS}$<br>$IMD_{(d3)}$<br>$IMD_{(d9-13)}$ | —<br>—<br>— | 23<br>−50<br>−75 | —<br>—<br>— | dB |

NOTE:

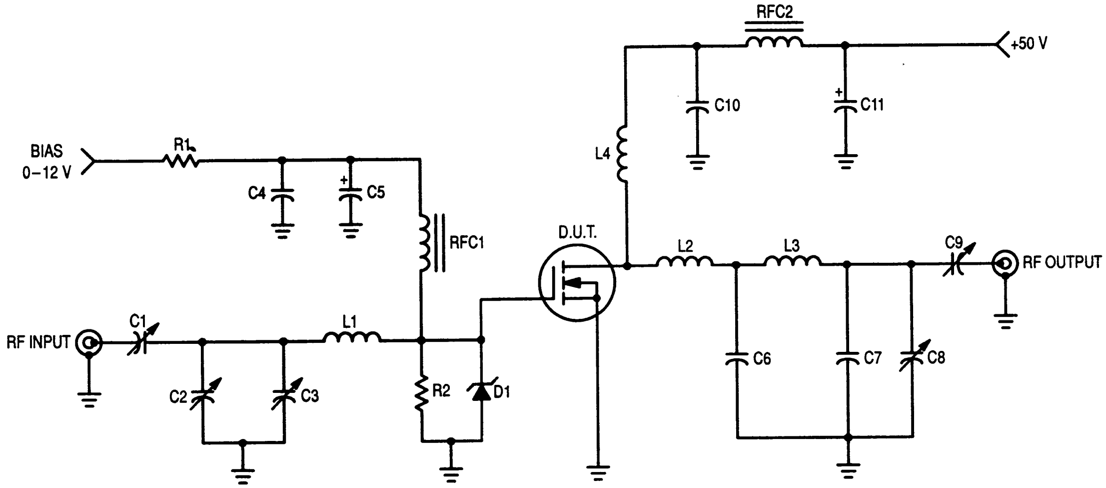
1. To MIL-STD-1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.



C1 — 470 pF Dipped Mica
C2, C5, C6, C7, C8, C9 — 0.1 µF Ceramic Chip or Monolythic with Short Leads
C3 — 200 pF Unencapsulated Mica or Dipped Mica with Short Leads
C4 — 15 pF Unencapsulated Mica or Dipped Mica with Short Leads
C10 — 10 µF/100 V Electrolytic

L1 — VK200/4B Ferrite Choke or Equivalent, 3.0 µH
L2 — Ferrite Bead(s), 2.0 µH
R1, R2 — 51 Ω/1.0 W Carbon
R3 — 3.3 Ω/1.0 W Carbon (or 2.0 x 6.8 Ω/1/2 W in Parallel)
T1 — 9:1 Broadband Transformer
T2 — 1:9 Broadband Transformer
Board Material — 0.062″ Fiberglass (G10),
1 oz. Copper Clad, 2 Sides, $\epsilon_r$ = 5

**Figure 1. 30 MHz Test Circuit**



C1, C2, C8 — Arco 463 or equivalent
C3 — 25 pF Unelco
C4 — 0.1 µF Ceramic
C5 — 1.0 µF, 15 WV Tantalum
C6 — 250 pF Unelco J101
C7 — 25 µF Unelco J101
C9 — Arco 262 or equivalent
C10 — 0.05 µF Ceramic
C11 — 15 µF, 60 WV Electrolytic

D1 — 1N5347 Zener Diode
L1 — 3/4″ #18 AWG into Hairpin
L2 — Printed Line, 0.200″ x 0.500″
L3 — 1″ #16 AWG into Hairpin
L4 — 2 Turns #16 AWG, 5/16 ID
RFC1 — 5.6 µH Choke
RFC2 — VK200-4B
R1, R2 — 150 Ω, 1.0 W Carbon
Board Material — 0.062″ Fiberglass (G10),
1 oz. Copper Clad, 2 Sides, $\varepsilon_r = 5.0$

**Figure 2. 175 MHz Test Circuit**

## TYPICAL CHARACTERISTICS

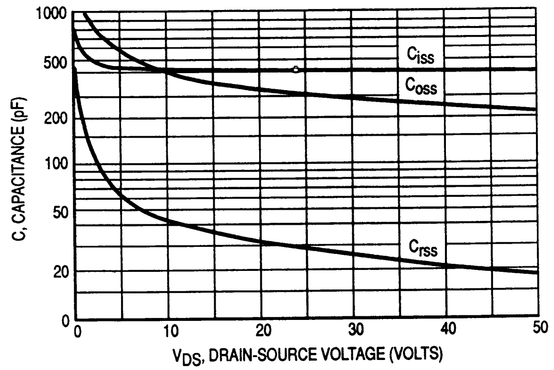


**Figure 3. Capacitance versus Drain-Source Voltage**

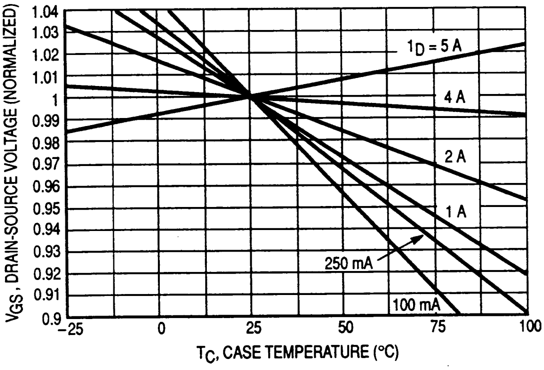


**Figure 4. Gate-Source Voltage versus Case Temperature**

## TYPICAL CHARACTERISTICS

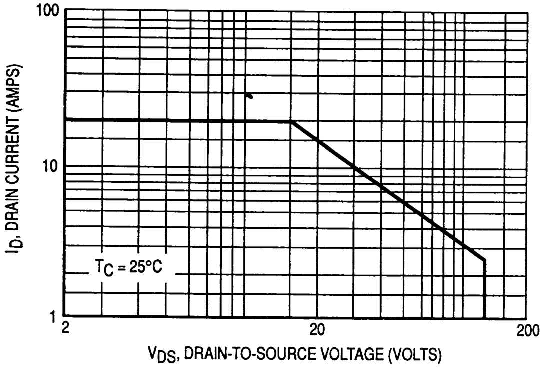


Figure 5. DC Safe Operating Area

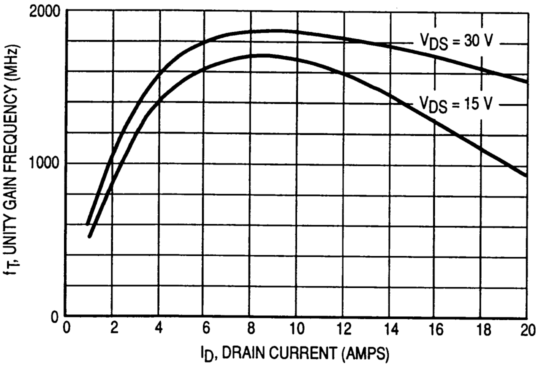


Figure 6. Common Source Unity Gain Frequency versus Drain Current

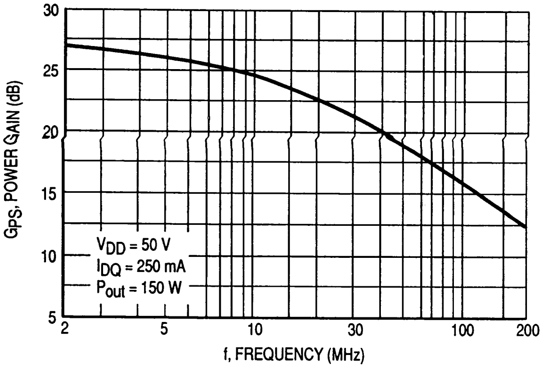


Figure 7. Power Gain versus Frequency

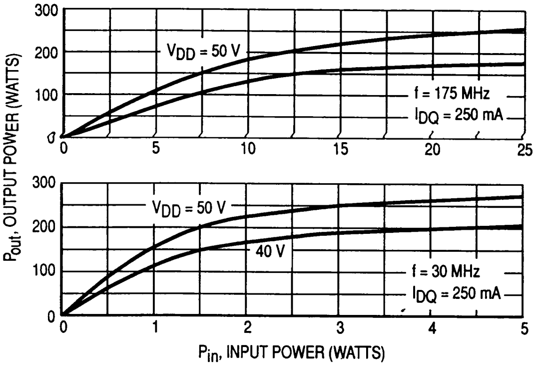


Figure 8. Output Power versus Input Power

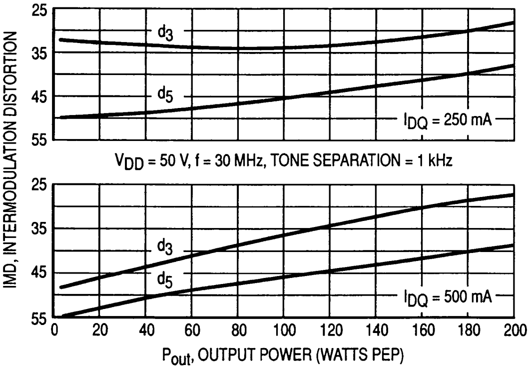
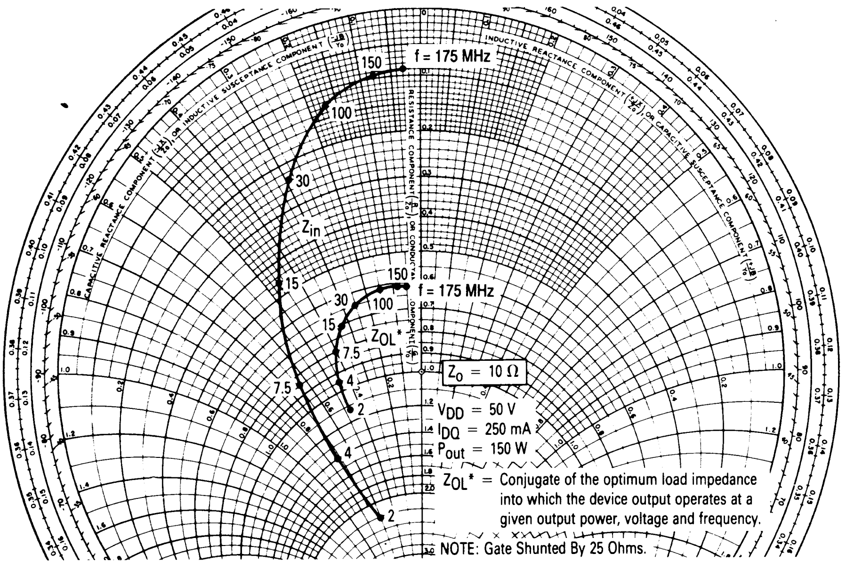


Figure 9. IMD versus $P_{out}$

## TYPICAL CHARACTERISTICS



$V_{DD}$ = 50 V
$I_{DQ}$ = 250 mA
$P_{out}$ = 150 W

$Z_{OL}$* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

NOTE: Gate Shunted By 25 Ohms.

Figure 10. Series Equivalent Impedance

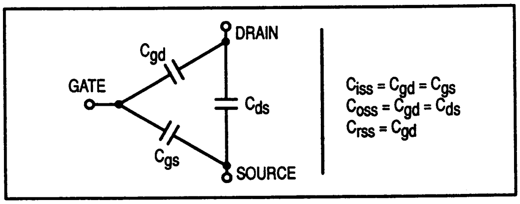
## RF POWER MOSFET CONSIDERATIONS

### MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal anode gate structure determines the capacitors from gate-to-drain ($C_{gd}$), and gate-to-source ($C_{gs}$). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain-to-source ($C_{ds}$).

These capacitances are characterized as input ($C_{iss}$), output ($C_{oss}$) and reverse transfer ($C_{rss}$) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The $C_{iss}$ can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



$C_{iss} = C_{gd} = C_{gs}$
$C_{oss} = C_{gd} = C_{ds}$
$C_{rss} = C_{gd}$

### LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 6 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to $f_T$ for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

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### GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of $10^9$ ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage, $V_{GS(th)}$.

**Gate Voltage Rating** — Never exceed the gate voltage rating. Exceeding the rated $V_{GS}$ can result in permanent damage to the oxide layer in the gate region.

**Gate Termination** — The gate of this device is essentially capacitor. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage build-up on the input capacitor due to leakage currents or pickup.

**Gate Protection** — This device does not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate-to-source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

## HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with a grounded iron.

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The MRF151 is an RF Power, MOS, N-channel enhancement mode field-effect transistor (FET) designed for HF and VHF power amplifier applications.

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## DC BIAS

The MRF151 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current ($I_{DQ}$) is not critical for many applications. The MRF151 was characterized at $I_{DQ}$ = 250 mA, each side, which is the suggested minimum value of $I_{DQ}$. For special applications such as linear amplification, $I_{DQ}$ may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias sytem.

## GAIN CONTROL

Power output of the MRF151 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

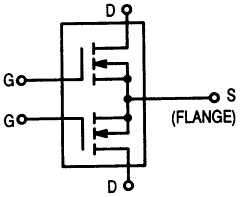
**MRF151G**

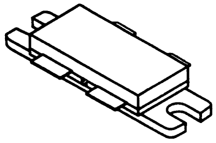
### The RF MOSFET Line
# RF Power Field-Effect Transistor
## N-Channel Enhancement-Mode MOSFET

. . . designed for broadband commercial and military applications at frequencies to 175 MHz. The high power, high gain and broadband performance of this device makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance at 175 MHz, 50 V:
  Output Power — 300 W
  Gain — 14 dB (16 dB Typ)
  Efficiency — 50%
- Low Thermal Resistance — 0.35°C/W
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability

**300 W, 50 V, 175 MHz
N-CHANNEL
BROADBAND
RF POWER MOSFET**





CASE 375, STYLE 2

**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DSS}$ | 125 | Vdc |
| Drain-Gate Voltage | $V_{DGO}$ | 125 | Vdc |
| Gate-Source Voltage | $V_{GS}$ | ±40 | Vdc |
| Drain Current — Continuous | $I_D$ | 40 | Adc |
| Total Device Dissipation @ $T_C = 25°C$<br>Derate above 25°C | $P_D$ | 500<br>2.85 | Watts<br>W/°C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Operating Junction Temperature | $T_J$ | 200 | °C |

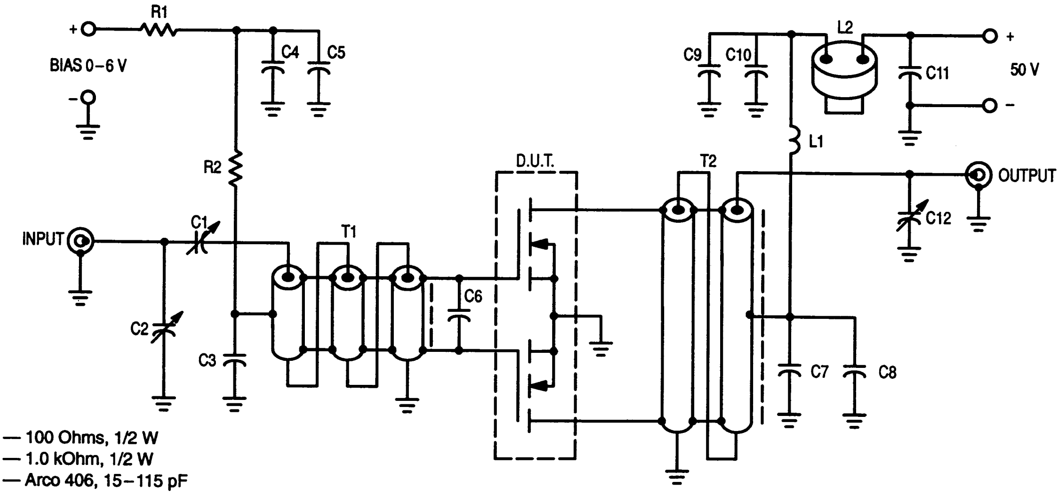
**THERMAL CHARACTERISTICS**

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 0.35 | °C/W |

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS (Each Side)** | | | | | |
| Drain-Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 100 mA) | $V_{(BR)DSS}$ | 125 | — | — | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 50 V, $V_{GS}$ = 0) | $I_{DSS}$ | — | — | 5.0 | mAdc |
| Gate-Body Leakage Current ($V_{GS}$ = 20 V, $V_{DS}$ = 0) | $I_{GSS}$ | — | — | 1.0 | µAdc |
| **ON CHARACTERISTICS (Each Side)** | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = 10 V, $I_D$ = 100 mA) | $V_{GS(th)}$ | 1.0 | 3.0 | 5.0 | Vdc |
| Drain-Source On-Voltage ($V_{GS}$ = 10 V, $I_D$ = 10 A) | $V_{DS(on)}$ | — | — | 5.0 | Vdc |
| Forward Transconductance ($V_{DS}$ = 10 V, $I_D$ = 5.0 A) | $g_{fs}$ | 5.0 | 7.0 | — | mhos |
| **DYNAMIC CHARACTERISTICS (Each Side)** | | | | | |
| Input Capacitance ($V_{DS}$ = 50 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{iss}$ | — | 350 | — | pF |
| Output Capacitance ($V_{DS}$ = 50 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{oss}$ | — | 225 | — | pF |
| Reverse Transfer Capacitance ($V_{DS}$ = 50 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{rss}$ | — | 20 | — | pF |
| **FUNCTIONAL TESTS** | | | | | |
| Common Source Amplifier Power Gain ($V_{DD}$ = 50 V, $P_{out}$ = 300 W, $I_{DQ}$ = 500 mA, f = 175 MHz) | $G_{ps}$ | 14 | 16 | — | dB |
| Drain Efficiency ($V_{DD}$ = 50 V, $P_{out}$ = 300 W, f = 175 MHz, $I_D$ (Max) = 11 A) | $\eta$ | 50 | 55 | — | % |
| Load Mismatch ($V_{DD}$ = 50 V, $P_{out}$ = 300 W, $I_{DQ}$ = 500 mA, VSWR 5:1 at all Phase Angles) | $\psi$ | No Degradation in Output Power | | | |



R1 — 100 Ohms, 1/2 W
R2 — 1.0 kOhm, 1/2 W
C1 — Arco 406, 15–115 pF
C2 — Arco 402, 1.5–20 pF
C3, C4, C7, C8, C9 — 1000 pF Chip
C5, C10 — 0.1 µF Chip
C6 — 330 pF Chip
C11 — 0.47 µF Ceramic Chip, Kemet 1215 or Equivalent (100 V)
C12 — Arco 403, 3.0–35 pF
L1 — 10 Turns AWG #16 Enameled Wire, Close Wound, 1/4″ I.D.
L2 — Ferrite Beads of Suitable Material for 1.5–2.0 µH Total Inductance

Unless Otherwise Noted, All Chip Capacitors are ATC Type 100 or Equivalent.

T1 — 9:1 RF Transformer. Can be made of 15–18 Ohms Semirigid Co-Ax, 62–90 Mils O.D.
T2 — 1:4 RF Transformer. Can be made of 15–18 Ohms Semirigid Co-Ax, 70–90 Mils O.D.
Board Material — 0.062″ Fiberglass (G10), 1 oz. Copper Clad, 2 Sides, $\varepsilon_r$ = 5.0

NOTE: For stability, the input transformer T1 must be loaded with ferrite toroids or beads to increase the common mode inductance. For operation below 100 MHz. The same is required for the output transformer.

See Figure 6 for construction details of T1 and T2.

**Figure 1. 175 MHz Test Circuit**

## TYPICAL CHARACTERISTICS

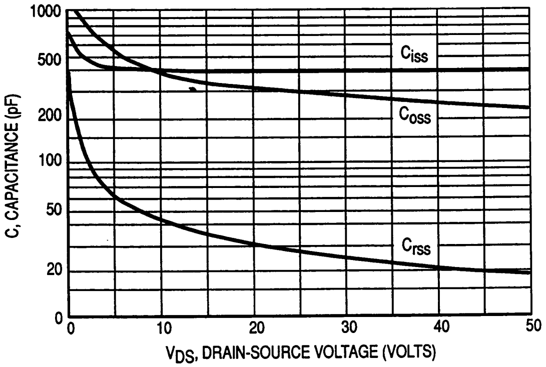


**Figure 2. Capacitance versus Drain-Source Voltage***

*Data shown applies to each half of MRF151G.

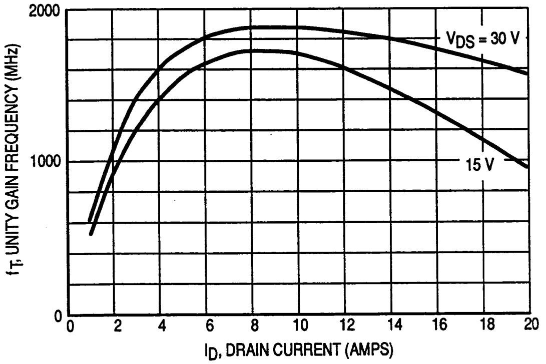


**Figure 3. Common Source Unity Gain Frequency versus Drain Current***

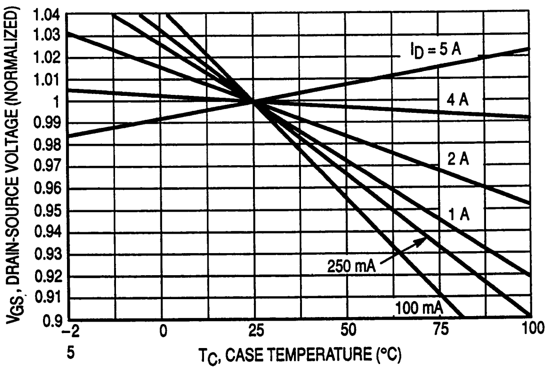


**Figure 4. Gate-Source Voltage versus Case Temperature***

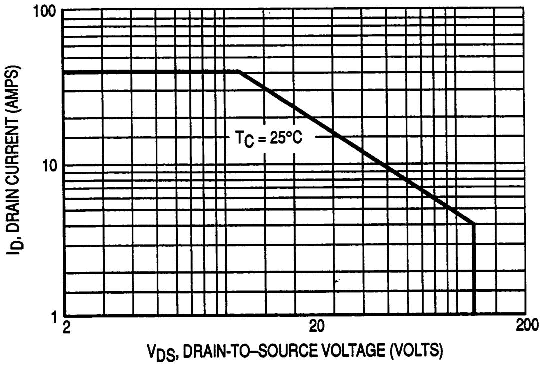


**Figure 5. DC Safe Operating Area**

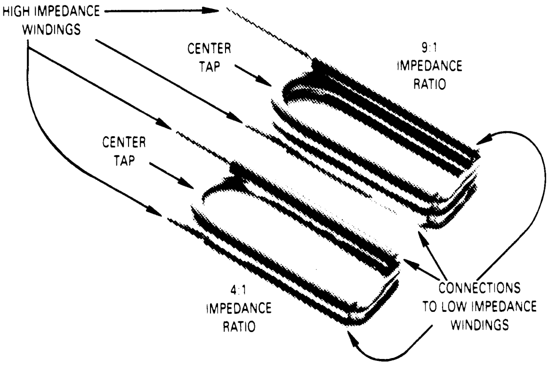


**Figure 6. RF Transformer**

## TYPICAL CHARACTERISTICS

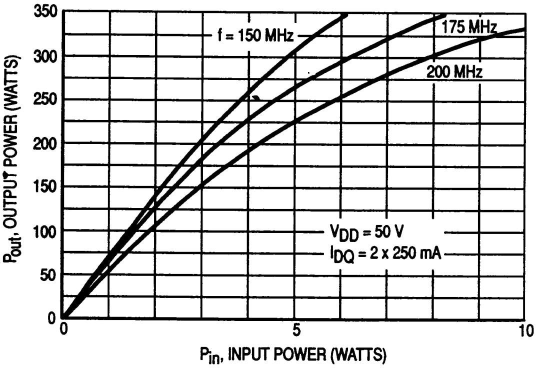


Figure 7. Output Power versus Input Power

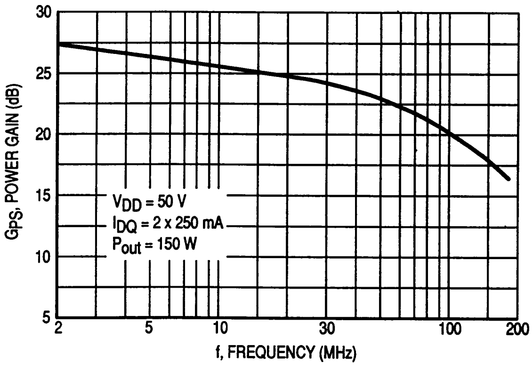
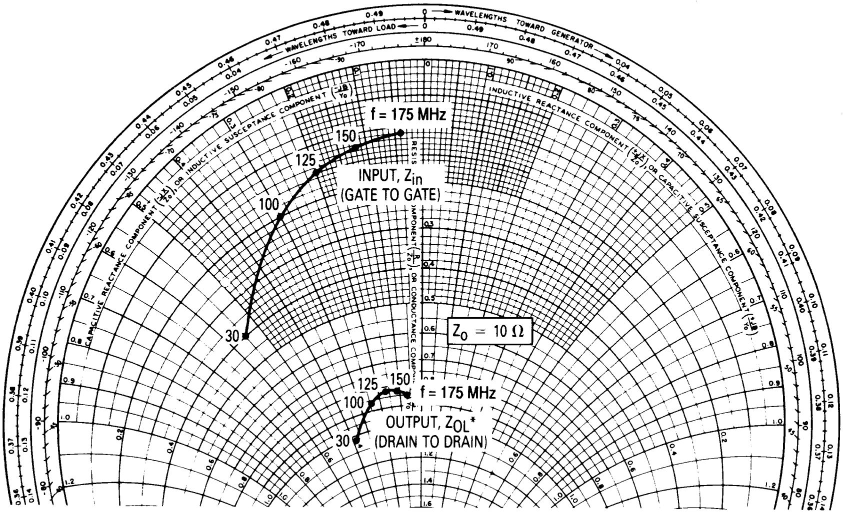


Figure 8. Power Gain versus Frequency



ZOL* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 9. Input and Output Impedance

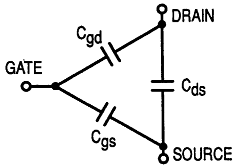
# RF POWER MOSFET CONSIDERATIONS

## MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal anode gate structure determines the capacitors from gate-to-drain ($C_{gd}$), and gate-to-source ($C_{gs}$). The PN junction formed during the fabrication of the RF MOSFET results in a junction capacitance from drain-to-source ($C_{ds}$).

These capacitances are characterized as input ($C_{iss}$), output ($C_{oss}$) and reverse transfer ($C_{rss}$) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The $C_{iss}$ can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



$C_{iss} = C_{gd} = C_{gs}$
$C_{oss} = C_{gd} = C_{ds}$
$C_{rss} = C_{gd}$

## LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 3 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to $f_T$ for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

## DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate-source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

## GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of $10^9$ ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage, $V_{GS(th)}$.

**Gate Voltage Rating** — Never exceed the gate voltage rating. Exceeding the rated $V_{GS}$ can result in permanent damage to the oxide layer in the gate region.

**Gate Termination** — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

**Gate Protection** — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate-to-source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

## HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with a grounded iron.

## DESIGN CONSIDERATIONS

The MRF151G is an RF Power, MOS, N-channel enhancement mode field-effect transistor (FET) designed for HF and VHF power amplifier applications.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power MOSFETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal.

## DC BIAS

The MRF151G is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current ($I_{DQ}$) is not critical for many applications. The MRF151G was characterized at $I_{DQ}$ = 250 mA, each side, which is the suggested minimum value of $I_{DQ}$. For special applications such as linear amplification, $I_{DQ}$ may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias sytem.

## GAIN CONTROL

Power output of the MRF151G may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.