MRF157

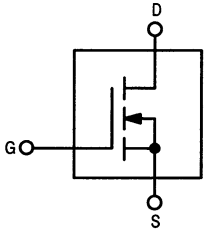
Motorola Preferred Device

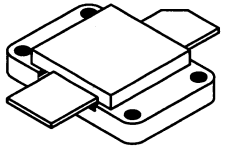
The RF Power MOS Line
Power Field Effect Transistor
N-Channel Enhancement Mode

Designed primarily for linear large-signal output stages to 80 MHz.

- Specified 50 Volts, 30 MHz Characteristics
  - Output Power = 600 Watts
  - Power Gain = 21 dB (Typ)
  - Efficiency = 45% (Typ)

600 W, to 80 MHz
MOS LINEAR
RF POWER FET





CASE 368, STYLE 2

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	125	Vdc
Drain-Gate Voltage	V_{DGO}	125	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	60	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1350 7.7	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

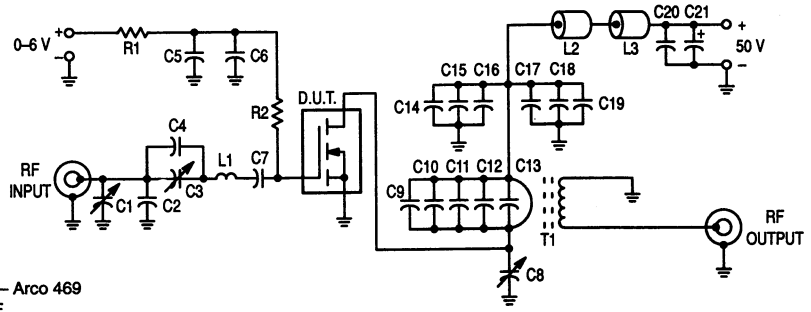
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.13	°C/W

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)	I_{DSS}	—	—	20	mAdc
Gate-Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	5.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V, I_D = 40 A)	$V_{DS(on)}$	—	—	5.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 20 A)	g_{fs}	16	24	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	—	1800	—	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	750	—	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	75	—	pF
FUNCTIONAL TESTS					
Common Source Amplifier Power Gain (V_{DD} = 50 V, P_{out} = 600 W, I_{DQ} = 800 mA, f = 30 MHz)	G_{ps}	15	21	—	dB
Drain Efficiency (V_{DD} = 50 V, P_{out} = 600 W, f = 30 MHz, I_{DQ} = 800 mA)	h	40	45	—	%
Intermodulation Distortion (V_{DD} = 50 V, P_{out} = 600 W(PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 800 mA)	$IMD_{(d3)}$	—	−25	—	dB



C1, C3, C8 — Arco 469
C2 — 330 pF
C4 — 680 pF
C5, C19, C20 — 0.47 μF, RMC Type 2225C
C6, C7, C14, C15, C16 — 0.1 μF
C9, C10, C11 — 470 pF
C12 — 1000 pF
C13 — Two Unencapsulated 1000 pF Mica, in Series
C17, C18 — 0.039 μF
C21 — 10 μF/100 V Electrolytic
L1 — 2 Turns #16 AWG, 1/2″ ID, 3/8″ Long
L2, L3 — Ferrite Beads, Fair-Rite Products Corp. #2673000801

R1, R2 — 10 Ohms/2W Carbon
T1 — RF Transformer, 1:25 Impedance Ratio. See Motorola Application Note AN749, Figure 4 for details. Ferrite Material: 2 Each, Fair-Rite Products Corp. #2667540001

All capacitors ATC type 100/200 chips or equivalent unless otherwise noted.

Figure 1. 30 MHz Test Circuit

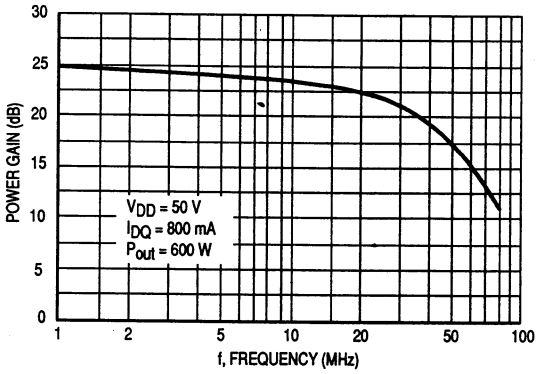


Figure 2. Power Gain versus Frequency

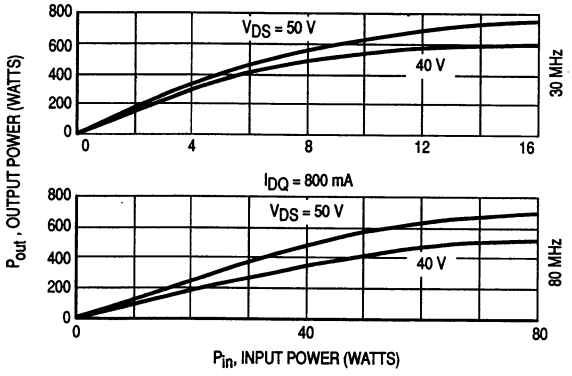


Figure 3. Output Power versus Input Power

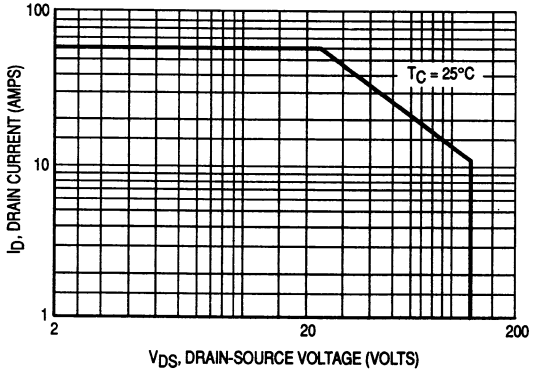


Figure 4. DC Safe Operating Area

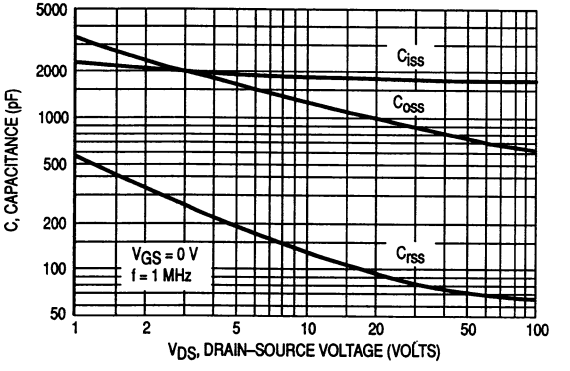


Figure 5. Capacitance versus Drain Voltage

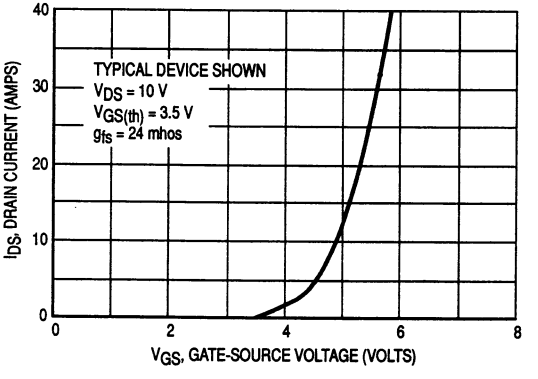


Figure 6. Gate Voltage versus Drain Current

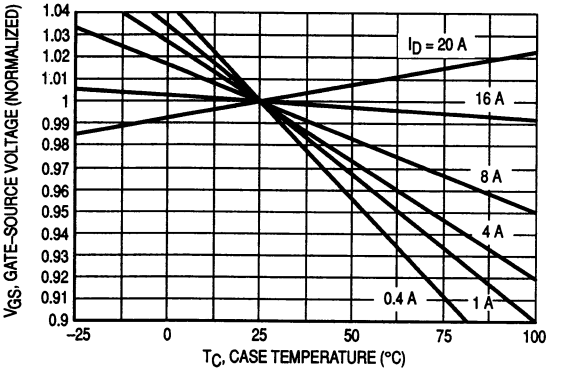


Figure 7. Gate-Source Voltage versus Case Temperature

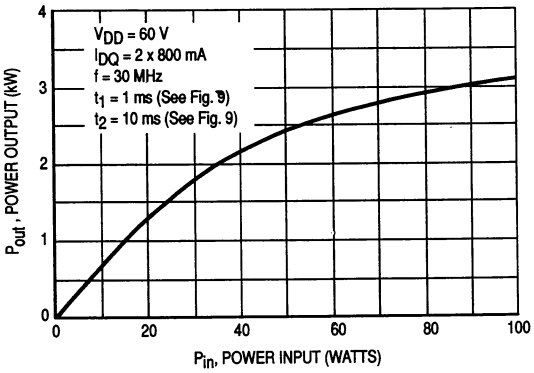


Figure 8. Output Power versus Input Power Under Pulse Conditions (2 x MRF157)

Note: Pulse data for this graph was taken in a push-pull circuit similar to the one shown. However, the output matching network was modified for the higher level of peak power.

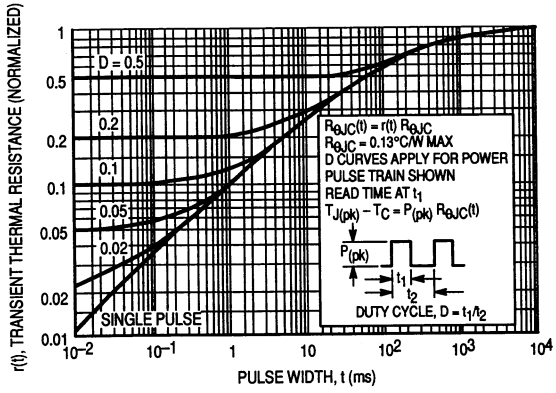
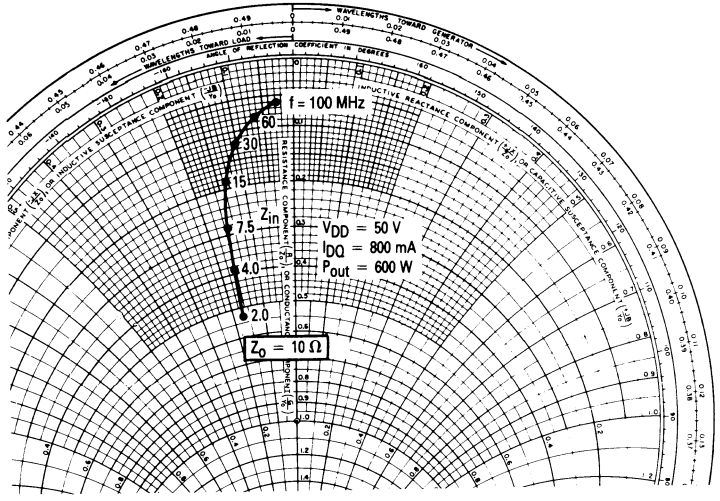


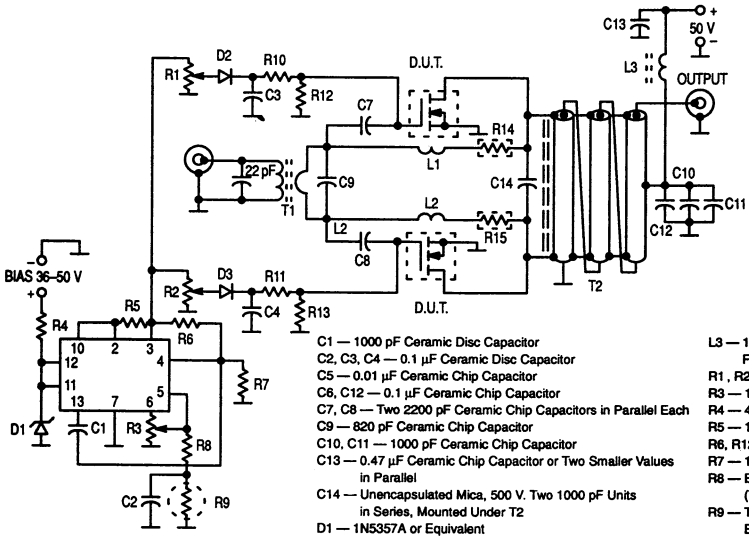
Figure 9. Thermal Response versus Pulse Width

2



Note: To determine Z_{OL}^*, use formula $\frac{(V_{CC} - V_{sat})^2}{2\ P_o} = Z_{OL}^*$

Figure 10. Series Equivalent Impedance



C1 — 1000 pF Ceramic Disc Capacitor
C2, C3, C4 — 0.1 µF Ceramic Disc Capacitor
C5 — 0.01 µF Ceramic Chip Capacitor
C6, C12 — 0.1 µF Ceramic Chip Capacitor
C7, C8 — Two 2200 pF Ceramic Chip Capacitors in Parallel Each
C9 — 820 pF Ceramic Chip Capacitor
C10, C11 — 1000 pF Ceramic Chip Capacitor
C13 — 0.47 µF Ceramic Chip Capacitor or Two Smaller Values in Parallel
C14 — Unencapsulated Mica, 500 V. Two 1000 pF Units in Series, Mounted Under T2
D1 — 1N5357A or Equivalent
D2, D3 — 1N4148 or Equivalent.
IC1 — MC1723 (723) Voltage Regulator
L1, L2 — 15 nH, Connecting Wires to R14 and R15, 2.5 cm Each #20 AWG
L3 — 10 µH, 10 Turns #12 AWG Enameled Wire on Fair-Rite Products Corp. Ferrite Toroid #5961000401 or Equivalent
R1, R2 — 1.0K Single Turn Trimpots
R3 — 10K Single Turn Trimpot
R4 — 470 Ohms, 2.0 Watts
R5 — 10 Ohms
R6, R12, R13 — 2.0K Ohms
R7 — 10K Ohms
R8 — Exact Value Depends on Thermistor R9 used (Typically 5.0 – 10K)
R9 — Thermistor, Keystone RL1009-5820-97-D1 or Equivalent
R10, R11 — 100 Ohms, 1.0W Carbon
R14, R15 — EMC Technology Model 5308 or KDI Pyrofilm PPR 870-150-3 Power Resistors, 25 Ohms
T1, T2 — 9:1 and 1:9 Impedance Ratio RF Transformers

Unless otherwise noted, all resistors are 1/2 watt metal film type. All chip capacitors except C13 are ATC type 100/200B or Dielectric Laboratories type C17.

Figure 11. 2.0 to 50 MHz, 1.0 kW Wideband Amplifier

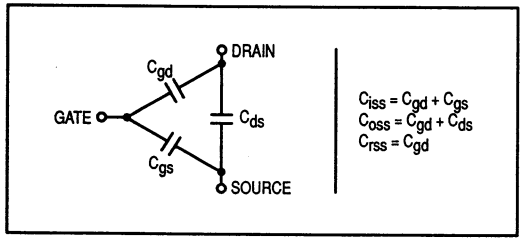
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during the fabrication of the TMOS® FET results in a junction capacitance from drain-to-source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the interterminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate-source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the TMOS FET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

IMPEDANCE CHARACTERISTICS

Device input and output impedances are normally obtained by measuring their conjugates in an optimized narrow band test circuit. These test circuits are designed and constructed for a number of frequency points depending on the frequency coverage of characterization. For low frequencies the circuits consist of standard LC matching networks including variable capacitors for peak tuning. At increasing power levels the output impedance decreases, resulting in higher RF currents in the matching network. This makes the practicality of output impedance measurements in the manner described questionable at power levels higher than 200–300 W for devices operated at 50 V and 150–200 W for devices operated at 28 V. The physical sizes and values required for the components to withstand the RF currents increase to a point where physical construction of the output matching network gets difficult if not impossible. For this reason the output impedances are not given for high power devices such as the MRF154 and MRF157. However, formulas like $\frac{(V_{DS} - V_{sat})^2}{2P_{out}}$ for a single ended design or $\frac{2((V_{DS} - V_{sat})^2)}{P_{out}}$ for a push-pull design can be used to obtain reasonably close approximations to actual values.

MOUNTING OF HIGH POWER RF POWER TRANSISTORS

The package of this device is designed for conduction cooling. It is extremely important to minimize the thermal resistance between the device flange and the heat dissipator.

If a copper heatsink is not used, a copper head spreader is strongly recommended between the device mounting surfaces and the main heatsink. It should be at least 1/4″ thick and extend at least one inch from the flange edges. A thin layer of thermal compound in all interfaces is, of course, essential. The recommended torque on the 4–40 mounting screws should be in the area of 4–5 lbs.-inch, and spring type lock washers along with flat washers are recommended.

For die temperature calculations, the Δ temperature from a corner mounting screw area to the bottom center of the flange is approximately 5°C and 10°C under normal operating conditions (dissipation 150 W and 300 W respectively).

The main heat dissipator must be sufficiently large and have low R_θ for moderate air velocity, unless liquid cooling is employed.

CIRCUIT CONSIDERATIONS

At high power levels (500 W and up), the circuit layout becomes critical due to the low impedance levels and high RF currents associated with the output matching. Some of the components, such as capacitors and inductors must also withstand these currents. The component losses are directly proportional to the operating frequency. The manufacturers specifications on capacitor ratings should be consulted on these aspects prior to design.

Push-pull circuits are less critical in general, since the ground referenced RF loops are practically eliminated, and the impedance levels are higher for a given power output. High power broadband transformers are also easier to design than comparable LC matching networks.

EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
V_{CBO}	V_{DGO}
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{fe}	g_{fs}
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$	$R_{DS(on)} = \frac{V_{DS(on)}}{I_D}$

MRF158
MRF158R

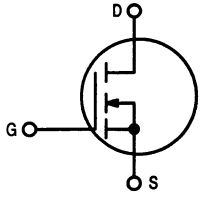
Motorola Preferred Devices

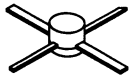
The RF TMOS® Line
Power Field Effect Transistor
N-Channel Enhancement Mode

Designed for wideband large-signal amplifier and oscillator applications to 500 MHz.

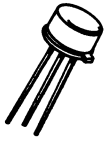
- Guaranteed 28 Volt, 400 MHz Performance
  Output Power = 2.0 Watts
  Minimum Gain = 16 dB
  Efficiency = 55% (Typical)
- Grounded Source Package for High Gain and Excellent Heat Dissipation (MRF158R)
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 100% Tested for Load Mismatch at All Phase Angles with 30:1 VSWR
- Excellent Thermal Stability, Ideally Suited for Class A Operation

2.0 W, to 500 MHz
TMOS
BROADBAND
RF POWER FET





CASE 305A, STYLE 2



CASE 79-05, STYLE 7

2

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	65	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)		V_{DGR}	65	Vdc
Gate-Source Voltage		V_{GS}	±40	Vdc
Drain Current — Continuous		I_D	0.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C		P_D	8.0 45	Watts mW/°C
Storage Temperature Range	MRF158 MRF158R	T_{stg}	−65 to +150 −65 to +200	°C
Operating Junction Temperature		T_J	200	°C

THERMAL CHARACTERISTICS

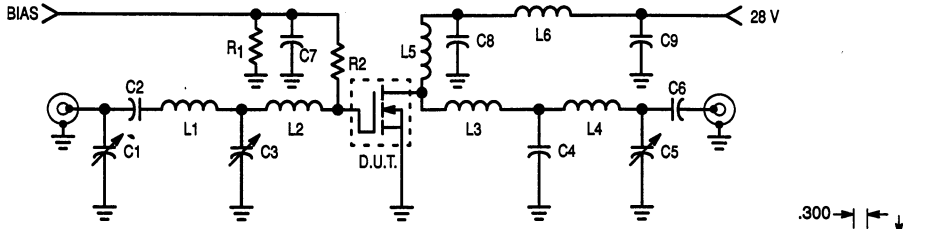
Characteristic		Symbol	Max	Unit
Thermal Resistance, Junction to Case	MRF158 MRF158R	$R_{\theta JC}$	13.2 22	°C/W

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

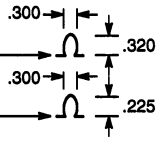
Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

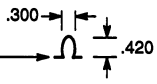
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	0.5	mAdc
Gate-Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (I_D = 10 mA, V_{DS} = 10 V)	$V_{GS(th)}$	1.0	4.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 100 mA)	g_{fs}	50	85	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	3.0	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	4.2	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	0.45	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 1)					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 2.0 W, f = 400 MHz, I_{DQ} = 100 mA)	G_{ps}	16	20	—	dB
Drain Efficiency (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 2.0 W, f = 400 MHz, I_{DQ} = 100 mA)	η	45	55	—	%
Electrical Ruggedness (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 2.0 W, f = 400 MHz, I_{DQ} = 100 mA, VSWR 30:1 at all Phase Angles)	Ψ	No Degradation in Output Power			
MRF158 Series Equivalent Input Impedance (V_{DD} = 28 V, P_{out} = 2.0 W, f = 400 MHz, I_{DQ} = 100 mA)	Z_{in}	—	8.8 – j27.37	—	Ohms
Series Equivalent Output Impedance (V_{DD} = 28 V, P_{out} = 2.0 W, f = 400 MHz, I_{DQ} = 100 mA)	Z_{out}	—	16.96 – j62	—	Ohms



C1, C3, C5 — 0.8–10 pF Piston Trimmer Capacitor
C2, C6 — 270 pF Chip Capacitor
C4 — 8.0 pF Mini-Unelco Capacitor
C7, C8 — 0.01 μF Ceramic Capacitor
C9 — 25 μF 50 V Tantalum Capacitor

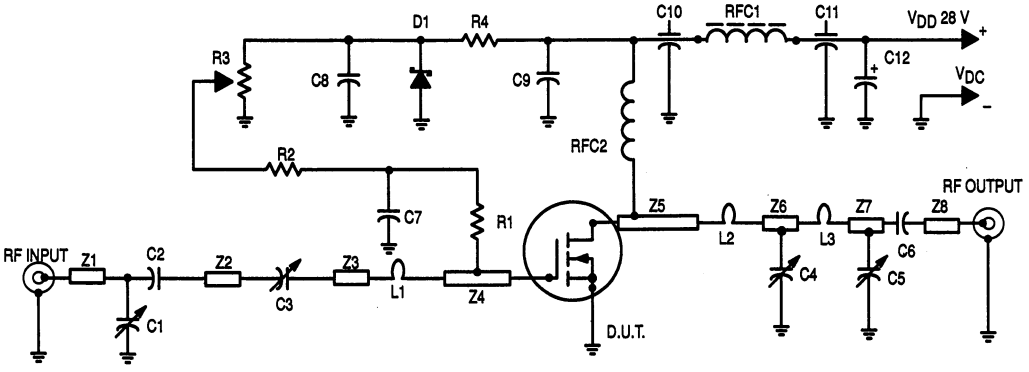


L1 — Hairpin Inductor #20 W
L2 — Hairpin Inductor #20 W
L3 — Two Turns #18 W 1/4″ ID



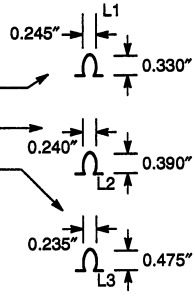
L4 — Hairpin Inductor #18 W
L5 — 8 Turns #18 W .380″ ID
L6 — VK200/10/3B Ferroxcube Choke
R1 — 1.0 kΩ 1/4 W Resistor
R2 — 10 kΩ 1/4 W Resistor
Board Material — 0.060″ Teflon Fiberglass $\epsilon_r = 2.55$
Copper Clad both sides 2 oz. copper

Figure 1. 400 MHz Test Circuit, MRF158R



C1, C4, C5 — Johanson Trimmer Capacitor, 2–20 pF
C2, C6 — 270 pF Chip Capacitor
C3 — Arco 404
C7, C8, C9 — 0.1 μF
C10, C11 — 680 pF Feed Through
C12 — 50 μF, 50 V
D1 — 1N5925A Motorola Zener
L1 — #18 AWG, Hairpin 0.825″ long, bend into hairpin
L2 — #18 AWG, Hairpin 0.875″ long, bend into hairpin
L3 — #18 AWG, Hairpin 0.965″ long, bend into hairpin

Board Material — 0.062″, Teflon Fiberglass, 2 oz., Copper clad both sides, $\epsilon_r = 2.55$



R1 — 91 Ω 1/2 Watt
R2 — 10 kΩ 1/2 Watt
R3 — 10 kΩ, 10 Turns Bourns
R4 — 1.8 k 1.4 Watt
RFC1 — Ferroxcube VK200-19/4B
RFC2 — 10 Turns #20 AWG Enameled, 0.250″ ID
Z1 — Microstrip Line 0.150″ wide, 0.420″ long
Z2 — Microstrip Line 0.150″ wide, 0.420″ long
Z3 — Microstrip Line 0.150″ wide, 0.475″ long
Z4 — Microstrip Line 0.150″ wide, 0.825″ long
Z5 — Microstrip Line 0.150″ wide, 0.750″ long
Z6 — Microstrip Line 0.150″ wide, 0.500″ long
Z7 — Microstrip Line 0.150″ wide, 0.500″ long
Z8 — Microstrip Line 0.150″ wide, 0.450″ long

Figure 2. 400 MHz Test Circuit, MRF158

TYPICAL CHARACTERISTICS

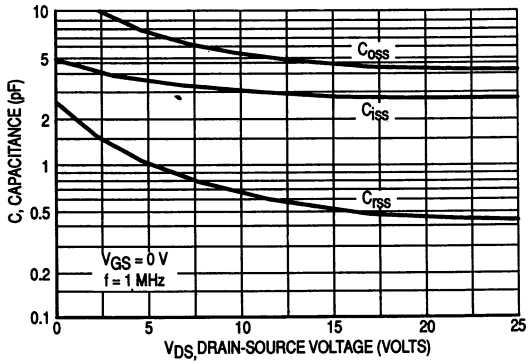


Figure 3. Capacitance versus Drain-Source Voltage

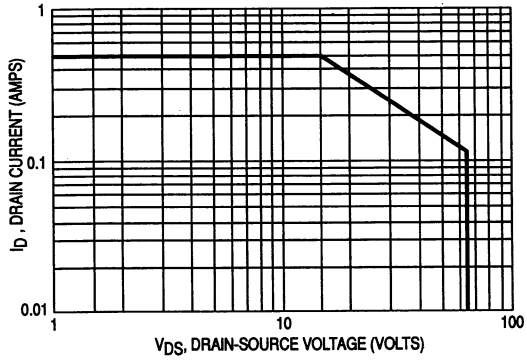


Figure 4. DC Safe Operating Area

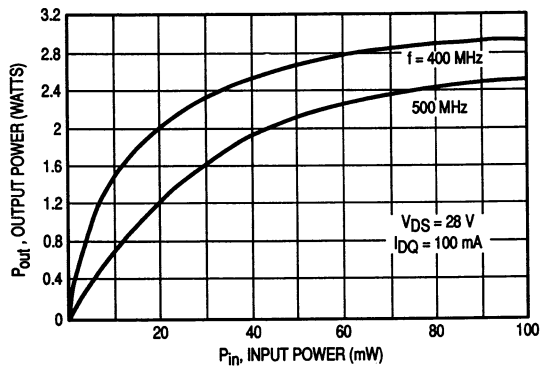


Figure 5. Output Power versus Input Power

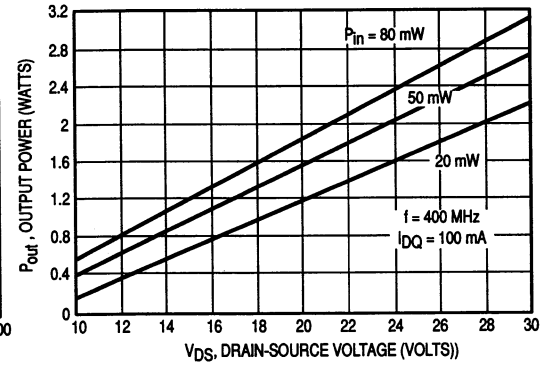


Figure 6. Output Power versus Voltage

MRF158R ONLY

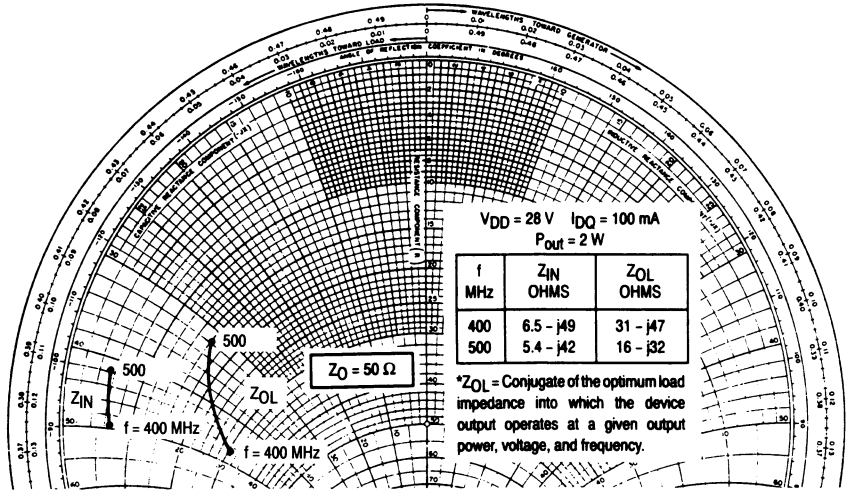


Figure 7. Series Equivalent Input and Output Impedances

Table 1. Typical Common Emitter S-Parameters (MRF158R)

V_{DS} (Volts)	I_D (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
28	100	5	1.00	−3.0	6.47	178	0.003	54	0.95	−3.0
		10	1.00	−3.0	5.95	176	0.003	83	0.95	−2.0
		20	1.00	−5.0	5.87	174	0.006	76	0.95	−4.0
		30	0.99	−8.0	5.86	171	0.009	82	0.95	−6.0
		40	0.99	−10	5.77	168	0.011	81	0.95	−8.0
		50	0.98	−12	5.71	165	0.014	77	0.95	−10
		100	0.95	−24	5.42	153	0.026	68	0.92	−20
		150	0.89	−34	5.07	141	0.034	61	0.89	−28
		200	0.83	−43	4.64	131	0.039	55	0.85	−36
		250	0.78	−51	4.26	121	0.040	51	0.80	−43
		300	0.73	−59	3.87	112	0.039	50	0.77	−48
		350	0.68	−65	3.55	104	0.036	53	0.73	−53
		400	0.64	−71	3.22	97	0.033	63	0.70	−58
		500	0.58	−82	2.77	84	0.037	96	0.64	−69
		600	0.54	−94	2.42	72	0.064	115	0.62	−79
		700	0.54	−107	2.19	63	0.100	117	0.62	−91
		800	0.54	−118	1.99	53	0.147	117	0.64	−101
		900	0.55	−129	1.81	45	0.209	112	0.64	−112
		1000	0.56	−138	1.66	37	0.283	105	0.64	−120

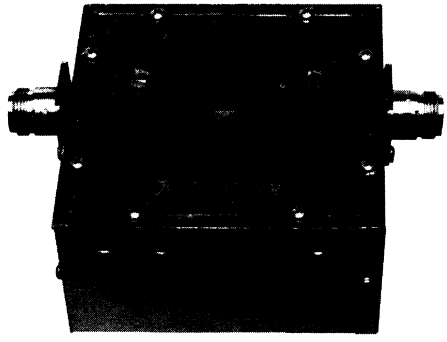


Figure 8. Test Circuit, Top View (MRF158R)

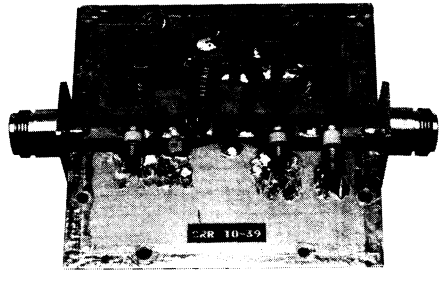


Figure 9. Test Circuit, Bottom View (MRF158R)

Table 2. Typical Common Emitter S-Parameters (MRF158)

V_{DS} (Volts)	I_D (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
28	100	5	1.00	−2.0	3.84	−179	0.003	73	0.97	−2.0
		10	1.00	−2.0	3.81	179	0.004	83	0.97	−2.0
		30	1.00	−7.0	3.74	174	0.011	81	0.97	−6.0
		50	1.00	−11	3.72	170	0.018	78	0.96	−9.0
		100	0.98	−21	3.62	159	0.034	70	0.95	−19
		200	0.93	−41	3.28	137	0.061	52	0.90	−35
		300	0.88	−58	2.88	120	0.077	39	0.86	−50
		400	0.83	−75	2.57	104	0.088	27	0.81	−63
		500	0.79	−87	2.24	91	0.090	17	0.78	−74
		600	0.75	−99	1.94	78	0.084	8.0	0.75	−84
		700	0.73	−110	1.72	68	0.077	2.0	0.75	−93
		800	0.72	−120	1.52	58	0.067	−3.0	0.75	−99
		900	0.71	−130	1.35	48	0.055	−6.0	0.74	−108
		1000	0.71	−139	1.18	40	0.043	−4.0	0.73	−114

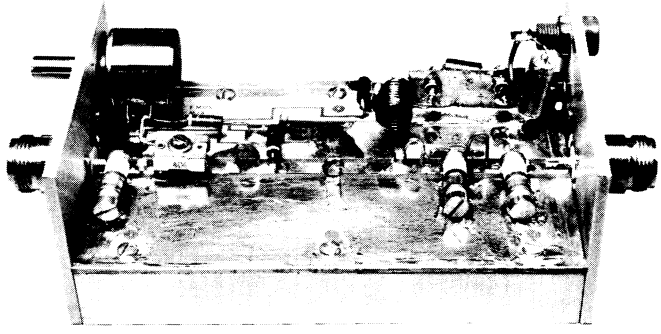
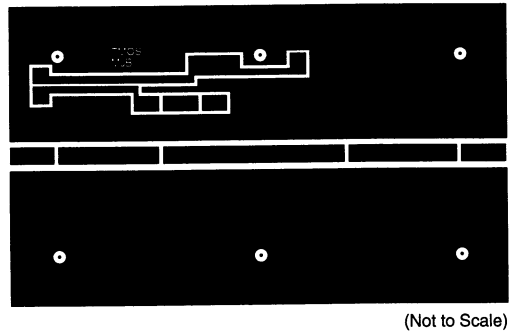


Figure 10. Test Circuit (MRF158)



(Not to Scale)

Figure 11. PC Board Photomaster (MRF158)

MRF164W

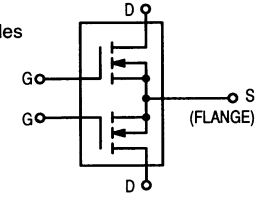
Motorola Preferred Devices

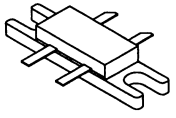
The RF TMOS Line
Power Field Effect Transistor
N-Channel Enhancement Mode

Designed primarily for wideband large-signal output and driver stages to 500 MHz.

- Guaranteed Performance at 400 MHz, 28 Vdc
- Output Power = 20 W
- Minimum Gain = 15 dB
- Push-Pull Configuration Reduces Even Numbered Harmonics
- Excellent Thermal Stability, Ideally Suited for Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 100% Tested for Load Mismatch at All Phase Angles with 30:1 VSWR

20 W, to 500 MHz
TMOS
BROADBAND
RF POWER FET





CASE 412-01, STYLE 1

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	5.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	116 0.67	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

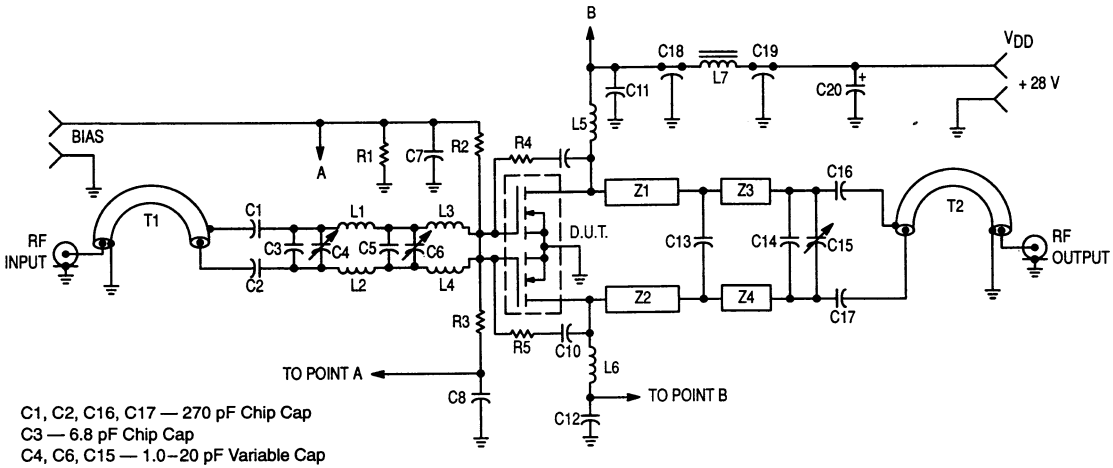
NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Preferred devices are Motorola recommended choices for future use and best overall value.

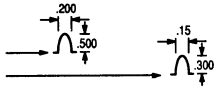
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	1.0	mAdc
Gate-Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 10 mA)	$V_{GS(th)}$	1.0	4.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 0.75 A)	g_{fs}	400	500	—	mmhos
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	18	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	20	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	2.5	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 1) (2)					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 20 W, f = 400 MHz, I_{DQ} = 50 mA)	G_{ps}	15	17	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 20 W, f = 400 MHz, I_{DQ} = 50 mA)	η	45	50	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 20 W, f = 400 MHz, I_{DQ} = 50 mA, Load VSWR 30:1 at all Phase Angles)	Ψ	No Degradation in Output Power Before and After Test			

NOTES:
1. Each side of device measured separately.
2. Measured in push-pull configuration.



C1, C2, C16, C17 — 270 pF Chip Cap
C3 — 6.8 pF Chip Cap
C4, C6, C15 — 1.0–20 pF Variable Cap
C5 — 18 pF Chip Cap
C7, C8, C11, C12 — 0.1 μF Ceramic Cap
C9, C10 — 0.01 μF Ceramic Cap
C13 — 6.8 pF Chip Cap
C14 — 4.7 pF Chip Cap
C18, C19 — 620 pF feedthru Cap
C20 — 10 μF 50 V Tantalum Cap
L1, L2 — Hairpin Inductor #18 Wire
L3, L4 — Hairpin Inductor #18 Wire
L5, L6 — 10 Turns #18 W .300 ID
L7 — VK-200/19-4B



R1 — 1.0K 1/4 W Resistor
R2, R3 — 10K 1/4 W Resistor
R4, R5 — 470 Ω 1/4 W Resistor
T1, T2 — Balun 2″ 50 Ω Semi Ridgid Coax
Z1, Z2 — Microstrip Element .850 long x .125 W
Z3, Z4 — Microstrip Element .525 long x .125 W
Board Material — Teflon Fiberglass, ε_r = 2.55 Copper Clad, 2 oz. Copper
.060″ Dielectric Thickness

Figure 1. 400 MHz Test Circuit

TYPICAL CHARACTERISTICS

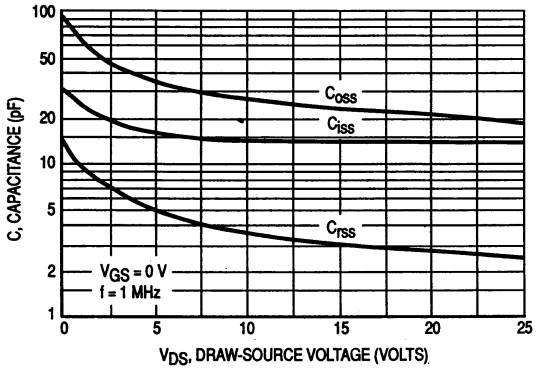


Figure 2. Capacitance versus Voltage

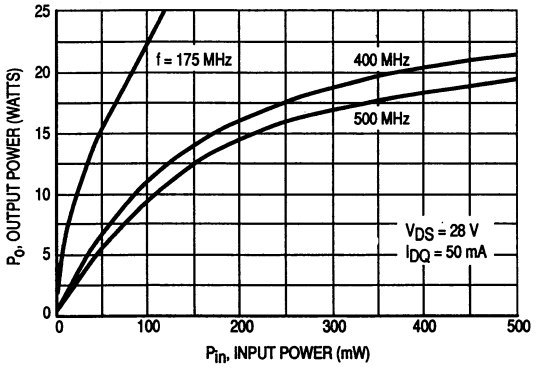


Figure 3. Output Power versus Input Power

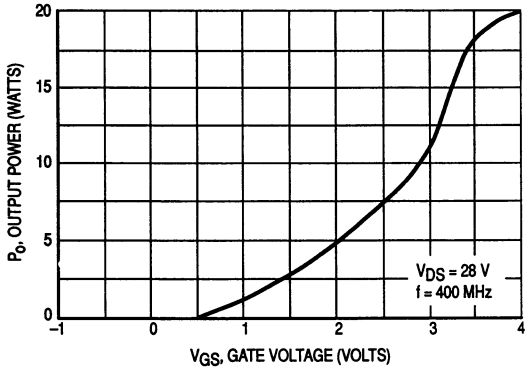


Figure 4. Output Power versus Gate Voltage

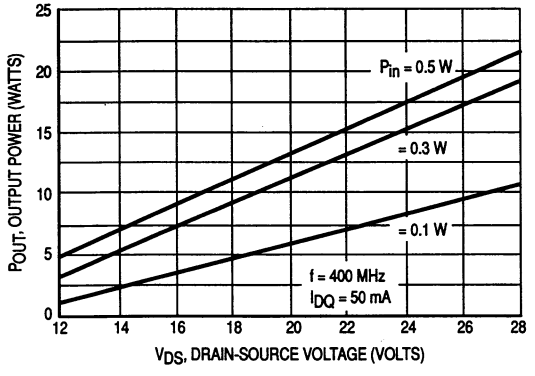
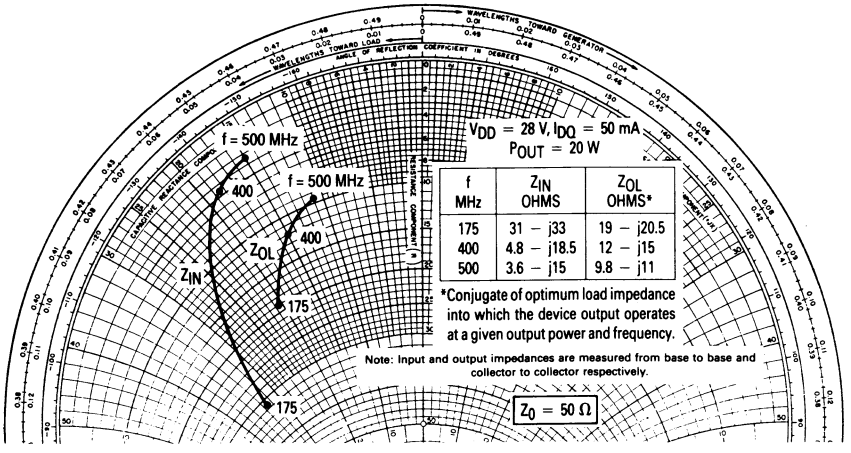
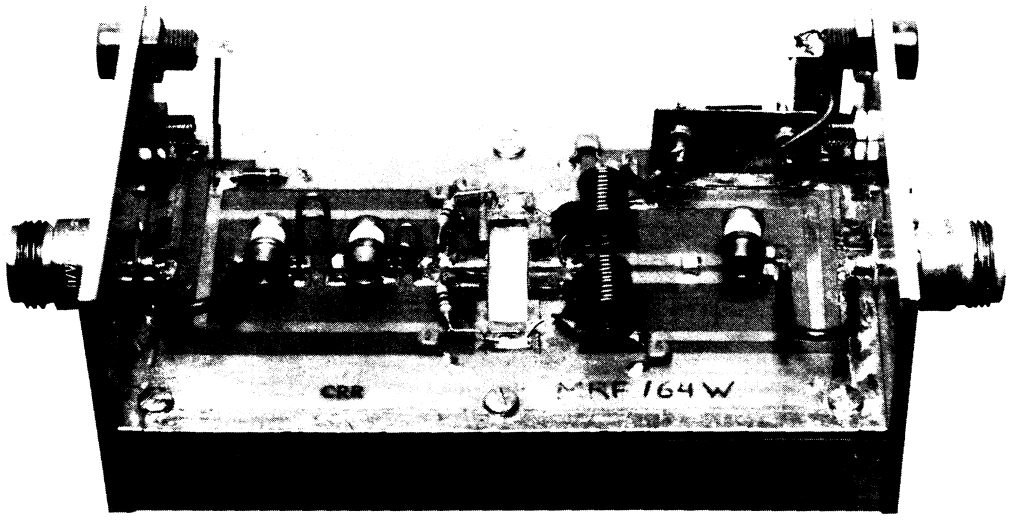


Figure 5. Output Power versus Voltage



f MHz	Z_{IN} OHMS	Z_{OL} OHMS*
175	31 − j33	19 − j20.5
400	4.8 − j18.5	12 − j15
500	3.6 − j15	9.8 − j11

Figure 6. Series Equivalent Input/Output Impedances



2

Figure 7. Test Amplifier

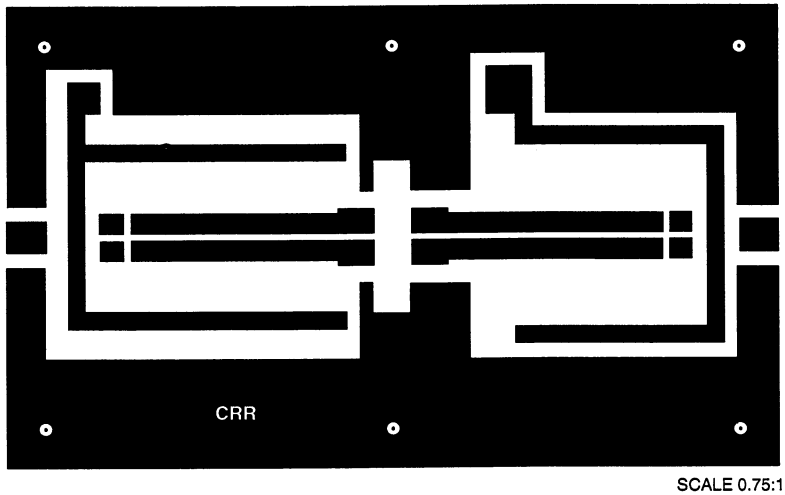


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Figure 8. Circuit Board Photomaster

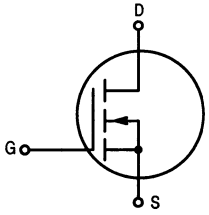
MRF166
MRF166C

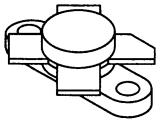
20 W, 500 MHz
MOSFET
BROADBAND
RF POWER FETs

The RF MOSFET Line
RF Power
Field Effect Transistors
N-Channel Enhancement Mode MOSFETs

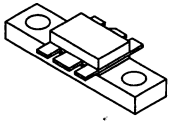
Designed primarily for wideband large-signal output and driver from 30–500 MHz.

- Low C_{rss} — 4.5 pF @ V_{DS} = 28 V
- MRF166C — Typical Performance at 400 MHz, 28 Vdc
  Output Power = 20 W
  Gain = 17 dB
  Efficiency = 55%
- Optional 4-Lead Flange Package (MRF166)
- Replacement for Industry Standards such as MRF136, DV2820, BLF244, SD1902, and ST1001
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- Excellent Thermal Stability, Ideally Suited for Class A Operation





CASE 211-07, STYLE 2



CASE 319, STYLE 3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Gate Voltage	V_{DSS}	65	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate-Source Voltage	V_{GS}	±40	Adc
Drain Current — Continuous	I_D	4.0	Adc
Total Device Dissipation @ T_C = 25°C Derate Above 25°C	P_D	70 0.4	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to 150	°C
Operating Junction Temperature	T_J	200	°C

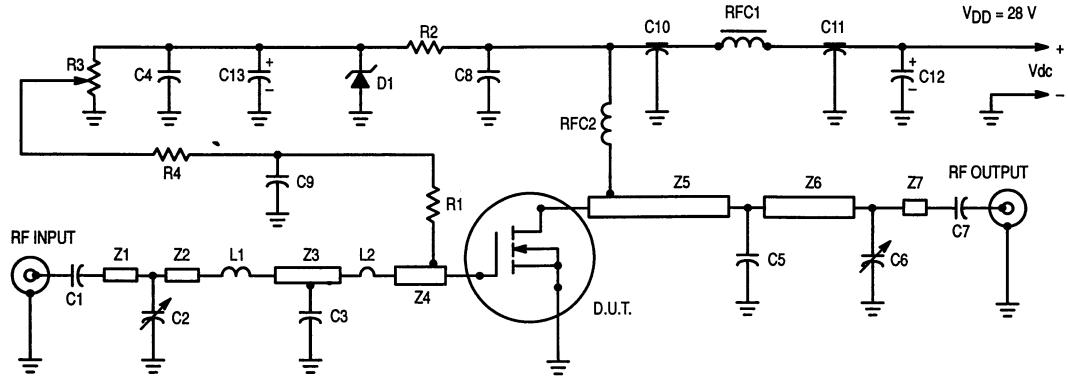
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0 V, I_D = 5.0 mA)	$V_{(BR)DSS}$	65	—	—	V
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	—	—	1.0	mA
Gate-Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0 V)	I_{GSS}	—	—	1.0	μA
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 25 mA)	$V_{GS(th)}$	1.0	3.0	6.0	V
Forward Transconductance (V_{DS} = 10 V, I_D = 1.5 A)	g_{fs}	600	800	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	—	30	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{oss}	—	35	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{rss}	—	4.5	—	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure (V_{DD} = 28 V, f = 30 MHz, I_{DQ} = 50 mA)	NF	—	2.5	—	dB
MRF166C					
Common Source Power Gain (V_{DD} = 28 V, P_{out} = 20 W, f = 400 MHz, I_{DQ} = 100 mA)	G_{ps}	14	17	—	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 20 W, f = 400 MHz, I_{DQ} = 100 mA)	η	50	55	—	%
Electrical Ruggedness (V_{DD} = 28 V, P_{out} = 20 W, f = 400 MHz, I_{DQ} = 100 mA, Load VSWR 30:1 at All Phase Angles)	ψ	No Degradation in Output Power			
MRF166					
Common Source Power Gain (V_{DD} = 28 V, P_{out} = 20 W, f = 150 MHz, I_{DQ} = 25 mA)	G_{ps}	15	19	—	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 20 W, f = 150 MHz, I_{DQ} = 25 mA)	η	55	65	—	%
Electrical Ruggedness (V_{DD} = 28 V, P_{out} = 20 W, f = 150 MHz, I_{DQ} = 25 mA, Load VSWR 30:1 at All Phase Angles)	ψ	No Degradation in Output Power			
Series Equivalent Input Impedance (V_{DD} = 28 V, P_{out} = 20 W, f = 150 MHz, I_{DQ} = 25 mA)	Z_{in}	—	3.99 – j12.2	—	Ohms
Series Equivalent Output Impedance (V_{DD} = 28 V, P_{out} = 20 W, f = 150 MHz, I_{DQ} = 25 mA)	Z_{out}	—	14.15 – j6.51	—	Ohms

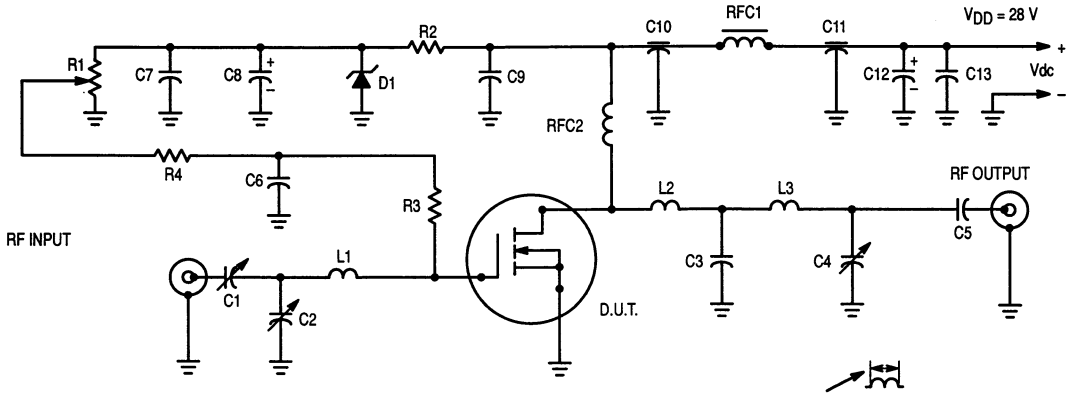


C1, C7 — 270 pF Chip Capacitor
C2, C6 — Johanson Trimmer Capacitor, 2–20 pF
C3 — 21 pF Mini Unelco
C4, C8, C9 — 0.01 µF
C5 — 18 pF Mini Unelco
C10, C11 — 680 pF Feed Through
C12, C13 — 50 µF, 50 V
D1 — 1N5925A Motorola Zener

Board Material — Teflon fiberglass
2 oz. Copper clad both sides, $\varepsilon_r = 2.55$
0.060″ Dielectric Thickness

L1 — #18 AWG, 2 Turns, 0.25″ ID 0.15″ Wide
L2 — #18 AWG Hairpin 0.7″ long, bend into hairpin
RFC1 — Ferroxcube VK200-19/4B
RFC2 — 18 Turns #18 AWG Enameled, 0.3″ ID
R1 — 220 Ω 1/2 Watt
R2 — 1.8 kΩ 1/4 Watt
R3 — 10 kΩ, 10 Turns Bourns
R4 — 10 k 1/4 Watt
Z1 — Microstrip Line 0.150″ wide, 0.420″ long
Z2 — Microstrip Line 0.150″ wide, 0.350″ long
Z3 — Microstrip Line 0.150″ wide, 0.350″ long
Z4 — Microstrip Line 0.150″ wide, 0.450″ long
Z5 — Microstrip Line 0.150″ wide, 1.1″ long
Z6 — Microstrip Line 0.150″ wide, 0.650″ long
Z7 — Microstrip Line 0.150″ wide, 0.200″ long

Figure 1. MRF166C 400 MHz Test Circuit



C1, C2 — 406 ARCO
C3 — 39 pF ATC 100 Mil Chip Cap
C4 — 403 ARCO
C5 — 470 pF ATC 100 Mil Chip Cap
C6, C7, C9, C13 — 0.01 µF
C8, C12 — 50 µF, 50 V
C10, C11 — 680 pF Feed Through
D1 — 1N5925A Motorola Zener

L1 — #20 AWG 2 Turns, 0.235″ ID, 0.10″ OD
L2 — #18 AWG 2 Turns, 0.225″ ID, 0.22″ OD
L3 — #18 AWG 2 Turns, 0.325″ ID, 0.13″ OD
RFC1 — Ferroxcube VK200-19/4B
RFC2 — 18 Turns #18 AWG Enameled, 0.3″ ID
R1 — 10 kΩ, 10 Turn Bourns
R2 — 1.8 kΩ 1/4 Watt
R3 — 120 Ω 1/2 Watt
R4 — 10 kΩ 1/4 Watt
Board Material — 0.062″ G10, 2 oz Cu Clad Double Sided

Figure 2. MRF166 150 MHz Test Circuit

TYPICAL CHARACTERISTICS

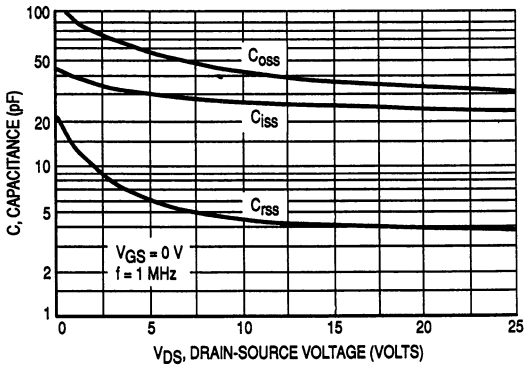


Figure 3. Capacitance versus Drain-Source Voltage

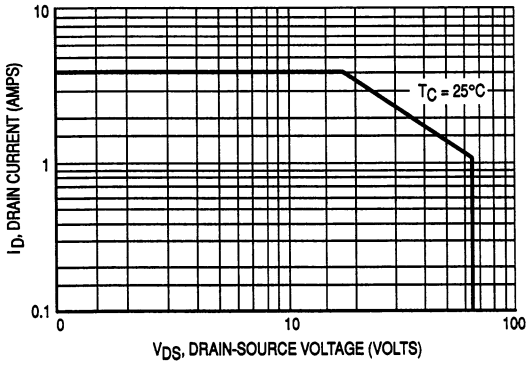


Figure 4. DC Safe Operating Area

MRF166

2

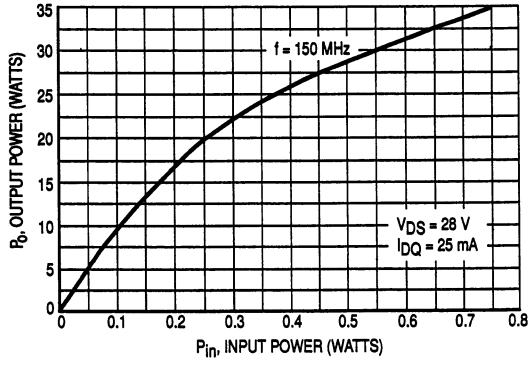


Figure 5. Output Power versus Input Power

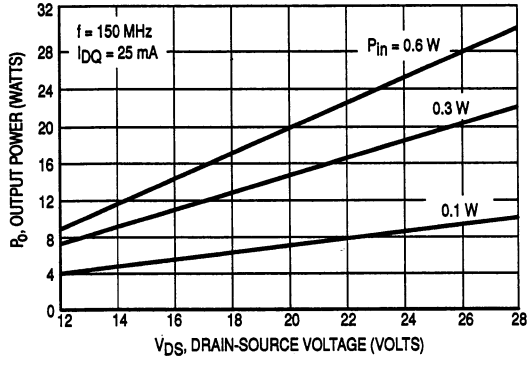


Figure 6. Output Power versus Voltage

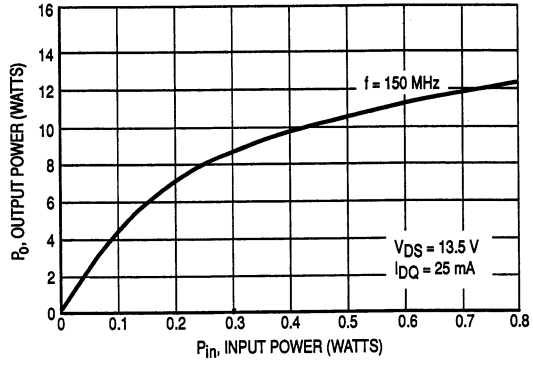


Figure 7. Output Power versus Input Power

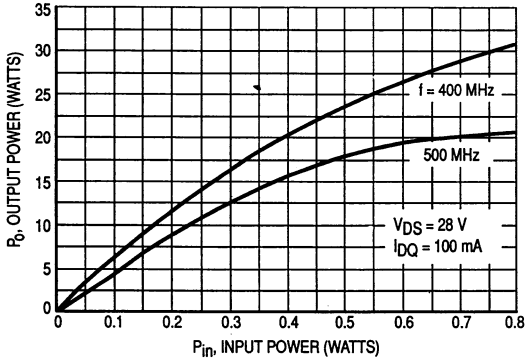


Figure 8. Output Power versus Input Power

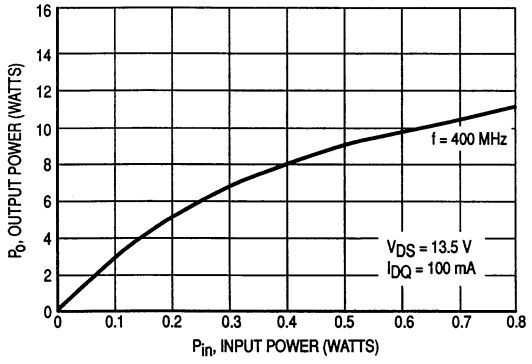


Figure 9. Output Power versus Input Power

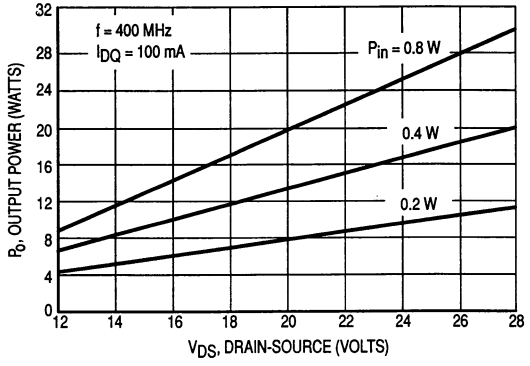
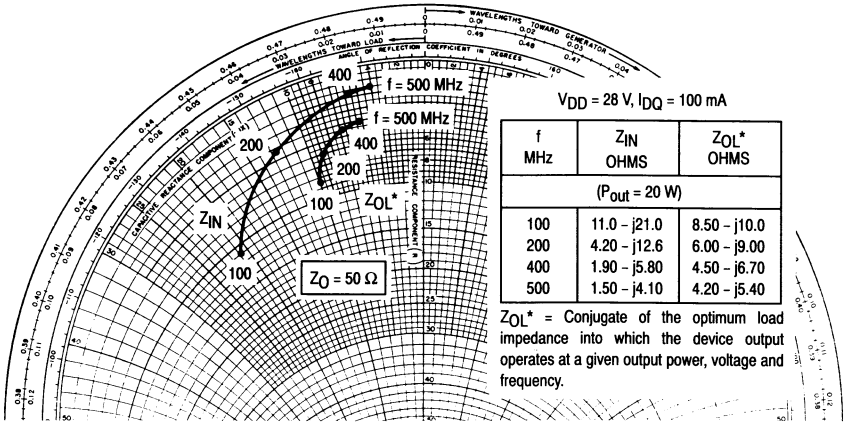


Figure 10. Output Power versus Voltage



f MHz	Z_{IN} OHMS	Z_{OL}* OHMS
(P_{out} = 20 W)		
100	11.0 – j21.0	8.50 – j10.0
200	4.20 – j12.6	6.00 – j9.00
400	1.90 – j5.80	4.50 – j6.70
500	1.50 – j4.10	4.20 – j5.40

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 11. Series Equivalent Input and Output Impedance

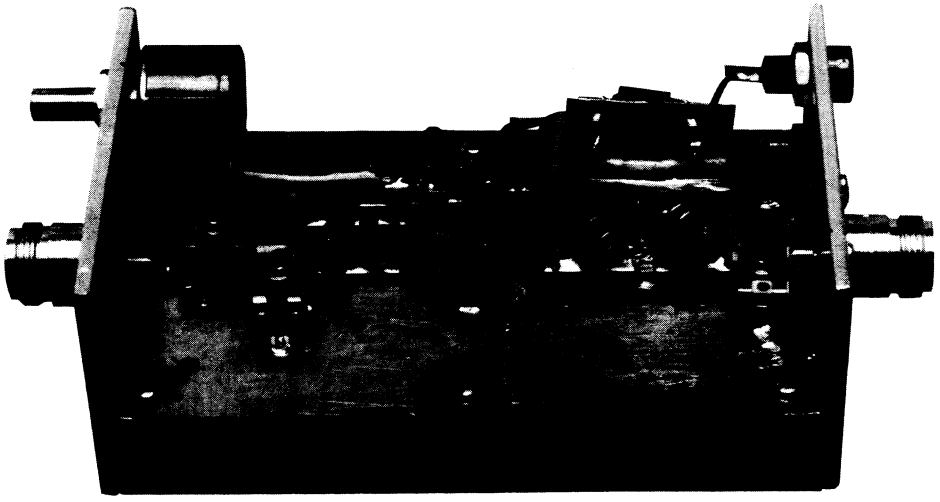
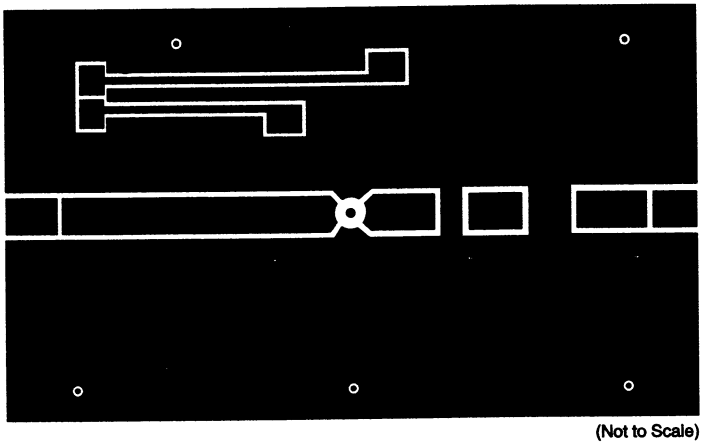


Figure 12. Test Fixture MRF166



(Not to Scale)

Figure 13. Photomaster for MRF166 Test Fixture