MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

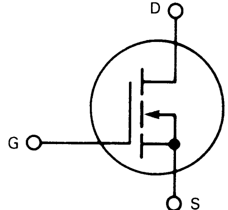
MRF161

The RF Line

N-CHANNEL ENHANCEMENT-MODE TMOS RF POWER FIELD-EFFECT TRANSISTOR

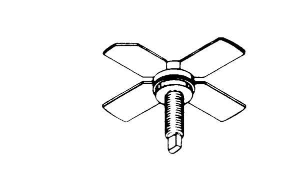
. . . designed for wideband large-signal amplifier and oscillator applications in the 2.0 to 400 MHz range.

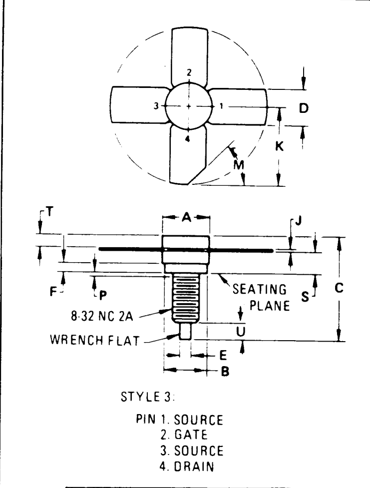
- Guaranteed 28 Volt, 400 MHz Performance
  Output Power = 5.0 Watts
  Minimum Gain = 11 dB
  Efficiency = 50% (Typical)
- Small-Signal and Large-Signal Characterization
- 100% Tested for Load Mismatch At All Phase Angles With 30:1 VSWR
- Low Noise Figure — 3.0 dB (Typ) at 100 mA, 400 MHz
- Excellent Thermal Stability, Ideally Suited For Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques



5.0 W 2.0–400 MHz

N-CHANNEL TMOS BROADBAND RF POWER FET





STYLE 3:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	14.99	16.51	0.590	0.650
D	5.46	5.96	0.215	0.235
E	1.40	1.65	0.055	0.065
F	1.52	–	0.060	–
J	0.08	0.17	0.003	0.007
K	11.05	–	0.435	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
S	3.00	3.25	0.118	0.128
T	1.40	1.78	0.055	0.070
U	2.92	3.68	0.115	0.145

CASE 244-04

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	0.9	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	17.5 0.10	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W

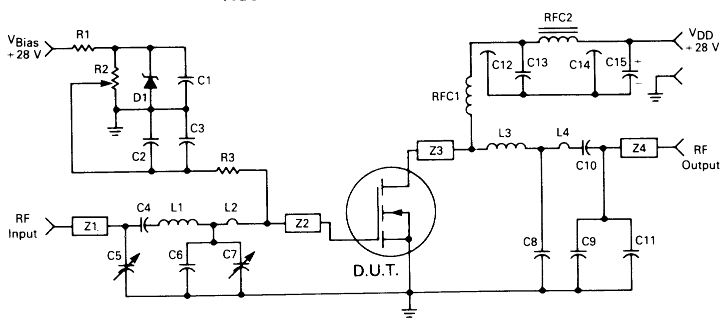
Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Resonable precautions in handling and packaging MOS devices should be observed.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	1.0	mAdc
Gate-Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 10 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 100 mA)	g_{fs}	80	110	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	7.0	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	9.7	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	2.3	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 1)					
Noise Figure (V_{DS} = 28 Vdc, I_D = 100 mA, f = 400 MHz, Z_S = 67.6 + j14.1, Z_L = 14.5 + j25.7)	NF	—	3.0	—	dB
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 5.0 W, f = 400 MHz, I_{DQ} = 50 mA)	G_{ps}	11	13.5	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 5.0 W, f = 400 MHz, I_{DQ} = 50 mA)	η	45	50	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 5.0 W, f = 400 MHz, I_{DQ} = 50 mA, VSWR 30:1 at All Phase Angles)	ψ	No Degradation in Output Power			

FIGURE 1 — 400 MHz TEST CIRCUIT



C1, C2, C13 — 0.1 μF, 50 V Disc Ceramic
C3 — 0.01 μF, 100 V Disc Ceramic
C4, C10 — 220 pF, 100 Mil Chip Cap
C5 — 1-10 pF Johanson or Equivalent
C6 — 5.0 pF Mini-Unleco or Equivalent
C7 — 1-20 pF Johanson or Equivalent
C8 — 15 pF, 100 Mil ATC Chip Cap or Equivalent
C9, C11 — 2.2, 100 Mil ATC Chip Cap or Equivalent
C12, C14 — 680 pF Feedthru
C15 — 50 μF, 35 V
R1 — 1.6 kΩ, 1/4 W
R2 — 10 Turns 10 kΩ
R3 — 10 k, 1/2 W
D1 — 1N5347B Motorola Zener or Equivalent

L1 — 1-3/4 Turns, 0.185″ ID 0.08″ Long #20 AWG Enamel — (25 nH)
L2 — #20 AWG Enamel, Hairpin 0.353″ — (10.5 nH) 0.185″

L3 — 1-3/4 Turns, 0.128″ ID 0.11″ Long #18 AWG Enamel — (15 nH)
L4 — #18 AWG Enamel, Hairpin 0.410″ — (12.5 nH) 0.185″

RFC1 — 10 Turns, 0.300″ ID #20 AWG Enamel Closewound
RFC2 — Ferroxcube VK-200
Z1 — 0.82″ x 0.164″ Microstrip — (Z_O = 50 Ω)
Z2, Z3 — 0.60″ x 0.25″ Microstrip
Z4 — 0.76″ x 0.164″ Microstrip — (Z_O = 50 Ω)
Board-Glass Teflon, 62 Mils, ϵ_r = 2.56

FIGURE 2 — OUTPUT POWER versus INPUT POWER

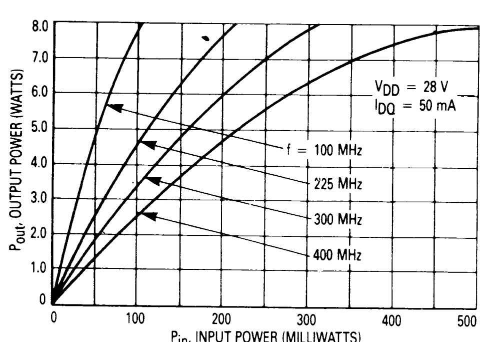


FIGURE 3 — OUTPUT POWER versus INPUT POWER

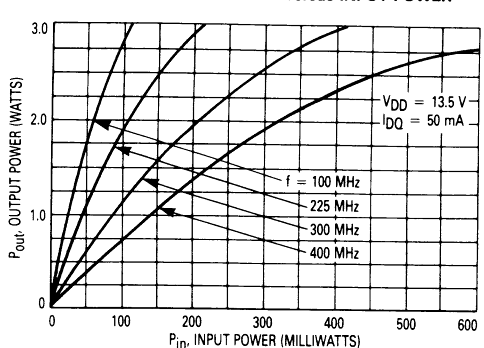


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 400 MHz

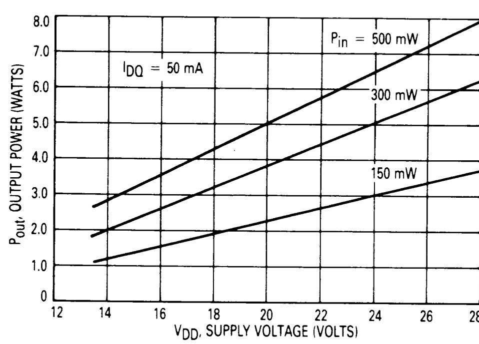


FIGURE 5 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 300 MHz

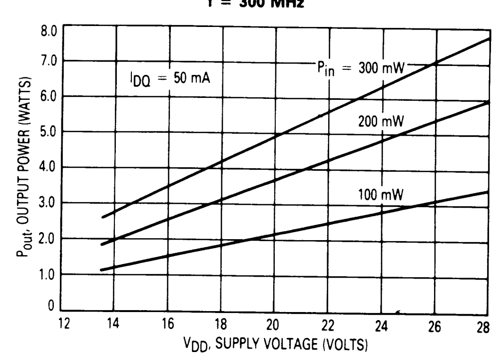


FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 225 MHz

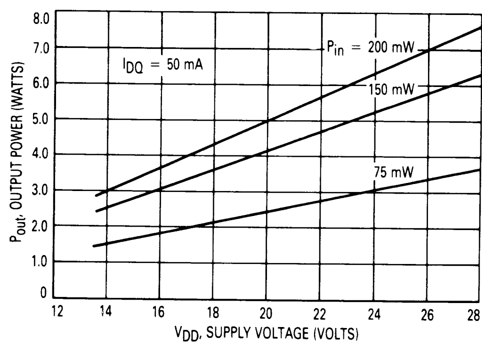
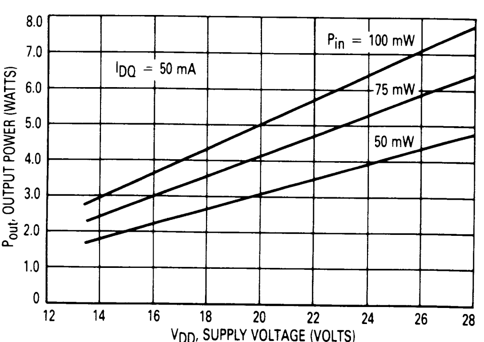


FIGURE 7 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 100 MHz



3

FIGURE 8 — OUTPUT POWER versus GATE VOLTAGE

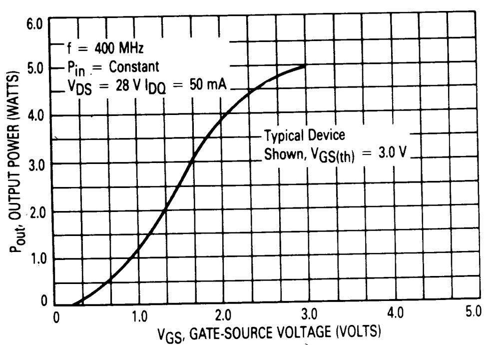


FIGURE 9 — DRAIN CURRENT versus GATE VOLTAGE (TRANSFER CHARACTERISTICS)

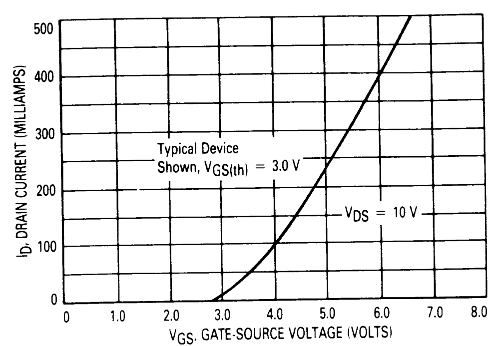


FIGURE 10 — GATE-SOURCE VOLTAGE versus CASE TEMPERATURE

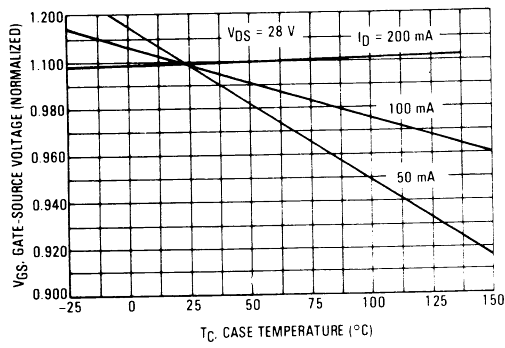


FIGURE 11 — CAPACITANCE versus VOLTAGE

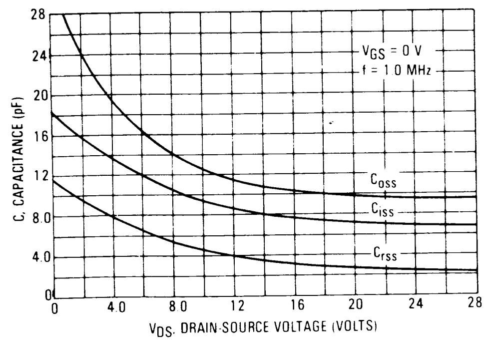


FIGURE 12 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

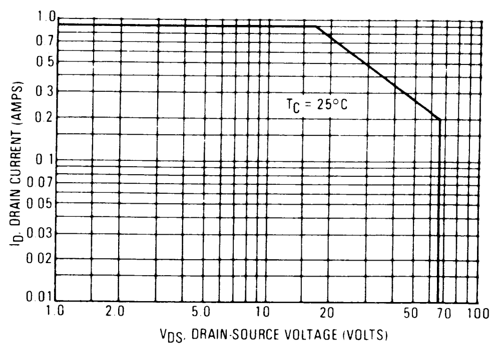
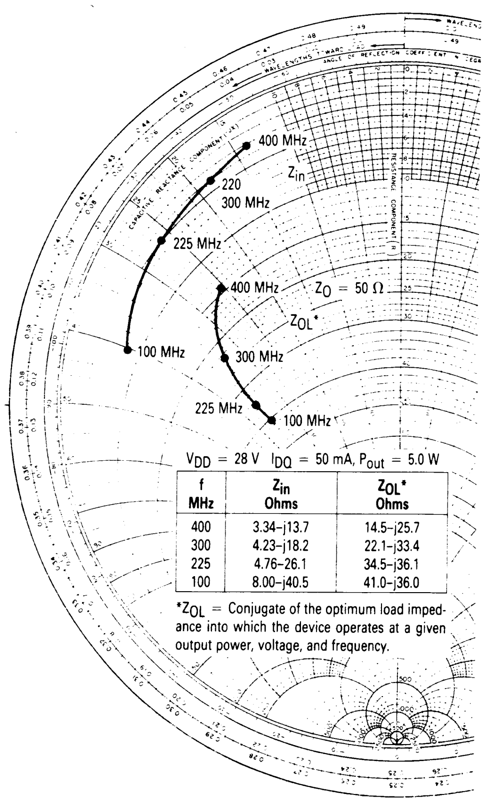


FIGURE 13 — LARGE-SIGNAL SERIES EQUIVALENT INPUT AND OUTPUT IMPEDANCE, Z_{in}, Z_{OL}*



V_{DD} = 28 V I_{DQ} = 50 mA, P_{out} = 5.0 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
400	3.34–j13.7	14.5–j25.7
300	4.23–j18.2	22.1–j33.4
225	4.76–26.1	34.5–j36.1
100	8.00–j40.5	41.0–j36.0

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

FIGURE 14 — COMMON SOURCE SCATTERING PARAMETERS
50 OHM SYSTEM
V_{DS} = 28 V, I_D = 250 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
2.0	1.000	−1.69	13.64	178	0.002	62	0.947	−1.84
5.0	1.000	−4.63	13.60	176	0.005	69	0.945	−4.00
10	0.997	−8.95	13.70	173	0.010	80	0.941	−7.92
20	0.989	−17.49	13.36	167	0.022	73	0.929	−15.8
30	0.977	−26	13.07	162	0.032	71	0.915	−23
40	0.968	−34	12.76	156	0.042	67	0.902	−30
50	0.949	−42	12.31	151	0.050	61	0.885	−37
60	0.930	−49	11.88	146	0.058	57	0.866	−43
70	0.913	−56	11.45	141	0.066	53	0.846	−49
80	0.897	−62	10.96	137	0.072	50	0.831	−55
90	0.885	−68	10.50	133	0.078	46	0.817	−60
100	0.867	−74	10.00	129	0.081	43	0.800	−65
110	0.853	−78	9.54	125	0.085	40	0.787	−69
120	0.838	−84	8.92	122	0.090	37	0.775	−74
130	0.819	−88	8.75	119	0.093	35	0.762	−78
140	0.812	−92	8.30	116	0.096	31	0.755	−81
150	0.800	−96	7.95	113	0.098	28	0.742	−86
160	0.785	−99	7.54	111	0.100	26	0.735	−89
170	0.775	−103	7.25	109	0.102	24	0.728	−93
180	0.765	−105	6.85	106	0.103	23	0.725	−96
190	0.755	−108	6.60	104	0.104	21	0.720	−98
200	0.740	−111	6.20	100	0.106	18	0.719	−99
225	0.735	−116	5.71	96	0.110	16	0.715	−103
250	0.723	−121	5.17	92	0.112	12	0.708	−107
275	0.720	−124	4.80	89	0.113	10	0.706	−110
300	0.716	−128	4.43	85	0.112	7.0	0.706	−113
325	0.715	−130	4.17	83	0.111	4.0	0.717	−115
350	0.715	−133	3.87	79	0.111	3.0	0.720	−117
375	0.715	−135	3.67	76	0.111	1.0	0.728	−118
400	0.711	−137	3.43	74	0.109	0	0.729	−119
425	0.714	−139	3.25	71	0.104	0	0.738	−120
450	0.717	−140	3.11	69	0.104	−2.0	0.743	−121
475	0.719	−141	2.95	67	0.103	−3.0	0.757	−122
500	0.722	−142	2.81	65	0.102	−4.0	0.770	−122
525	0.723	−144	2.69	62	0.099	−6.0	0.777	−123
550	0.727	−144	2.55	61	0.097	−6.0	0.787	−123
575	0.729	−145	2.46	59	0.097	−7.0	0.802	−124
600	0.733	−146	2.37	57	0.094	−7.0	0.814	−124
625	0.734	−147	2.29	55	0.090	−8.0	0.824	−126
650	0.740	−148	2.19	54	0.087	−8.0	0.830	−127
675	0.749	−149	2.12	53	0.085	−6.0	0.849	−127
700	0.758	−149	2.07	51	0.084	−6.0	0.879	−127
725	0.761	−150	1.99	49	0.082	−5.0	0.886	−127
750	0.763	−151	1.93	48	0.081	−4.0	0.905	−127
775	0.765	−151	1.90	48	0.079	−3.0	0.919	−128
800	0.770	−152	1.83	46	0.076	−1.0	0.921	−128

FIGURE 15 — S_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V, I_D = 250 mA

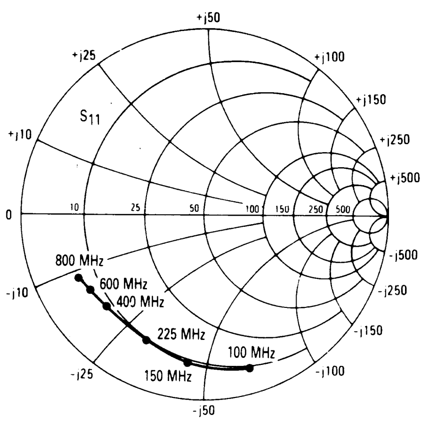


FIGURE 16 — S_{12}, REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V, I_D = 250 mA

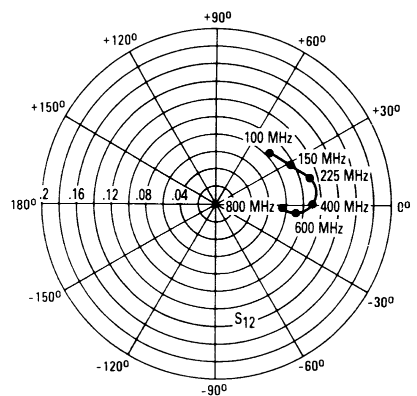


FIGURE 17 — S_{21}, FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V, I_D = 250 mA

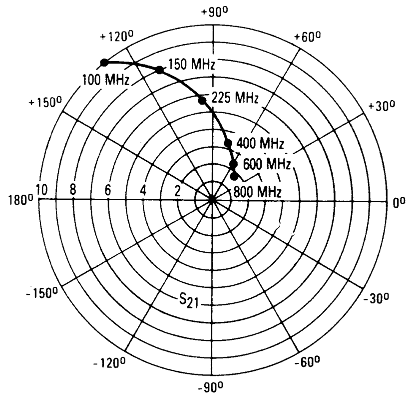
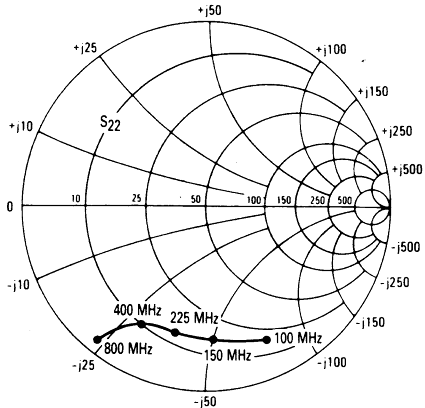


FIGURE 18 — S_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{OS} = 28 V, I_D = 250 mA



DESIGN CONSIDERATIONS

The MRF161 is a TMOS RF power N-Channel enhancement mode field-effect transistor (FET) designed especially for UHF power amplifier and oscillator applications. Motorola TMOS FETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V-groove vertical power FETs.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of TMOS RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF161 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF161 was characterized at I_{DQ} = 50 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some applications may require a more elaborate bias system.

GAIN CONTROL

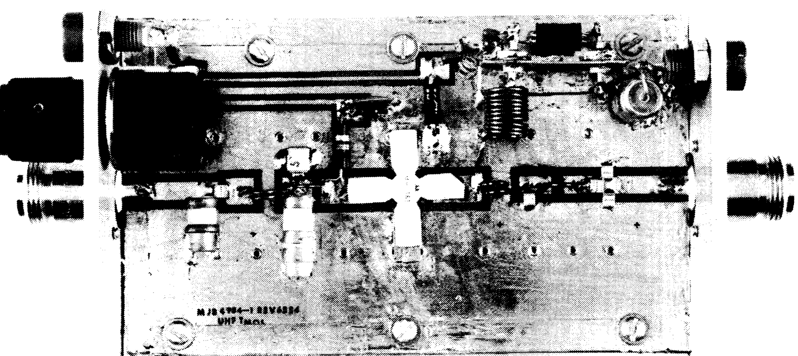
Power output of the MRF161 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC, and modulation systems. (See Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar UHF transistors are suitable for the MRF161. See Motorola Application Note AN721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of TMOS FETs helps ease the task of broadband network design. Both small signal scattering parameters and large signal impedances are provided. While the s-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of TMOS power FETs.

RF power FETs are triode devices and, therefore, not unilateral. This, coupled with the very high gain of the MRF161, yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. Two port parameter stability analysis with the MRF161 s-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A for a discussion of two port network theory and stability.

FIGURE 19 — 400 MHz TEST CIRCUIT



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MRF162

The RF Line

15 W 2.0-400 MHz

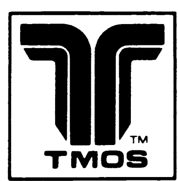
N-CHANNEL TMOS
BROADBAND RF POWER

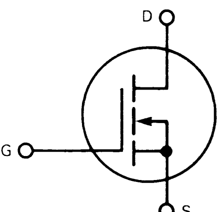
FET

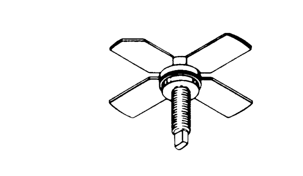
N-CHANNEL ENHANCEMENT-MODE TMOS RF POWER FIELD-EFFECT TRANSISTOR

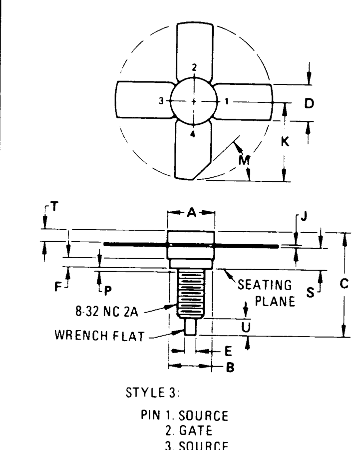
. . . designed for wideband large-signal output and driver applications in the 2.0 to 400 MHz range.

- Guaranteed 28 Volt, 400 MHz Performance
  Output Power = 15 Watts
  Minimum Gain = 11 dB
  Efficiency = 50% (Typical)
- Small-Signal and Large-Signal Characterization
- 100% Tested for Load Mismatch At All Phase Angles With 30:1 VSWR
- Low Noise Figure — 2.0 dB (Typ) at 300 mA, 400 MHz
- Excellent Thermal Stability, Ideally Suited For Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques









STYLE 3:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	14.99	16.51	0.590	0.650
D	5.46	5.96	0.215	0.235
E	1.40	1.65	0.055	0.065
F	1.52	–	0.060	–
J	0.08	0.17	0.003	0.007
K	11.05	–	0.435	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
S	3.00	3.25	0.118	0.128
T	1.40	1.78	0.055	0.070
U	2.92	3.68	0.115	0.145

CASE 244-04

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	2.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.286	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

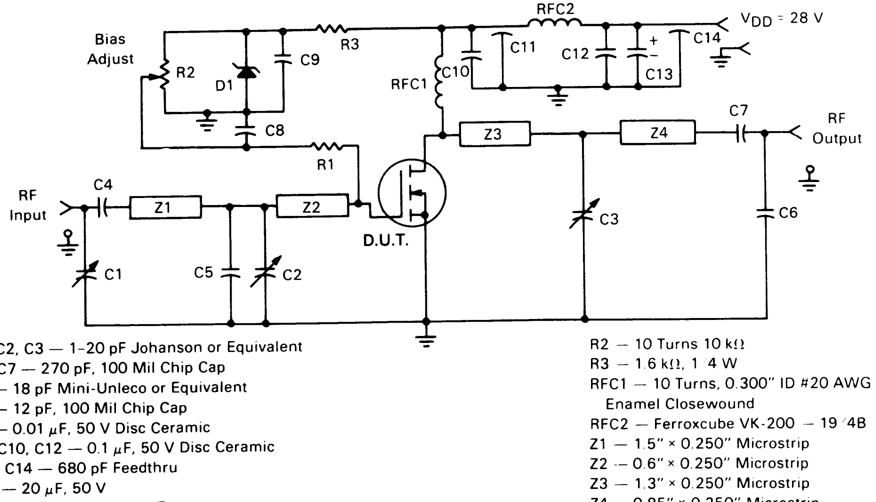
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.5	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	2.0	mAdc
Gate-Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 25 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 250 mA)	g_{fs}	250	400	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	24	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	27	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	5.5	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 1)					
Noise Figure (V_{DS} = 28 Vdc, I_D = 300 mA, f = 400 MHz, Z_S = 5.9 + j7.8 Ω, Z_L = 3.78 + j5.75 Ω)	NF	—	2.0	—	dB
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 15 W, f = 400 MHz, I_{DQ} = 50 mA)	G_{ps}	11	13.6	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 15 W, f = 400 MHz, I_{DQ} = 50 mA)	η	45	50	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 15 W, f = 400 MHz, I_{DQ} = 50 mA, VSWR 30:1 at All Phase Angles)	ψ	No Degradation in Output Power			

FIGURE 1 — 400 MHz TEST CIRCUIT



C1, C2, C3 — 1-20 pF Johanson or Equivalent
C4, C7 — 270 pF, 100 Mil Chip Cap
C5 — 18 pF Mini-Unleco or Equivalent
C6 — 12 pF, 100 Mil Chip Cap
C8 — 0.01 μF, 50 V Disc Ceramic
C9, C10, C12 — 0.1 μF, 50 V Disc Ceramic
C11, C14 — 680 pF Feedthru
C13 — 20 μF, 50 V
D1 — 1N5925A Motorola Zener
R1 — 10 kΩ, 1/4 W

R2 — 10 Turns 10 kΩ
R3 — 1.6 kΩ, 1/4 W
RFC1 — 10 Turns, 0.300" ID #20 AWG Enamel Closewound
RFC2 — Ferroxcube VK-200 — 19/4B
Z1 — 1.5" × 0.250" Microstrip
Z2 — 0.6" × 0.250" Microstrip
Z3 — 1.3" × 0.250" Microstrip
Z4 — 0.85" × 0.250" Microstrip
Board — Glass Teflon, 62 Mils, ϵ_r = 2.56

FIGURE 2 — OUTPUT POWER versus INPUT POWER

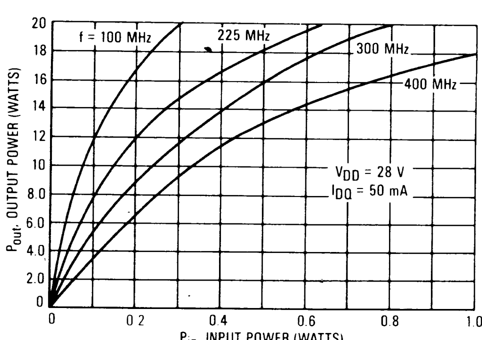


FIGURE 3 — OUTPUT POWER versus INPUT POWER

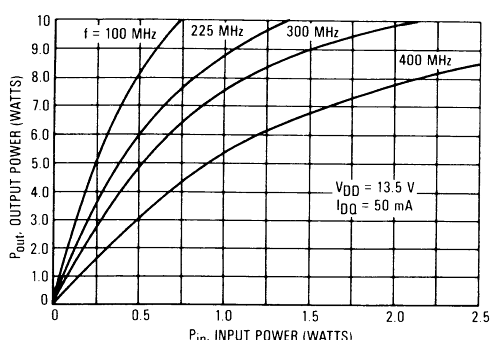


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 400 MHz

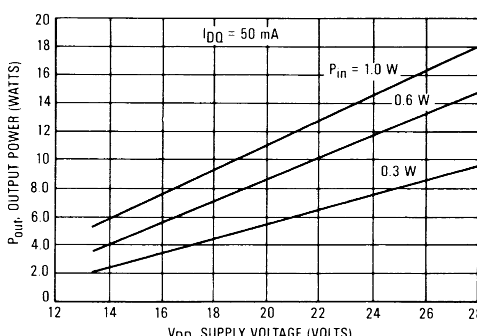


FIGURE 5 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 300 MHz

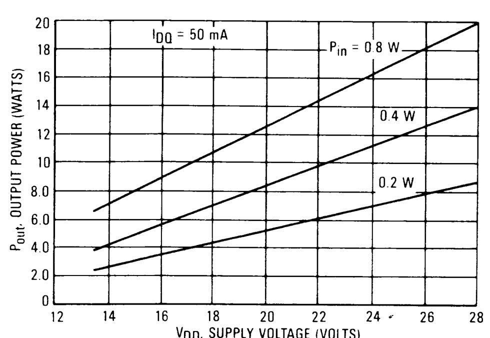


FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 225 MHz

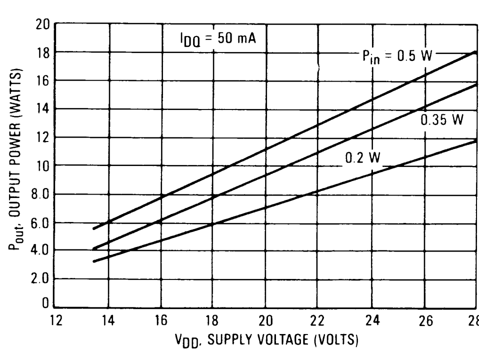


FIGURE 7 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 100 MHz

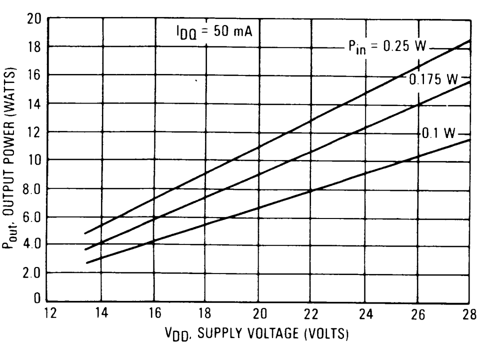


FIGURE 8 — OUTPUT POWER versus GATE VOLTAGE

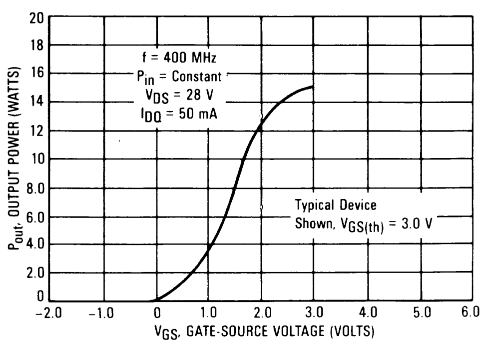


FIGURE 9 — DRAIN CURRENT versus GATE VOLTAGE (TRANSFER CHARACTERISTICS)

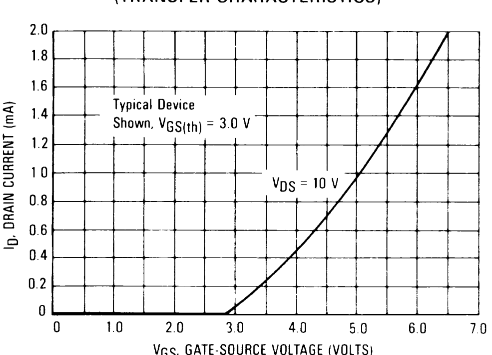


FIGURE 10 — GATE-SOURCE VOLTAGE versus CASE TEMPERATURE

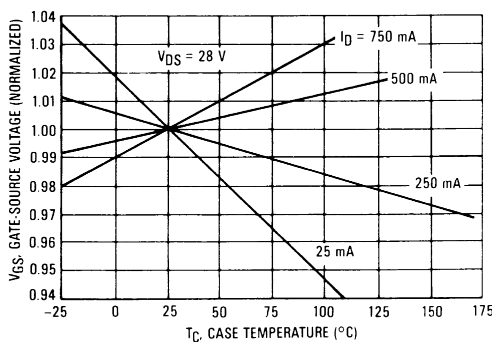


FIGURE 11 — CAPACITANCE versus DRAIN-SOURCE VOLTAGE

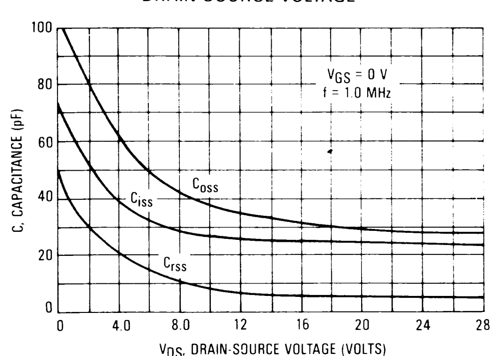


FIGURE 12 — DC SAFE OPERATING AREA

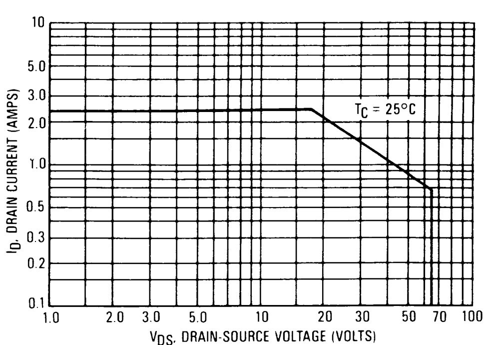
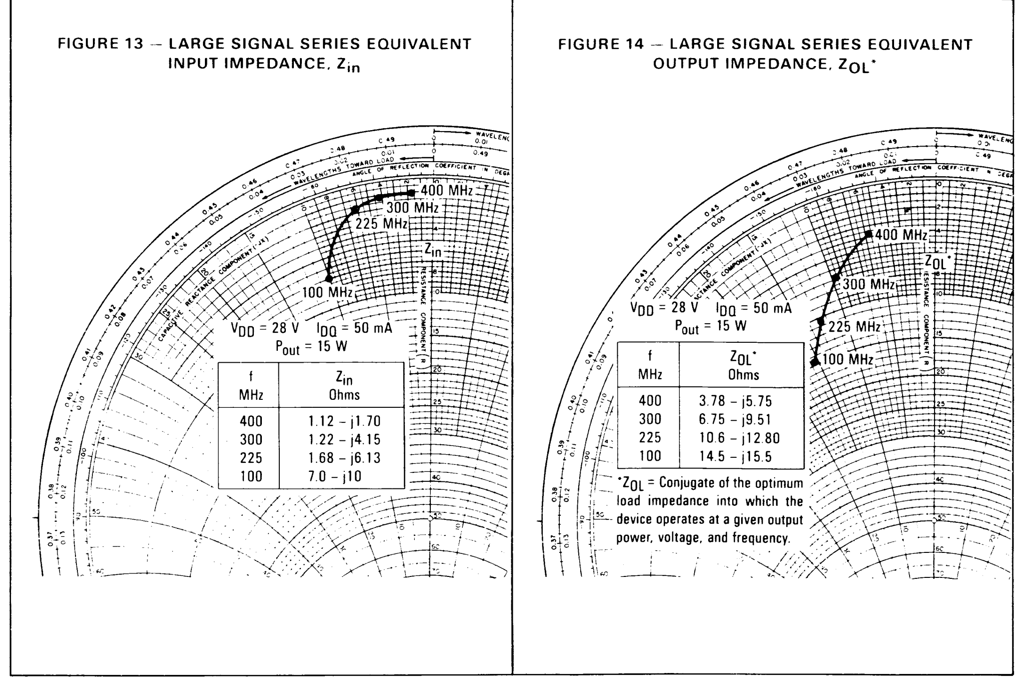


FIGURE 13 — LARGE SIGNAL SERIES EQUIVALENT INPUT IMPEDANCE, Z_{in}

FIGURE 14 — LARGE SIGNAL SERIES EQUIVALENT OUTPUT IMPEDANCE, Z_{OL}*



f MHz	Z_{in} Ohms
400	1.12 – j1.70
300	1.22 – j4.15
225	1.68 – j6.13
100	7.0 – j10

f MHz	Z_{OL}* Ohms
400	3.78 – j5.75
300	6.75 – j9.51
225	10.6 – j12.80
100	14.5 – j15.5

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

FIGURE 15 — COMMON SOURCE SCATTERING PARAMETERS
50 OHM SYSTEM
V_{DS} = 28 V, I_D = 0.5 A

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
2.0	0.996	-11	34.29	171	0.007	+80	0.730	-12
5.0	0.983	-27	33.00	159	0.016	+73	0.729	-30
10	0.943	-51	31.76	147	0.030	+60	0.728	-57
20	0.871	-86	24.38	130	0.047	+41	0.726	-94
30	0.833	-109	18.82	118	0.054	+30	0.727	-116
40	0.811	-123	14.93	110	0.058	+23	0.728	-129
50	0.796	-133	12.42	105	0.060	+18	0.729	-138
60	0.788	-140	10.45	101	0.061	+14	0.729	-143
70	0.782	-145	9.13	97	0.061	+11	0.729	-148
80	0.779	-149	8.01	94	0.062	+8.9	0.731	-151
90	0.777	-152	7.12	92	0.062	+7.1	0.733	-153
100	0.776	-155	6.48	89	0.062	+5.3	0.735	-155
110	0.775	-157	5.92	87	0.062	+3.9	0.737	-156
120	0.775	-158	5.45	85	0.062	+2.4	0.739	-158
130	0.775	-160	5.03	83	0.062	+1.5	0.741	-159
140	0.775	-161	4.69	81	0.062	+0.4	0.743	-159
150	0.775	-162	4.37	80	0.061	-0.6	0.744	-160
160	0.777	-163	4.10	78	0.062	-1.3	0.746	-161
170	0.777	-163	3.87	77	0.061	-2.2	0.748	-161
180	0.778	-164	3.65	75	0.061	-2.8	0.750	-161
190	0.780	-165	3.46	74	0.061	-3.7	0.753	-162
200	0.781	-165	3.29	72	0.060	-4.2	0.755	-162
225	0.784	-166	2.87	69	0.060	-5.8	0.765	-163
250	0.788	-166	2.57	66	0.059	-7.7	0.770	-163
275	0.790	-167	2.30	64	0.059	-9.0	0.780	-163
300	0.792	-167	2.20	62	0.059	-11	0.795	-163
325	0.794	-168	1.94	57	0.059	-12	0.812	-163
350	0.794	-169	1.78	56	0.058	-15	0.815	-163
375	0.799	-169	1.67	54	0.057	-16	0.826	-163
400	0.805	-169	1.56	51	0.055	-17	0.836	-163
425	0.815	-169	1.45	50	0.054	-17	0.862	-163
450	0.825	-169	1.39	47	0.053	-17	0.860	-162
475	0.834	-170	1.32	45	0.052	-17	0.871	-162
500	0.837	-170	1.23	42	0.051	-16	0.871	-162
525	0.838	-171	1.16	41	0.050	-14	0.872	-162
550	0.843	-171	1.11	39	0.048	-13	0.883	-162
575	0.845	-172	1.07	37	0.048	-12	0.894	-162
600	0.855	-172	1.03	35	0.046	-10	0.901	-163
625	0.856	-173	0.977	33	0.045	-9.0	0.905	-163
650	0.875	-173	0.947	32	0.044	-7.0	0.921	-163
675	0.885	-173	0.914	30	0.044	-5.0	0.938	-163
700	0.888	-174	0.873	27	0.043	-4.0	0.949	-164
725	0.892	-174	0.841	27	0.042	-1.0	0.947	-164
750	0.900	-174	0.821	26	0.043	+2.0	0.970	-164
775	0.910	-175	0.814	24	0.044	+4.0	0.978	-164
800	0.918	-176	0.775	22	0.045	+8.0	0.978	-164

FIGURE 16 — S_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V, I_D = 0.5 A

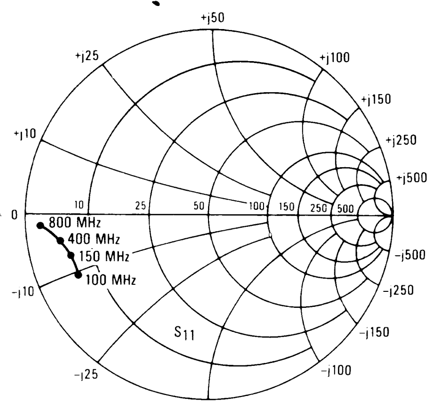


FIGURE 17 — S_{12}, REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V, I_D = 0.5 A

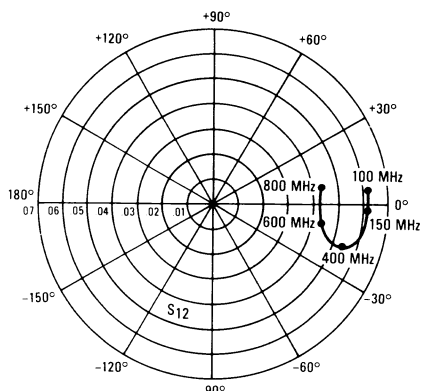


FIGURE 18 — S_{21}, FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} 28 V, I_D 0.5 A

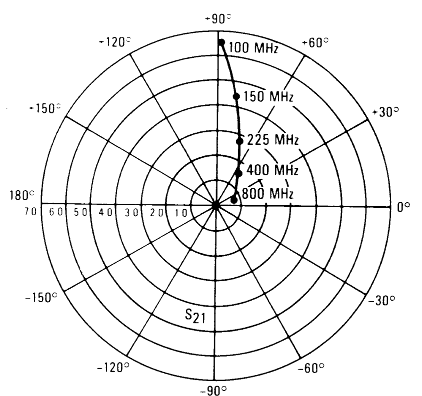
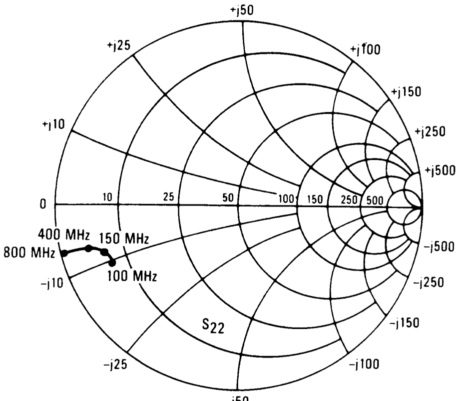


FIGURE 19 — S_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} 28 V, I_D 0.5 A



DESIGN CONSIDERATIONS

The MRF162 is a TMOS RF power N-Channel enhancement mode field-effect transistor (FET) designed especially for UHF power amplifier applications. Motorola TMOS FETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V-groove vertical power FETs.

Motorola Application Note AN-211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of TMOS RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF162 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF162 was characterized at $I_{DQ} = 50$ mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some applications may require a more elaborate bias system.

GAIN CONTROL

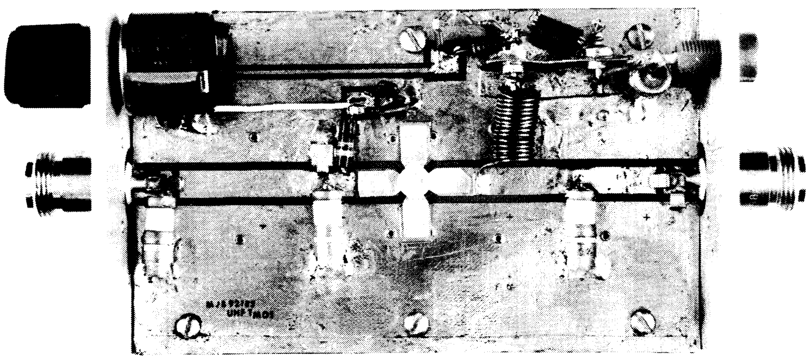
Power output of the MRF162 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC, and modulation systems. (See Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar UHF transistors are suitable for the MRF162. See Motorola Application Note AN-721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of TMOS FETs helps ease the task of broadband network design. Both small signal scattering parameters and large signal impedances are provided. While the s-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of TMOS power FETs.

RF power FETs are triode devices and, therefore, not unilateral. This, coupled with the very high gain of the MRF162, yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. Two port parameter stability analysis with the MRF162 s-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN-215A for a discussion of two port network theory and stability.

FIGURE 20 — 400 MHz TEST CIRCUIT



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MRF163

The RF Line

25 W 2.0–400 MHz

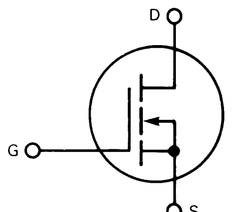
N-CHANNEL TMOS
BROADBAND RF POWER

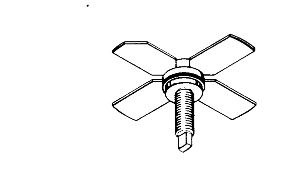
FET

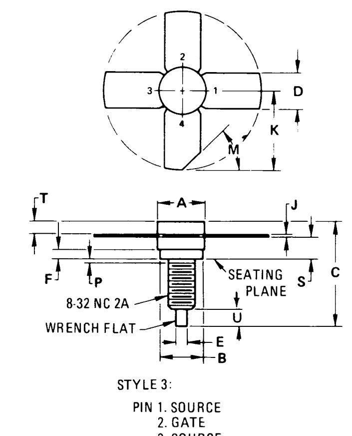
N-CHANNEL ENHANCEMENT-MODE TMOS RF POWER FIELD-EFFECT TRANSISTOR

. . . designed for wideband large-signal output and driver applications in the 2.0 to 400 MHz range.

- Guaranteed 28 Volt, 400 MHz Performance
  Output Power = 25 Watts
  Minimum Gain = 10 dB
  Efficiency = 50% (Typical)
- Small-Signal and Large-Signal Characterization
- 100% Tested for Load Mismatch At All Phase Angles With 30:1 VSWR
- Low Noise Figure — 2.5 dB (Typ) at 500 mA, 400 MHz
- Excellent Thermal Stability, Ideally Suited For Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques







STYLE 3:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	14.99	16.51	0.590	0.650
D	5.46	5.96	0.215	0.235
E	1.40	1.65	0.055	0.065
F	1.52	–	0.060	–
J	0.08	0.17	0.003	0.007
K	11.05	–	0.435	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
S	3.00	3.25	0.118	0.128
T	1.40	1.78	0.055	0.070
U	2.92	3.68	0.115	0.145

CASE 244-04

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	5.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	87.5 0.500	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

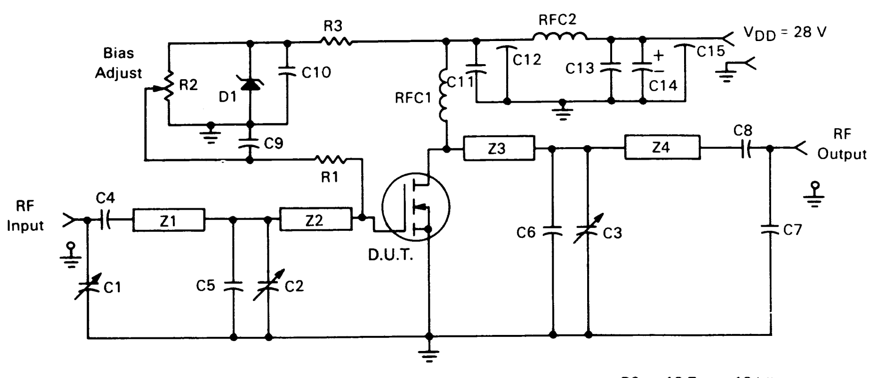
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	4.0	mAdc
Gate-Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 25 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 500 mA)	g_{fs}	500	750	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	48	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	54	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	11	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 1)					
Noise Figure (V_{DS} = 28 Vdc, I_D = 500 mA, f = 400 MHz, Z_S = 3.23 + j2.57 Ω, Z_L = 2.11 + j2.97 Ω)	NF	—	2.5	—	dB
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 25 W, f = 400 MHz, I_{DQ} = 25 mA)	G_{ps}	10	12	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 25 W, f = 400 MHz, I_{DQ} = 25 mA)	η	45	50	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 25 W, f = 400 MHz, I_{DQ} = 25 mA, VSWR 30:1 at All Phase Angles)	ψ	No Degradation in Output Power			

FIGURE 1 — 400 MHz TEST CIRCUIT



C1, C2, C3 — 1-20 pF Johanson or Equivalent
C4, C8 — 270 pF, 100 Mil Chip Cap
C5, C6 — 18 pF Mini-Unleco or Equivalent
C7 — 12 pF Mini-Unleco or Equivalent
C9 — 0.01 μF, 50 V Disc Ceramic
C10, C11, C13 — 0.1 μF, 50 V Disc Ceramic
C12, C15 — 680 pF Feedthru
C14 — 20 μF, 50 V
D1 — 1N5925A Motorola Zener
R1 — 10 kΩ, 1/4 W
R2 — 10 Turns 10 kΩ
R3 — 1.6 kΩ, 1/4 W
RFC1 — 10 Turns, 0.300″ ID #20 AWG Enamel Closewound
RFC2 — Ferroxcube VK-200 — 19/4B
Z1 — 1.350″ × 0.250″ Microstrip
Z2 — 0.600″ × 0.250″ Microstrip
Z3 — 0.710″ × 0.250″ Microstrip
Z4 — 1.300″ × 0.250″ Microstrip
Board — Glass Teflon, 62 Mils, ϵ_r = 2.56

FIGURE 2 — OUTPUT POWER versus INPUT POWER

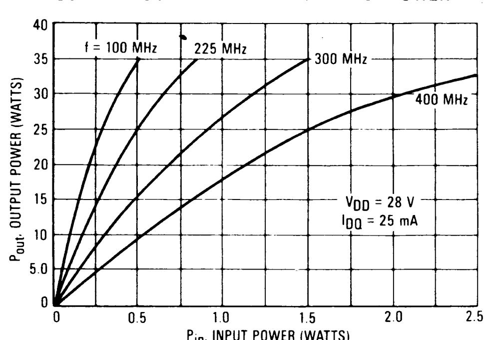


FIGURE 3 — OUTPUT POWER versus INPUT POWER

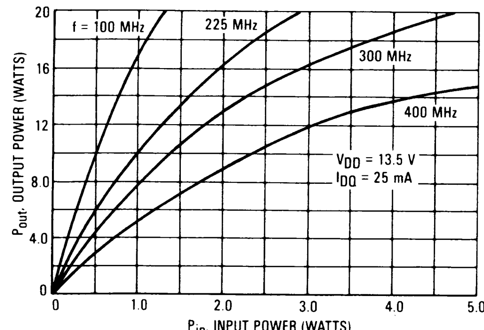


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 400 MHz

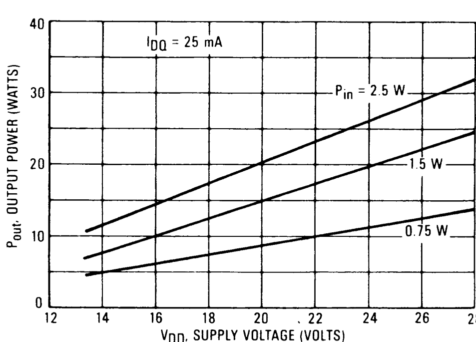


FIGURE 5 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 300 MHz

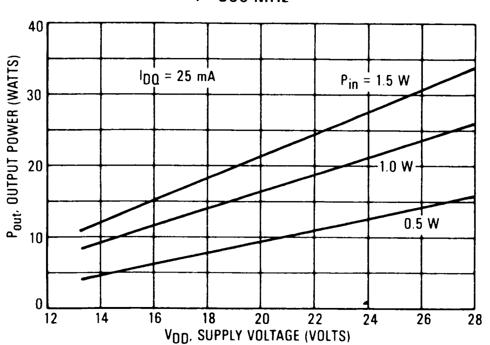


FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 225 MHz

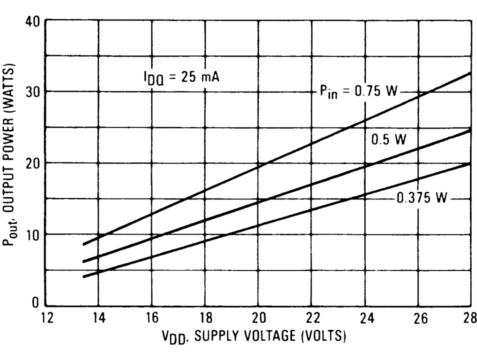


FIGURE 7 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 100 MHz

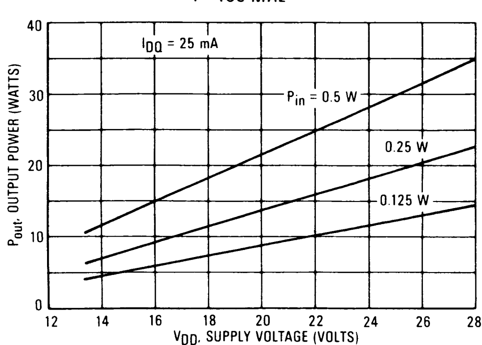


FIGURE 8 — OUTPUT POWER versus GATE VOLTAGE

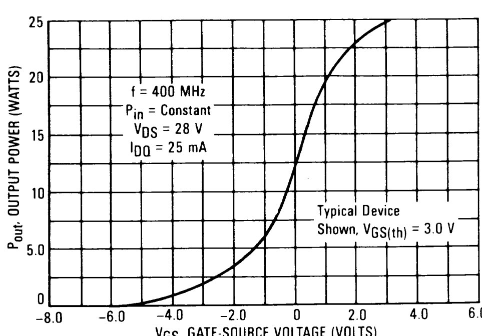


FIGURE 9 — DRAIN CURRENT versus GATE VOLTAGE (TRANSFER CHARACTERISTICS)

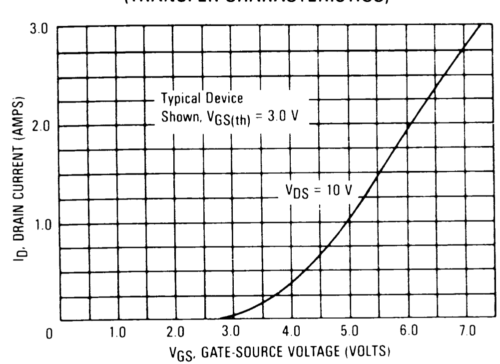


FIGURE 10 — GATE-SOURCE VOLTAGE versus CASE TEMPERATURE

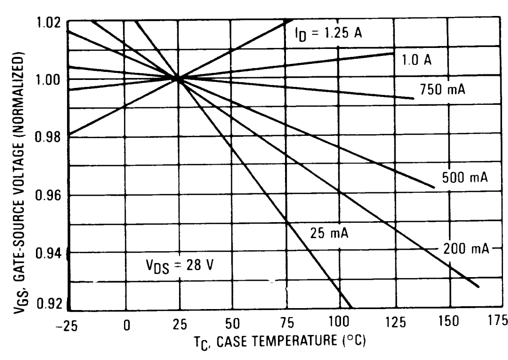


FIGURE 11 — CAPACITANCE versus DRAIN-SOURCE VOLTAGE

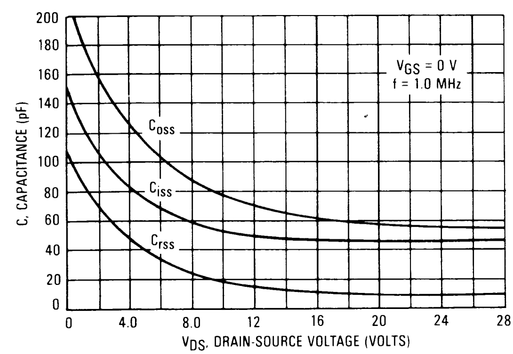


FIGURE 12 — DC SAFE OPERATING AREA

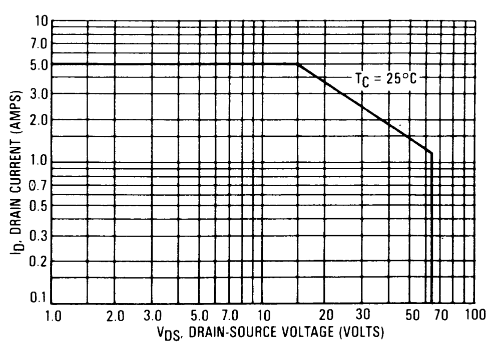
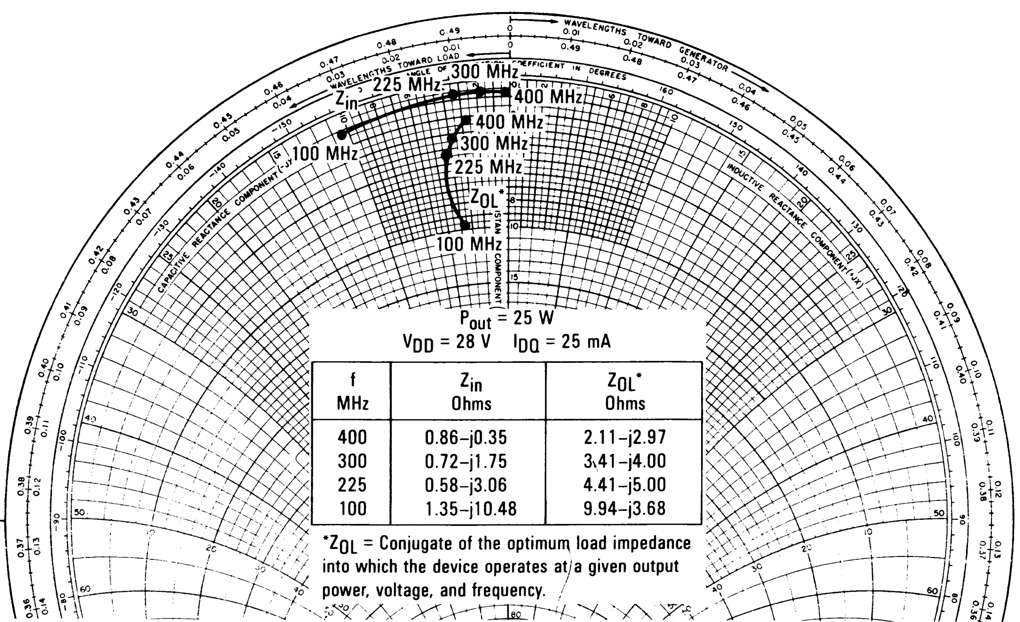


FIGURE 13 — INPUT AND OUTPUT IMPEDANCE



P_{out} = 25 W
V_{DD} = 28 V I_{DQ} = 25 mA

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
400	0.86–j0.35	2.11–j2.97
300	0.72–j1.75	3.41–j4.00
225	0.58–j3.06	4.41–j5.00
100	1.35–j10.48	9.94–j3.68

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

FIGURE 14 — COMMON SOURCE SCATTERING PARAMETERS
50 OHM SYSTEM
V_{DS} = 28 V, I_D = 0.5 A

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠φ	$\|S_{21}\|$	∠φ	$\|S_{12}\|$	∠φ	$\|S_{22}\|$	∠φ
2.0	0.985	-30	56.97	166	0.010	+63.9	0.611	-36
10	0.875	-105	34.12	125	0.032	+30.6	0.736	-116
25	0.841	-145	16.17	104	0.038	+9.2	0.798	-152
50	0.833	-162	8.201	92.7	0.038	+1.6	0.800	-165
75	0.836	-167	5.496	86.8	0.037	-2.5	0.802	-168
100	0.838	-170	4.121	82.3	0.039	-3.0	0.804	-170
125	0.838	-171	3.255	78.6	0.039	-5.8	0.809	-170
150	0.840	-172	2.718	74.3	0.037	-8.5	0.815	-171
175	0.844	-173	2.326	70.8	0.037	-9.6	0.819	-171
200	0.849	-173	2.027	67.2	0.036	-10.4	0.824	-171
225	0.851	-173	1.782	64.0	0.036	-10.3	0.833	-171
250	0.857	-173	1.593	60.9	0.034	-11.7	0.839	-171
275	0.862	-173	1.438	58.9	0.035	-11.1	0.844	-171
300	0.866	-173	1.319	55.6	0.033	-12.1	0.846	-170
325	0.872	-173	1.209	52.3	0.032	-12.7	0.861	-170
350	0.875	-173	1.110	49.0	0.031	-13.4	0.873	-170
375	0.879	-173	1.030	46.7	0.031	-12.2	0.876	-170
400	0.882	-173	0.966	44.1	0.030	-14.6	0.883	-170
425	0.888	-173	0.904	41.3	0.029	-13.4	0.888	-170
450	0.891	-173	0.836	39.4	0.028	-11.7	0.895	-170
475	0.893	-173	0.792	37.1	0.027	-8.8	0.902	-170
500	0.901	-173	0.748	35.2	0.027	-6.1	0.911	-170
525	0.906	-173	0.715	32.4	0.025	-6.0	0.921	-170
550	0.911	-173	0.679	30.2	0.024	-6.0	0.928	-170
575	0.912	-173	0.637	28.7	0.024	-3.9	0.934	-170
600	0.913	-173	0.605	26.9	0.024	-1.0	0.939	-170
625	0.919	-174	0.579	25.3	0.024	+1.0	0.947	-170
650	0.921	-174	0.566	23.0	0.025	+10.1	0.961	-170
675	0.927	-174	0.540	22.6	0.025	+12.1	0.963	-170
700	0.927	-174	0.510	19.9	0.025	+16.5	0.966	-170
725	0.927	-173	0.485	19.5	0.025	+23.1	0.967	-170
750	0.933	-174	0.481	17.4	0.026	+25.3	0.967	-170
775	0.937	-174	0.453	17.2	0.028	+28.0	0.976	-170
800	0.942	-174	0.448	16.8	0.030	+33.8	0.976	-170

FIGURE 15 — S_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V, I_D = 0.5 A

800 MHz
400 MHz
100 MHz
S_{11}

FIGURE 16 — S_{12}, REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V, I_D = 0.5 A

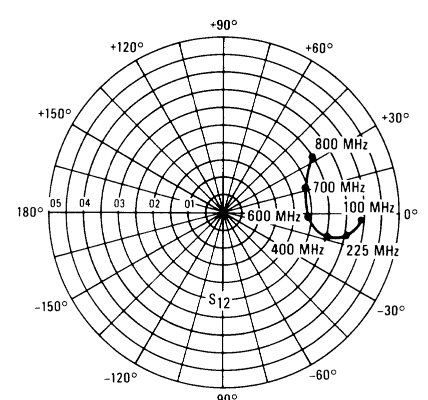


FIGURE 17 — S_{21}, FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V, I_D = 0.5 A

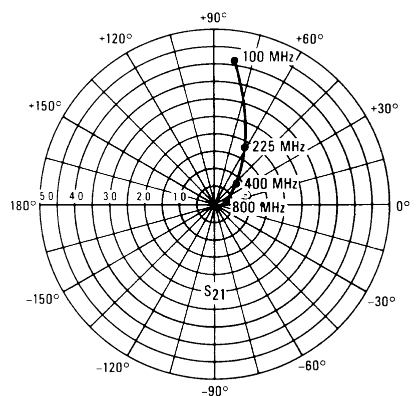
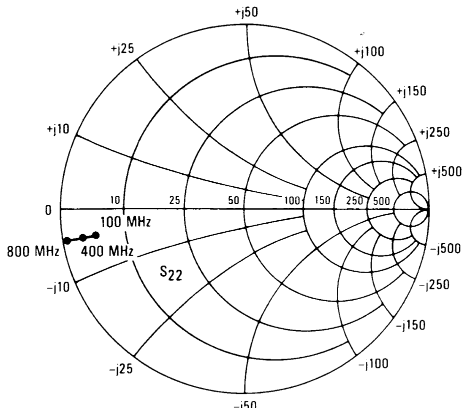


FIGURE 18 — S_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V, I_D = 0.5 A



DESIGN CONSIDERATIONS

The MRF163 is a TMOS RF power N-Channel enhancement mode field-effect transistor (FET) designed especially for UHF power amplifier applications. Motorola TMOS FETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V-groove vertical power FETs.

Motorola Application Note AN-211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of TMOS RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF163 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF163 was characterized at I_{DQ} = 25 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some applications may require a more elaborate bias system.

GAIN CONTROL

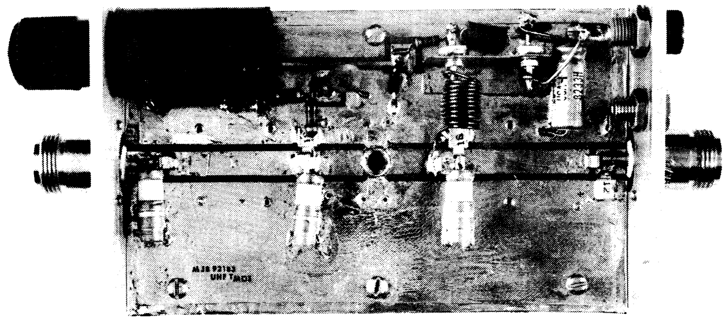
Power output of the MRF163 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC, and modulation systems. (See Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar UHF transistors are suitable for the MRF163. See Motorola Application Note AN-721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of TMOS FETs helps ease the task of broadband network design. Both small signal scattering parameters and large signal impedances are provided. While the s-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of TMOS power FETs.

RF power FETs are triode devices and, therefore, not unilateral. This, coupled with the very high gain of the MRF163, yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. Two port parameter stability analysis with the MRF163 s-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN-215A for a discussion of two port network theory and stability.

FIGURE 19 — 400 MHz TEST CIRCUIT



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MRF171

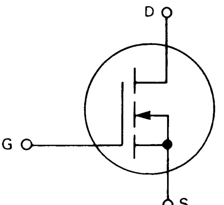
The RF TMOS Line

N-CHANNEL ENHANCEMENT-MODE TMOS RF POWER FIELD-EFFECT TRANSISTOR

. . . designed primarily for wideband large-signal output and driver stages in the 2.0–200 MHz frequency range.

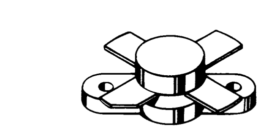
- Guaranteed Performance at 150 MHz, 28 Vdc

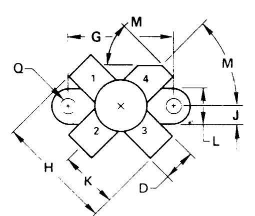
  Output Power = 45 Watts
  Minimum Gain = 12 dB
  Efficiency = 50% (Min)
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Excellent Thermal Stability, Ideally Suited for Class A Operation
- Low Noise Figure — 1.5 dB Typ at 1.0 A, 150 MHz



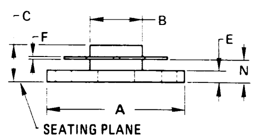
45 W 2.0–200 MHz

N-CHANNEL TMOS BROADBAND RF POWER FET





STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.29	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

CASE 211-07

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Drain-Gate Voltage	V_{DGR}*	65	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	4.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.66	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	°C/W

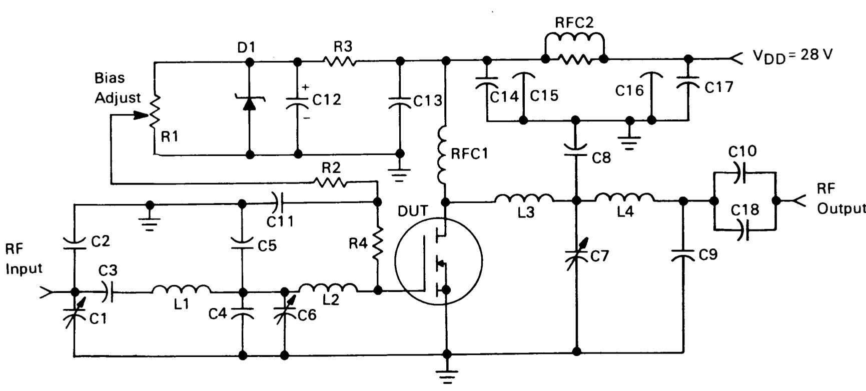
*R_{GS} = 1.0 MΩ

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate-Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 25 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 1.0 A)	g_{fs}	0.7	1.1	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	55	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	70	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	14	—	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure (V_{DS} = 28 Vdc, I_D = 1.0 A, f = 150 MHz)	NF	—	1.5	—	dB
Common Source Power Gain (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 45 W, f = 150 MHz, I_{DQ} = 25 mA)	G_{ps}	12	15	—	dB
Drain Efficiency (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 45 W, f = 150 MHz, I_{DQ} = 25 mA)	η	50	60	—	%
Electrical Ruggedness (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 45 W, f = 150 MHz, I_{DQ} = 25 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			

FIGURE 1 — 150 MHz TEST CIRCUIT



C1, C6, C7 — 1.0-20 pF Johanson
C2, C4, C5, C8 — 63 pF ATC Chip (100 mils)
C3, C10, C18 — 680 pF ATC Chip (100 mils)
C9 — 12 pF ATC Chip (100 mils)
C11, C13, C14, C17 — 0.1 μF Erie Redcap, 50 V
C12 — 25 μF, 50 V
C15, C16 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener
L1 — 2 Turns, #18 AWG, 0.3″ ID, 0.3″ Long
L2 — 1-1/4 Turns, #18 AWG, 0.21″ ID
L3 — 1-1/4 Turns, #18 AWG, 0.21″ ID
L4 — 2 Turns, #18 AWG, 0.23″ ID, 0.15″ Long
RFC1 — 20 Turns, #20 AWG Enameled, 0.3″ ID, Close Wound
RFC2 — 15 Turns, #20 AWG Enameled on 2.0 W, 10 Ω Resistor
R1 — 10 kΩ, 10 Turns Helipot 7216-R10K-L.25
R2 — 10 kΩ, 1/4 W
R3 — 1.8 kΩ, 1/2 W
R4 — 47 Ω, 1/2 W

FIGURE 2 — OUTPUT POWER versus INPUT POWER

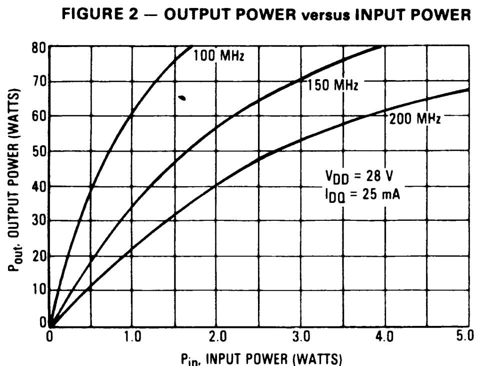


FIGURE 3 — OUTPUT POWER versus INPUT POWER

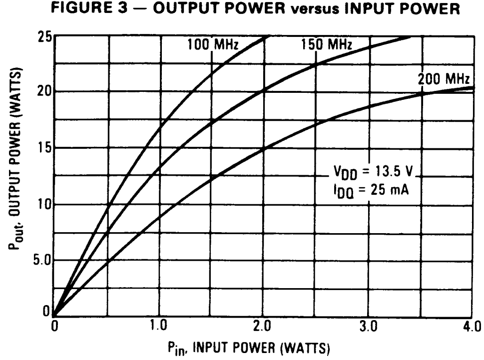


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 100 MHz

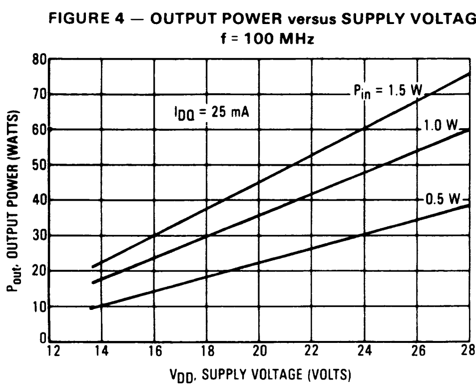


FIGURE 5 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 150 MHz

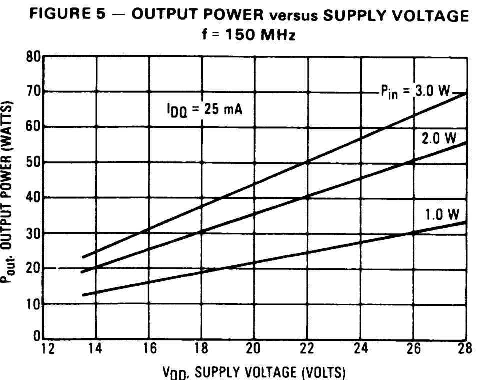


FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 200 MHz

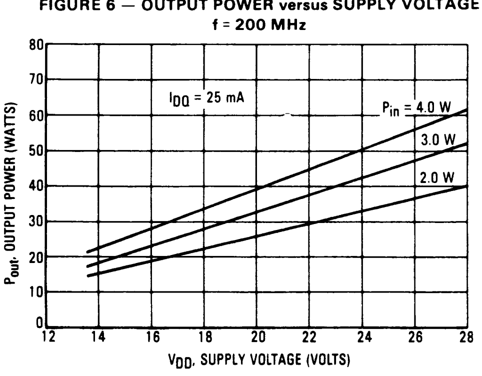
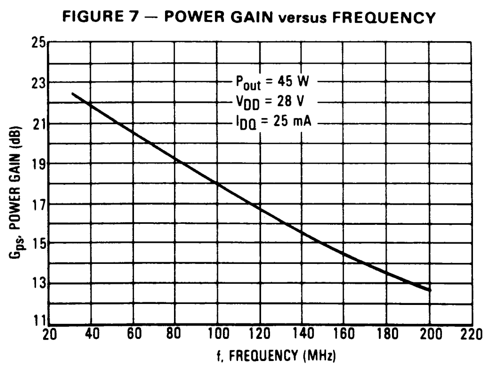


FIGURE 7 — POWER GAIN versus FREQUENCY



3

FIGURE 8 — OUTPUT POWER versus GATE VOLTAGE

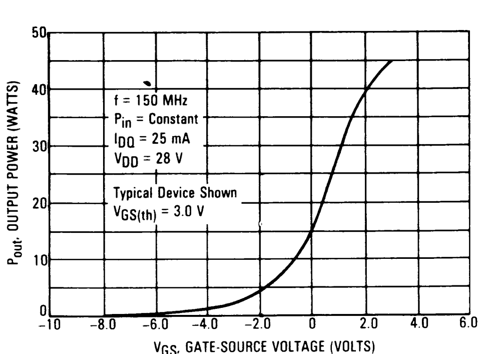


FIGURE 9 — DRAIN CURRENT versus GATE VOLTAGE (TRANSFER CHARACTERISTICS)

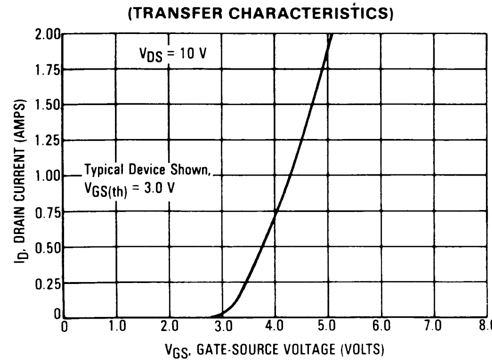


FIGURE 10 — GATE-SOURCE VOLTAGE versus CASE TEMPERATURE

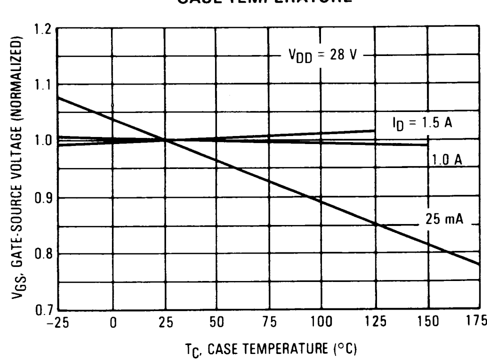


FIGURE 11 — CAPACITANCE versus DRAIN VOLTAGE

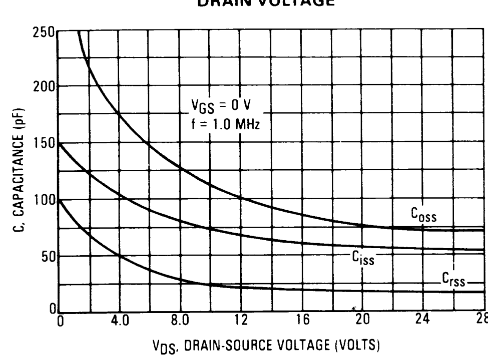


FIGURE 12 — DC SAFE OPERATING AREA

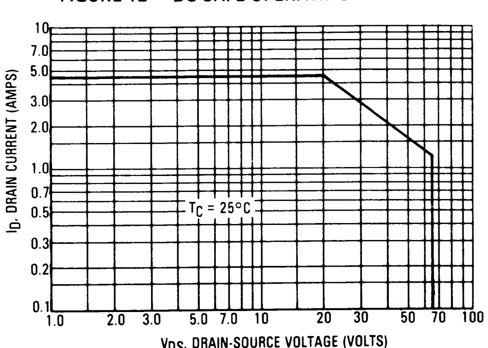


FIGURE 13 — COMMON SOURCE SCATTERING PARAMETERS
V_{DS} = 28 V, I_D = 0.5 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
2.0	0.966	-50	72.4	153	0.014	63	0.674	-59
5.0	0.891	-97	50.8	128	0.025	39	0.757	-109
10	0.841	-132	30.1	110	0.030	23	0.801	-141
20	0.821	-155	15.9	99	0.032	14	0.818	-160
30	0.817	-162	10.7	93	0.032	11	0.822	-166
40	0.816	-167	8.06	90	0.032	10	0.823	-169
50	0.816	-169	6.45	88	0.032	11	0.825	-171
60	0.816	-171	5.37	85	0.032	11	0.826	-172
70	0.816	-172	4.60	84	0.032	12	0.828	-173
80	0.816	-172	4.01	82	0.032	13	0.829	-174
90	0.816	-173	3.56	80	0.033	14	0.830	-174
100	0.816	-173	3.15	77	0.034	15	0.832	-174
110	0.816	-173	2.85	76	0.035	16	0.832	-175
120	0.816	-173	2.59	75	0.036	18	0.832	-175
130	0.817	-174	2.40	74	0.036	19	0.832	-175
140	0.817	-174	2.23	72	0.037	20	0.834	-175
150	0.820	-174	2.09	71	0.037	21	0.835	-175
160	0.823	-174	1.97	70	0.037	22	0.836	-175
170	0.825	-175	1.85	69	0.037	23	0.839	-175
180	0.826	-175	1.75	68	0.037	25	0.840	-175
190	0.829	-175	1.66	67	0.037	26	0.843	-175
200	0.832	-175	1.59	66	0.038	27	0.845	-175
250	0.844	-176	1.24	61	0.039	37	0.856	-175
300	0.855	-176	1.02	55	0.042	45	0.867	-174
350	0.862	-177	0.88	51	0.047	53	0.878	-174
400	0.868	-178	0.76	48	0.052	59	0.885	-174
450	0.873	-179	0.67	45	0.059	64	0.897	-174
500	0.907	+179	0.63	42	0.067	67	0.892	-175

3

FIGURE 14 — S_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 0.5 A

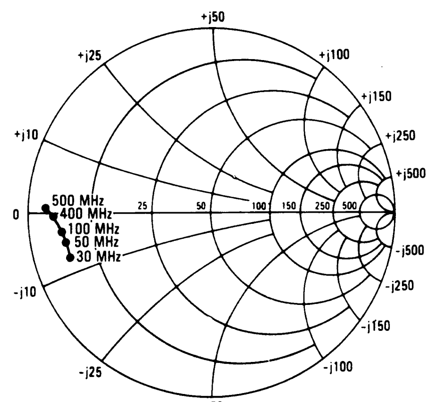
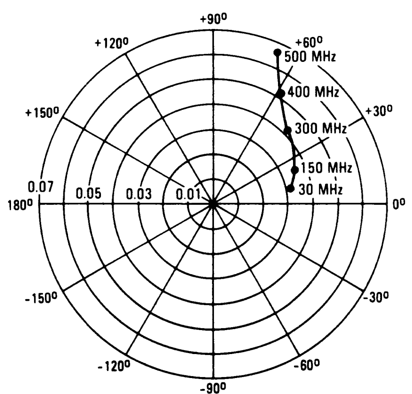


FIGURE 15 — S_{12}, REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 0.5 A



3

FIGURE 16 — S_{21}, FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 0.5 A

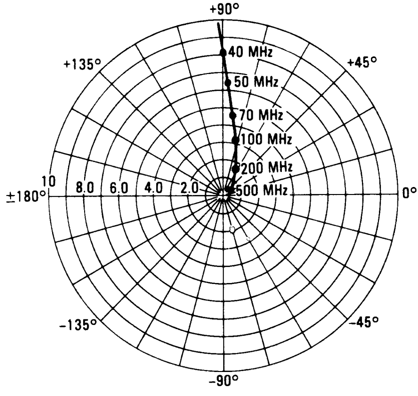
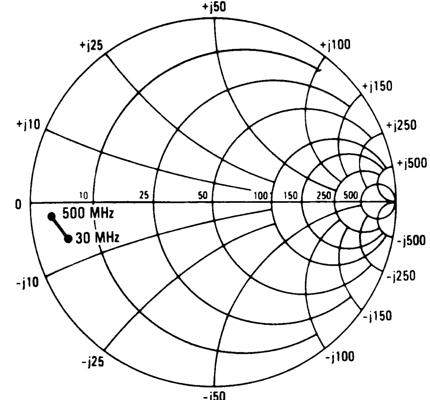


FIGURE 17 — S_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 0.5 A



DESIGN CONSIDERATIONS

The MRF171 is a TMOS RF power N-Channel enhancement mode field-effect transistor (FET) designed especially for VHF power amplifier and oscillator applications. Motorola TMOS FETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with "V-groove" vertical power FETs.

Motorola Application Note AN-211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of TMOS RF power FETs include high-gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF171 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF171 was characterized at I_{DQ} = 25 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF171 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC, and modulation systems. (See Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar VHF transistors are suitable for MRF171. See Motorola Application Note AN-721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of TMOS FETs helps ease the task of broadband network design. Both small-signal scattering parameters and large-signal impedances are provided. While the s-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of TMOS power FETs.

RF power FETs are triode devices and, therefore, not unilateral. This, coupled with the very high gain of the MRF171, yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The MRF171 was characterized with a 47-ohm input shunt loading resistor. Two port parameter stability analysis with the MRF 171 s-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN-215A for a discussion of two-port network theory and stability.

Input resistive loading is not feasible in low noise applications. The MRF171 noise figure data was generated in a circuit with drain loading and a low loss input network.

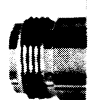
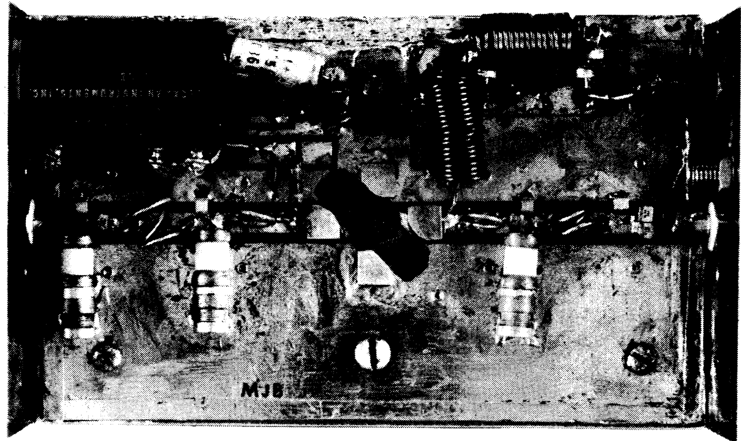
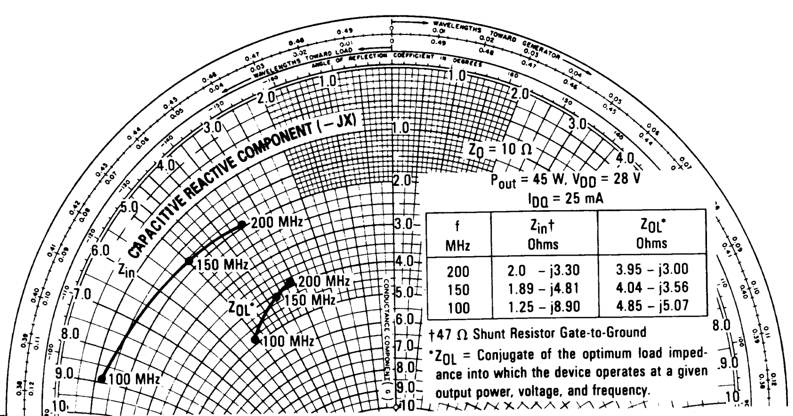



FIGURE 18 — 150 MHz TEST CIRCUIT

FIGURE 19 — LARGE-SIGNAL SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE



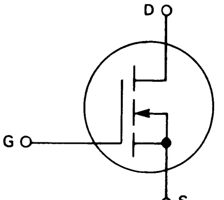
MRF172

The RF TMOS Line

N-CHANNEL ENHANCEMENT-MODE TMOS RF POWER FIELD-EFFECT TRANSISTOR

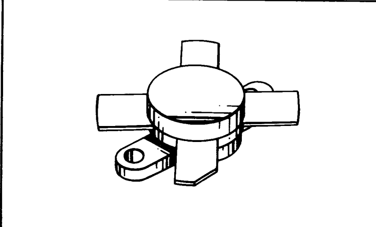
. . . designed primarily for wideband large-signal output and driver stages in the 2.0–200 MHz frequency range.

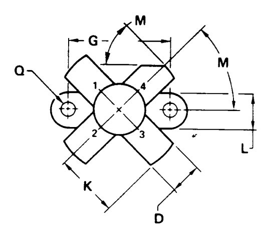
- Guaranteed Performance at 150 MHz, 28 Vdc
  Output Power = 80 Watts
  Minimum Gain = 10 dB
  Efficiency = 50% (Min)
- Excellent Thermal Stability, Ideally Suited for Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Low Noise Figure— 1.5 dB Typ at 2.0 A, 150 MHz

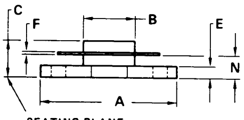


80 W 2.0-200 MHz

N-CHANNEL TMOS BROADBAND RF POWER FET







STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	11.81	12.95	0.465	0.510
C	5.82	6.98	0.229	0.275
D	5.46	5.97	0.216	0.235
E	2.13	2.79	0.084	0.110
F	0.08	0.18	0.003	0.007
G	18.29	18.54	0.720	0.730
K	11.05	–	0.435	–
L	6.22	6.48	0.246	0.255
M	45° NOM		45° NOM	
N	3.66	4.52	0.144	0.178
Q	2.92	3.30	0.115	0.130

CASE 211-11

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain — Source Voltage	V_{DSS}	65	Vdc
Drain — Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate — Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	9.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	220 1.26	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

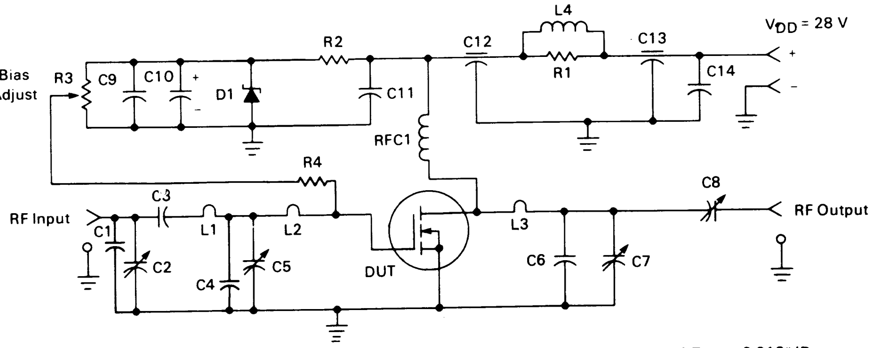
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.80	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 50 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate-Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 50 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.0 A)	g_{fs}	1.2	1.8	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	100	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	135	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	26	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 1)					
Noise Figure (V_{DD} = 28 Vdc, I_D = 2.0 A, f = 150 MHz)	NF	—	1.5	—	dB
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA)	G_{ps}	10	12.3	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA)	η	50	60	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			

FIGURE 1 — 150 MHz TEST CIRCUIT



C1 — 25 pF Unleco
C2, C5, C7 — Arco 462, 5-80 pF
C3 — 100 pF Unleco
C4 — 40 pF Unleco
C6 — 60 pF Unleco
C8 — Arco 463, 9-180 pF
C9, C11, C14 — 0.1 μF Erie Redcap
C10 — 50 μF, 50 V
C12, C13 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener

L1 — #16 AWG, 1-1/4 Turns, 0.213″ ID
L2 — #16 AWG, Hairpin 0.25″ 0.062″
L3 — #14 AWG, Hairpin 0.47″ 0.2″
L4 — 10 Turns #16 AWG Enameled Wire on R1
RFC1 — 18 Turns #16 AWG Enameled Wire, 0.3″ ID
R1 — 10 Ω, 2.0 W
R2 — 1.8 kΩ, 1/2 W
R3 — 10 kΩ, 10 Turn Bourns
R4 — 10 kΩ, 1/4 W

FIGURE 2 — OUTPUT POWER versus INPUT POWER

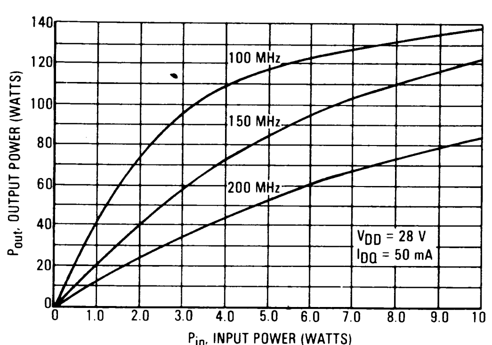


FIGURE 3 — OUTPUT POWER versus INPUT POWER

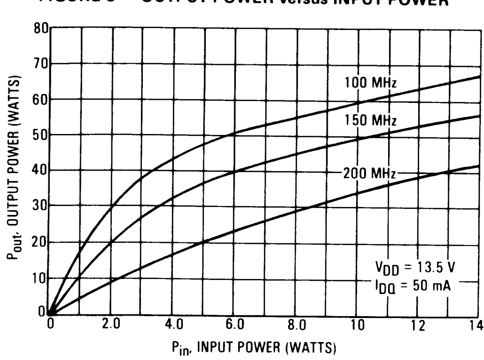


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 100 MHz

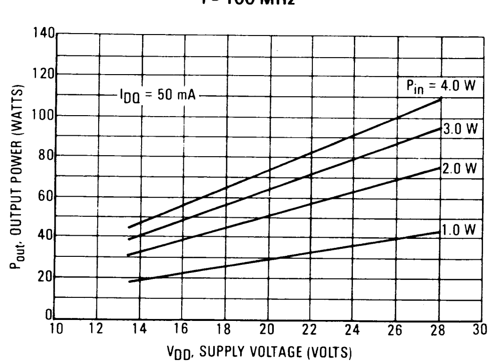


FIGURE 5 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 150 MHz

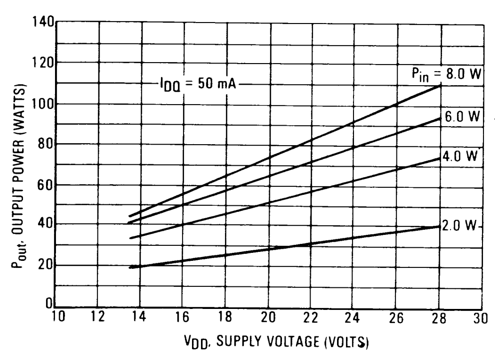


FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 200 MHz

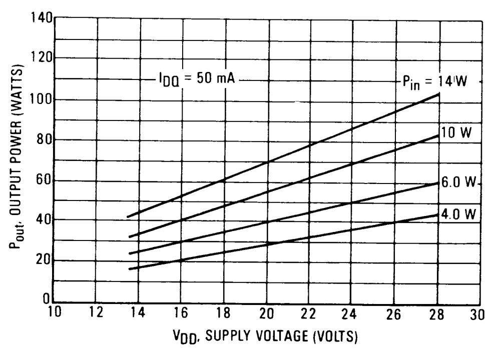
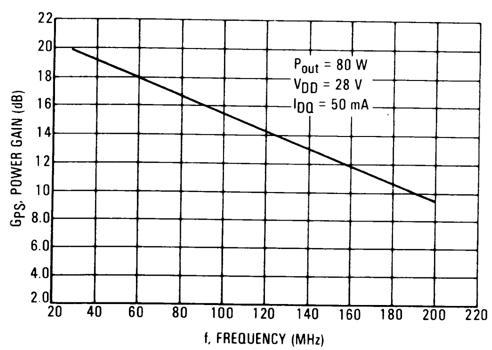


FIGURE 7 — POWER GAIN versus FREQUENCY



3

FIGURE 8 — OUTPUT POWER versus GATE VOLTAGE

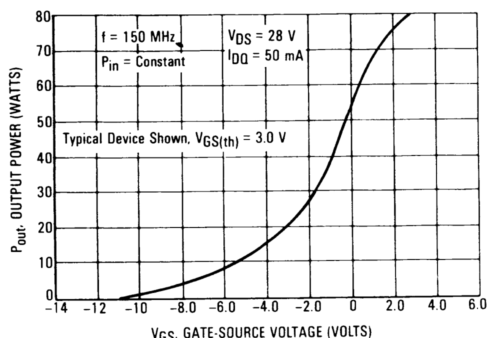


FIGURE 9 — DRAIN CURRENT versus GATE VOLTAGE (TRANSFER CHARACTERISTICS)

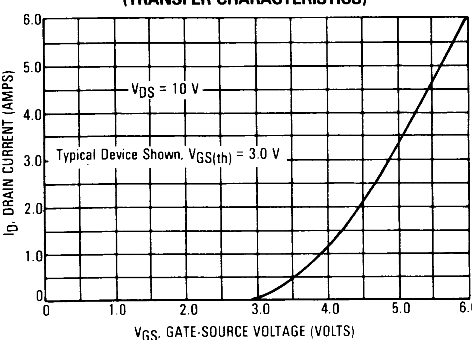


FIGURE 10 — GATE-SOURCE VOLTAGE versus CASE TEMPERATURE

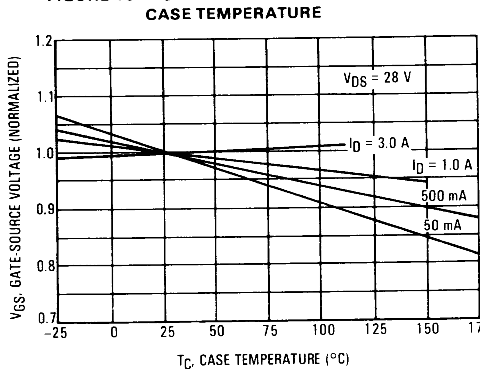


FIGURE 11 — CAPACITANCE versus DRAIN VOLTAGE

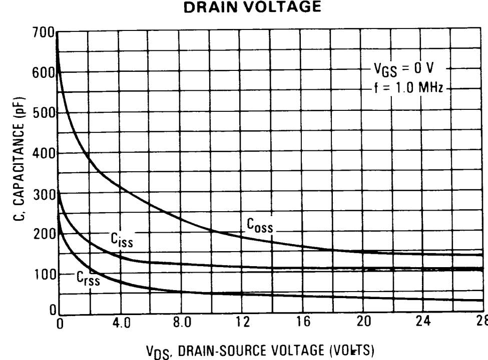


FIGURE 12 — DC SAFE OPERATING AREA

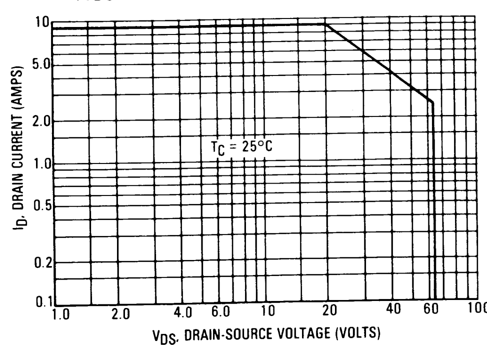


FIGURE 13 — COMMON SOURCE SCATTERING PARAMETERS
V_{DS} = 28 V, I_D = 2.0 A

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
2.0	0.928	-112	87.5	122	0.013	34	0.776	-128
5.0	0.902	-149	40.5	104	0.015	17	0.857	-158
10	0.897	-164	20.7	96	0.016	12	0.872	-169
20	0.896	-172	10.4	90	0.016	13	0.876	-174
30	0.896	-175	6.94	88	0.016	17	0.877	-176
40	0.896	-176	5.20	85	0.017	21	0.878	-177
50	0.897	-177	4.15	83	0.017	25	0.879	-177
60	0.897	-177	3.45	82	0.017	29	0.880	-177
70	0.898	-178	2.95	80	0.018	33	0.881	-177
80	0.899	-178	2.57	78	0.019	37	0.882	-177
90	0.901	-178	2.27	76	0.020	40	0.883	-177
100	0.903	-178	2.00	74	0.021	42	0.885	-177
110	0.905	-178	1.80	73	0.022	44	0.887	-177
120	0.907	-178	1.62	71	0.024	45	0.888	-177
130	0.908	-178	1.51	70	0.026	47	0.895	-177
140	0.909	-178	1.39	70	0.027	49	0.895	-177
150	0.910	-178	1.30	69	0.028	51	0.895	-177
160	0.911	-178	1.22	68	0.029	51	0.897	-177
170	0.912	-179	1.14	66	0.030	52	0.899	-177
180	0.921	-179	1.08	65	0.032	54	0.900	-177
190	0.921	-179	1.01	64	0.033	55	0.903	-177
200	0.922	-179	0.974	63	0.035	56	0.905	-177
210	0.920	-179	0.928	61	0.036	58	0.907	-176
220	0.915	-179	0.872	60	0.038	59	0.907	-176
230	0.915	-179	0.828	60	0.040	60	0.914	-176
240	0.917	-179	0.793	59	0.042	61	0.917	-176
250	0.922	-179	0.772	59	0.044	62	0.918	-176
260	0.927	+179	0.744	57	0.046	62	0.920	-176
270	0.928	+179	0.714	57	0.048	63	0.920	-176
280	0.929	+179	0.689	56	0.049	64	0.923	-176
290	0.929	+179	0.662	55	0.051	65	0.923	-176
300	0.938	+179	0.642	55	0.053	65	0.923	-176

FIGURE 14 — S_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 2.0 A

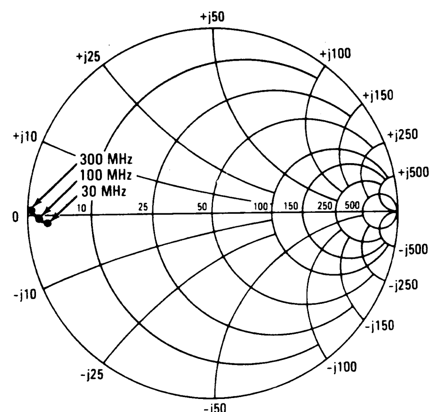


FIGURE 15 — S_{12}, REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 2.0 A

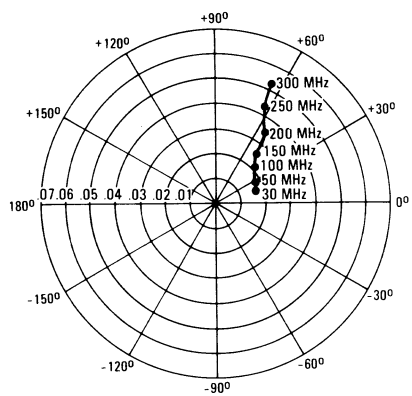


FIGURE 16 — S_{21}, FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 2.0 A

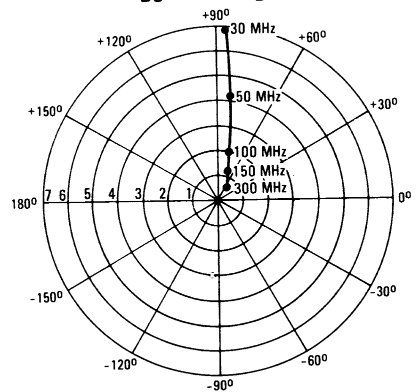
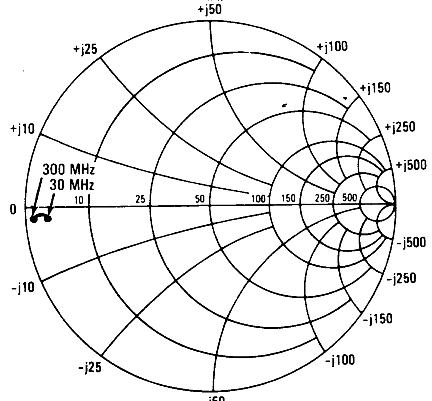


FIGURE 17 — S_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 2.0 A



DESIGN CONSIDERATIONS

The MRF172 is a TMOS RF power N-channel enhancement mode field-effect transistor (FET) designed for VHF power amplifier applications. Motorola TMOS FETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V-groove MOS power FETs.

Motorola Application Note AN-211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of TMOS RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF172 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF172 was characterized at I_{DQ} = 50 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF172 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC, and modulation systems. (See Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar VHF transistors are suitable for MRF172. See Motorola Application Note AN-721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of TMOS FETs helps ease the task of broadband network design. Both small-signal scattering parameters and large-signal impedances are provided. While the s-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of TMOS power FETs.

FIGURE 18 — 150 MHz TEST CIRCUIT

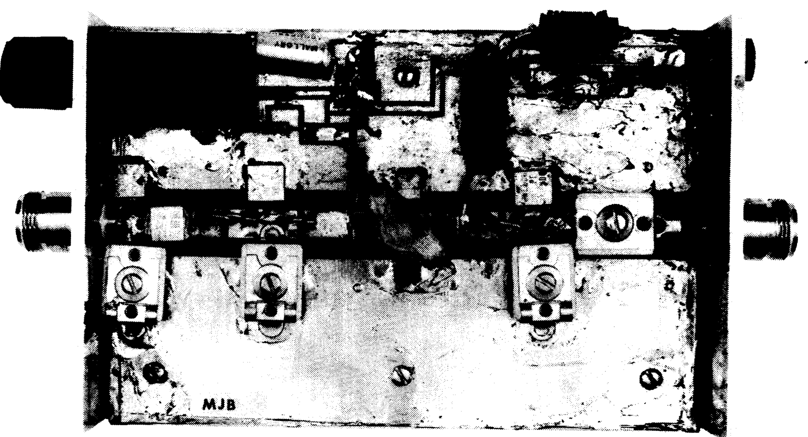


FIGURE 19 — SERIES EQUIVALENT INPUT IMPEDANCE, Z_{in}

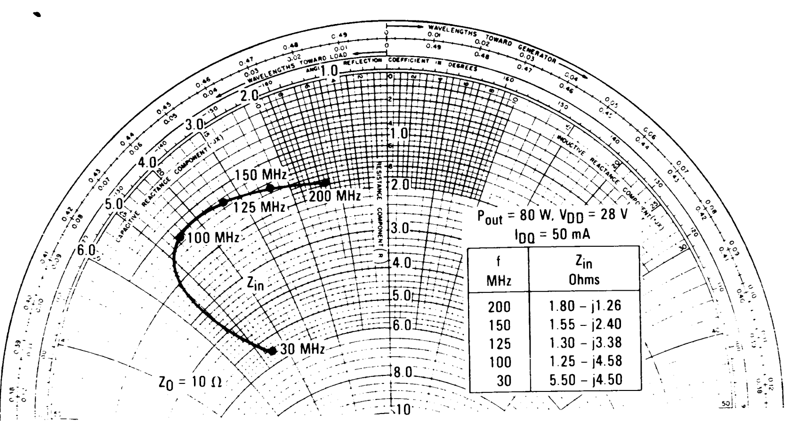
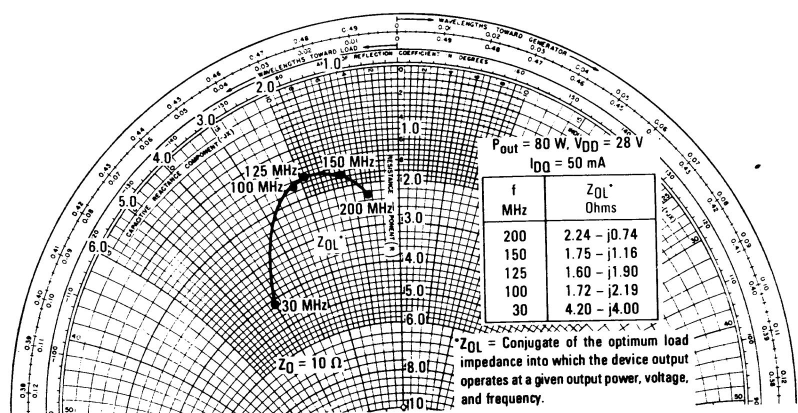


FIGURE 20 — SERIES EQUIVALENT OUTPUT IMPEDANCE, Z_{OL}*



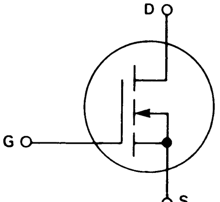
MRF174

The RF TMOS Line

N-CHANNEL ENHANCEMENT-MODE TMOS RF POWER FIELD-EFFECT TRANSISTOR

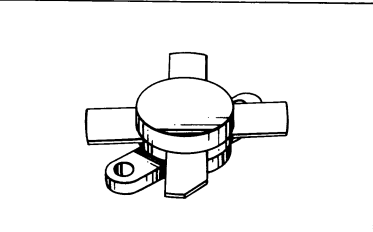
. . . designed primarily for wideband large-signal output and driver stages in the 2.0–200 MHz frequency range.

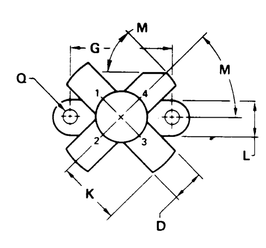
- Guaranteed Performance at 150 MHz, 28 Vdc
  Output Power = 125 Watts
  Minimum Gain = 9.0 dB
  Efficiency = 50% (Min)
- Excellent Thermal Stability, Ideally Suited for Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Low Noise Figure — 3.0 dB Typ at 2.0 A, 150 MHz

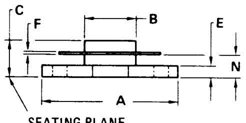


125 W 2.0–200 MHz

N-CHANNEL TMOS BROADBAND RF POWER FET







SEATING PLANE

STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	11.81	12.95	0.465	0.510
C	5.82	6.98	0.229	0.275
D	5.46	5.97	0.216	0.235
E	2.13	2.79	0.084	0.110
F	0.08	0.18	0.003	0.007
G	18.29	18.54	0.720	0.730
K	11.05	–	0.435	–
L	6.22	6.48	0.246	0.255
M	45° NOM		45° NOM	
N	3.66	4.52	0.144	0.178
Q	2.92	3.30	0.115	0.130

CASE 211-11

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain — Source Voltage	V_{DSS}	65	Vdc
Drain — Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate — Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	13	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

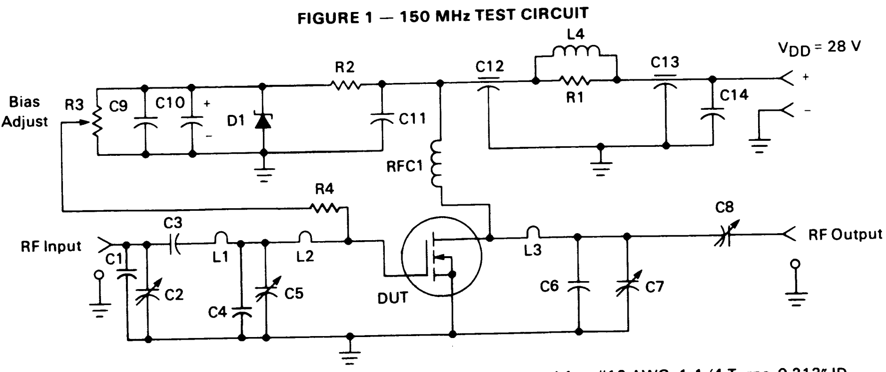
Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 50 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	10	mAdc
Gate-Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 3.0 A)	g_{fs}	1.75	2.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	175	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	230	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	40	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 1)					
Noise Figure (V_{DD} = 28 Vdc, I_D = 2.0 A, f = 150 MHz)	NF	—	3.0	—	dB
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 125 W, f = 150 MHz, I_{DQ} = 100 mA)	G_{ps}	9.0	11.8	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 125 W, f = 150 MHz, I_{DQ} = 100 mA)	η	50	60	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 125 W, f = 150 MHz, I_{DQ} = 100 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			

FIGURE 1 — 150 MHz TEST CIRCUIT



C1 — 35 pF Unleco
C2, C5 — Arco 462, 5-80 pF
C3 — 100 pF Unleco
C4 — 25 pF Unleco
C6 — 40 pF Unleco
C7 — Arco 461, 2.7-30 pF
C8 — Arco 463, 9-180 pF
C9, C11, C14 — 0.1 μF Erie Redcap
C10 — 50 μF, 50 V
C12, C13 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener

L1 — #16 AWG, 1-1/4 Turns, 0.213″ ID
L2 — #16 AWG, Hairpin 0.25″, 0.062″
L3 — #14 AWG, Hairpin 0.47″, 0.2″
L4 — 10 Turns #16 AWG Enameled Wire on R1
RFC1 — 18 Turns #16 AWG Enameled Wire, 0.3″ ID
R1 — 10 Ω, 2.0 W
R2 — 1.8 kΩ, 1/2 W
R3 — 10 kΩ, 10 Turn Bourns
R4 — 10 kΩ, 1/4 W

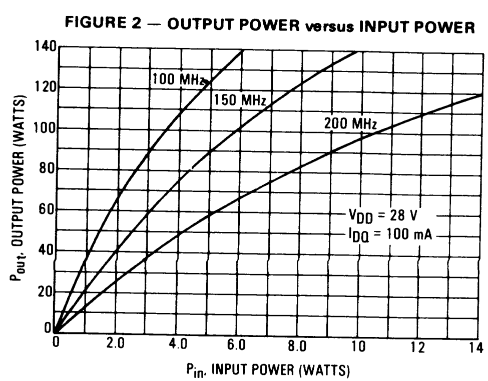


FIGURE 2 — OUTPUT POWER versus INPUT POWER

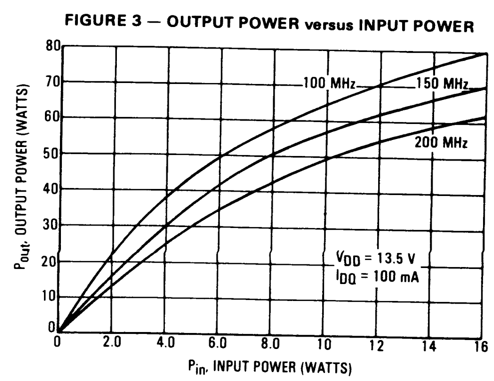


FIGURE 3 — OUTPUT POWER versus INPUT POWER

FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 100 MHz

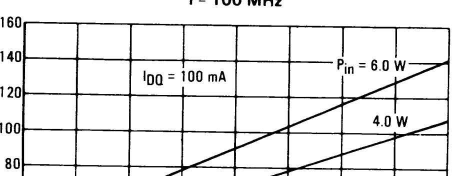
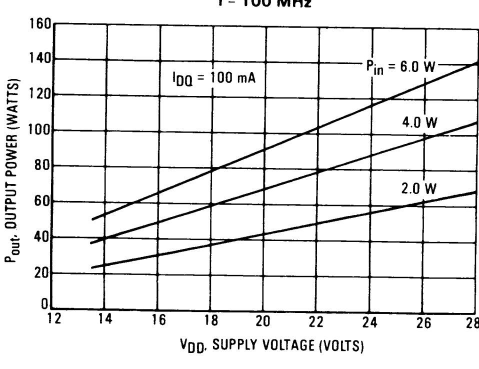



FIGURE 5 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 150 MHz

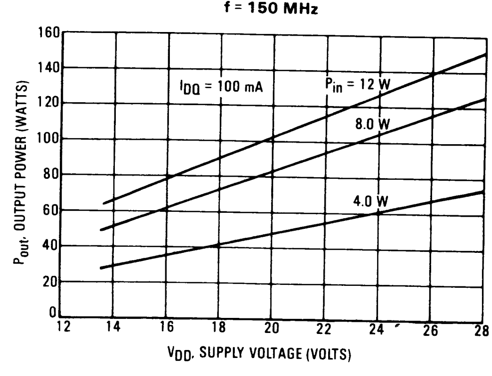


FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 200 MHz

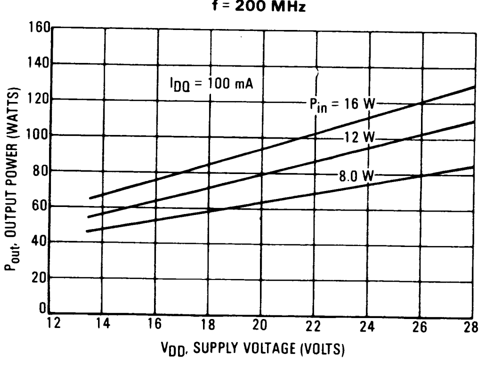


FIGURE 7 — POWER GAIN versus FREQUENCY

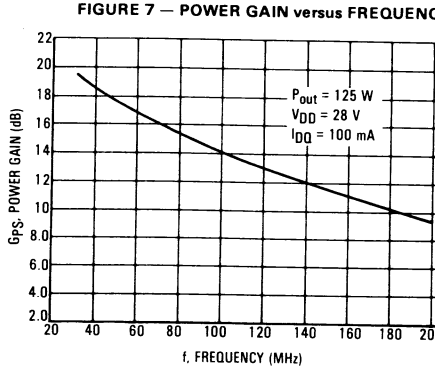


FIGURE 8 — OUTPUT POWER versus GATE VOLTAGE

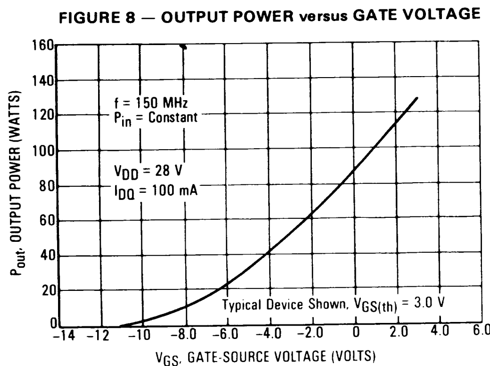


FIGURE 9 — DRAIN CURRENT versus GATE VOLTAGE (TRANSFER CHARACTERISTICS)

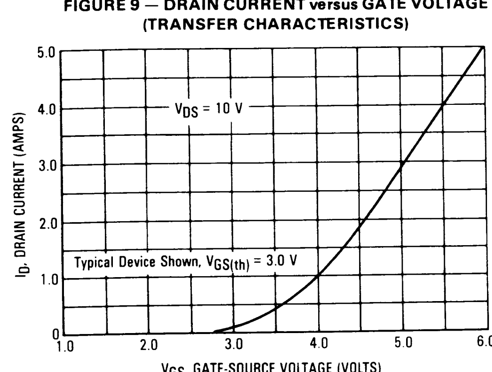


FIGURE 10 — GATE-SOURCE VOLTAGE versus CASE TEMPERATURE

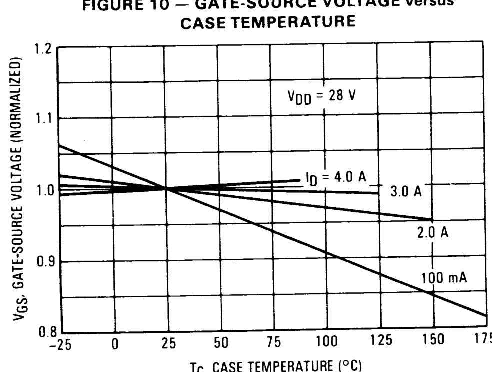


FIGURE 11 — CAPACITANCE versus DRAIN VOLTAGE

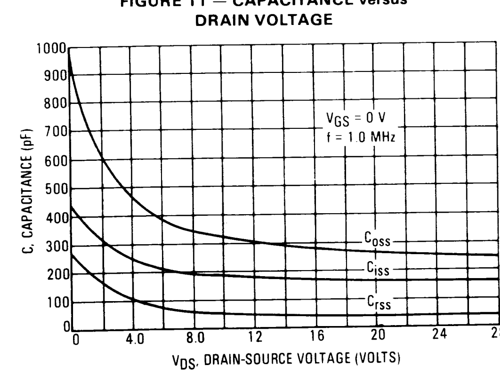


FIGURE 12 — DC SAFE OPERATING AREA

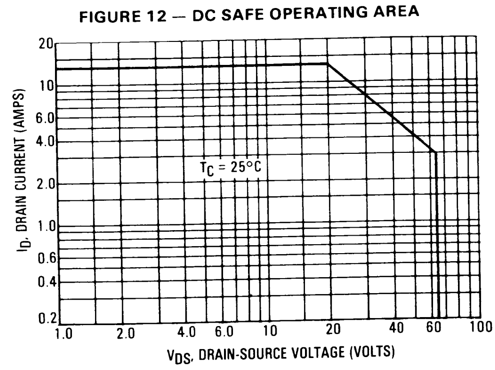


FIGURE 13 — COMMON SOURCE SCATTERING PARAMETERS
V_{DS} = 28 V, I_D = 3.0 A

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
2.0	0.932	-133	74.0	112	0.011	23	0.835	-151
5.0	0.923	-160	31.6	98	0.011	12	0.886	-168
10	0.921	-170	16.0	93	0.011	10	0.896	-174
20	0.921	-175	8.00	88	0.011	12	0.899	-177
30	0.921	-177	5.32	86	0.011	16	0.900	-178
40	0.921	-177	3.98	83	0.012	21	0.901	-178
50	0.922	-178	3.17	81	0.012	26	0.902	-178
60	0.923	-178	2.63	79	0.012	30	0.903	-178
70	0.924	-178	2.24	77	0.013	34	0.904	-178
80	0.925	-178	1.95	75	0.013	39	0.906	-178
90	0.927	-178	1.72	73	0.014	43	0.907	-178
100	0.930	-178	1.50	71	0.016	45	0.910	-178
110	0.930	-178	1.31	70	0.018	46	0.912	-178
120	0.931	-178	1.19	68	0.019	47	0.914	-178
130	0.942	-178	1.10	67	0.019	49	0.919	-178
140	0.936	-178	1.01	66	0.021	50	0.921	-178
150	0.938	-178	0.936	65	0.021	53	0.922	-178
160	0.938	-178	0.879	64	0.022	53	0.923	-178
170	0.940	-178	0.830	63	0.023	54	0.923	-177
180	0.942	-178	0.780	61	0.024	56	0.924	-177
190	0.942	-178	0.737	60	0.026	59	0.928	-177
200	0.952	-178	0.705	59	0.027	58	0.929	-177
210	0.950	-178	0.668	57	0.029	61	0.934	-177
220	0.942	-178	0.626	56	0.030	61	0.933	-177
230	0.943	-178	0.592	56	0.032	62	0.939	-177
240	0.946	-177	0.566	55	0.033	64	0.941	-177
250	0.952	-177	0.545	54	0.035	64	0.943	-177
260	0.958	-177	0.523	53	0.036	65	0.946	-177
270	0.956	-177	0.500	52	0.038	67	0.943	-177
280	0.960	-177	0.481	52	0.039	68	0.946	-177
290	0.956	-178	0.460	51	0.042	68	0.944	-177
300	0.955	-178	0.443	50	0.043	68	0.947	-177

FIGURE 14 — S_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 3.0 A

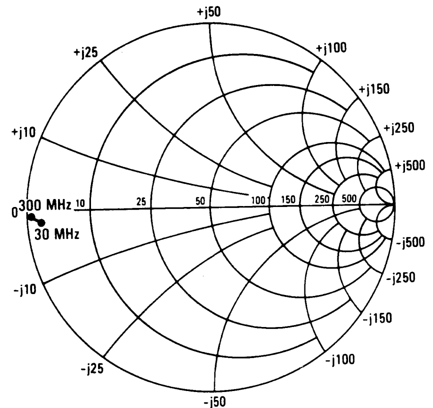


FIGURE 15 — S_{12}, REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 3.0 A

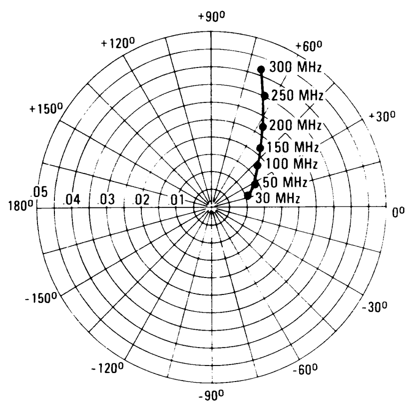


FIGURE 16 — S_{21}, FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 3.0 A

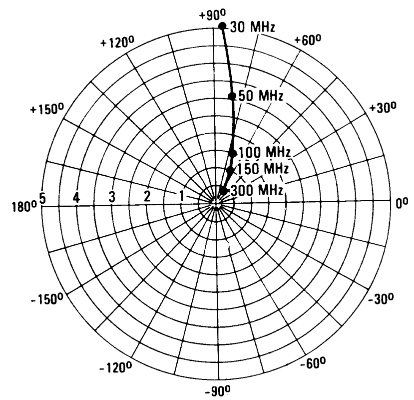
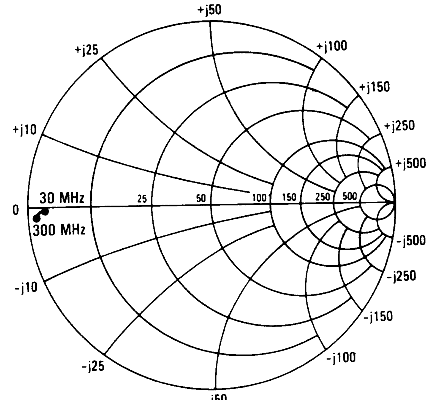


FIGURE 17 — S_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 3.0 A



DESIGN CONSIDERATIONS

The MRF174 is a TMOS RF power N-channel enhancement mode field-effect transistor (FET) designed for VHF power amplifier applications. Motorola TMOS FETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V-groove MOS power FETs.

Motorola Application Note AN-211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of TMOS RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF174 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF174 was characterized at I_{DQ} = 100 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF174 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC, and modulation systems. (See Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar VHF transistors are suitable for MRF174. See Motorola Application Note AN-721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of TMOS FETs helps ease the task of broadband network design. Both small-signal scattering parameters and large-signal impedances are provided. While the s-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of TMOS power FETs.

FIGURE 18 — 150 MHz TEST CIRCUIT

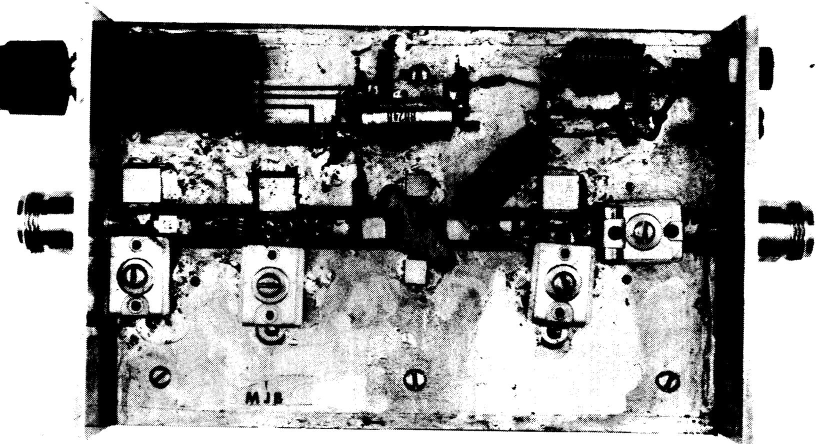
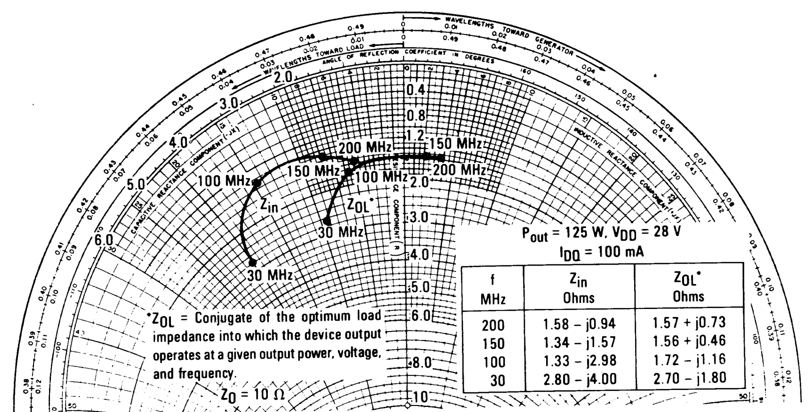


FIGURE 19 — SERIES EQUIVALENT INPUT AND OUTPUT IMPEDANCE, Z_{in}, Z_{OL}*



f MHz	Z_{in} Ohms	Z_{OL}* Ohms
200	1.58 – j0.94	1.57 + j0.73
150	1.34 – j1.57	1.56 + j0.46
100	1.33 – j2.98	1.72 – j1.16
30	2.80 – j4.00	2.70 – j1.80