MRF173*
MRF173CQ

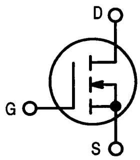
*Motorola Preferred Device

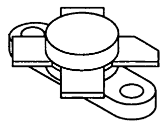
The RF MOSFET Line
RF Power
Field Effect Transistors
N-Channel Enhancement Mode MOSFETs

80 W, 28 V, 175 MHz
N-CHANNEL
BROADBAND
RF POWER MOSFETs

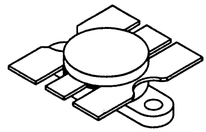
Designed for broadband commercial and military applications up to 200 MHz frequency range. The high-power, high-gain and broadband performance of these devices make possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance at 150 MHz, 28 V:
  Output Power = 80 W
  Gain = 11 dB (13 dB Typ)
  Efficiency = 55% Min. (60% Typ)
- Low Thermal Resistance
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability
- Low Noise Figure — 1.5 dB Typ at 2.0 A, 150 MHz
- Excellent Thermal Stability; Suited for Class A Operation





CASE 211-11, STYLE 2
MRF173



CASE 316-01, STYLE 3
MRF173CQ

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Drain-Gate Voltage	V_{DGO}	65	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	9.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	220 1.26	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Temperature Range	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.8	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{DS} = 0 V, V_{GS} = 0 V) I_D = 50 mA	$V_{(BR)DSS}$	65	—	—	V
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	—	—	2.0	mA
Gate-Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0 V)	I_{GSS}	—	—	1.0	µA
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 50 mA)	$V_{GS(th)}$	1.0	3.0	6.0	V
Drain-Source On-Voltage ($V_{DS(on)}$, V_{GS} = 10 V, I_D = 3.0 A)	$V_{DS(on)}$	—	—	1.4	V
Forward Transconductance (V_{DS} = 10 V, I_D = 2.0 A)	g_{fs}	1.8	2.2	—	mhos

(continued)

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	—	110	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{oss}	—	105	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{rss}	—	10	—	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure (V_{DD} = 28 V, f = 150 MHz, I_{DQ} = 50 mA)	NF	—	1.5	—	dB
Common Source Power Gain (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA)	G_{ps}	11	13	—	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA)	η	55	60	—	%
Electrical Ruggedness (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA) Load VSWR 30:1 at all phase angles	ψ	No Degradation in Output Power			
Series Equivalent Input Impedance MRF173 (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA)	Z_{in}	—	2.99–j4.5	—	Ohms
Series Equivalent Output Impedance MRF173 (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA)	Z_{out}	—	2.68–j1.3	—	Ohms
Series Equivalent Input Impedance MRF173CQ (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA)	Z_{in}	—	1.35–j5.15	—	Ohms
Series Equivalent Output Impedance MRF173CQ (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA)	Z_{out}	—	2.72–j149	—	Ohms

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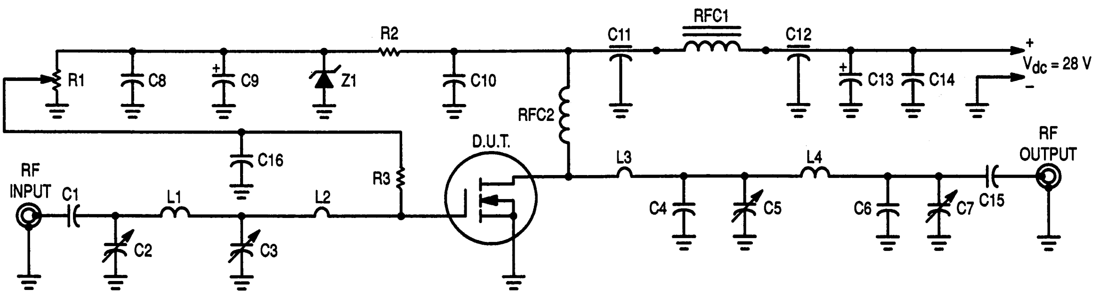

C1, C15 — 470 pF Unelco
C2, C3, C5 — Arco 463, 9–180 pF
C4, C6 — 15 pF Unelco
C7 — Arco 462 5–80 pF
C8, C10, C14, C16 — 0.1 µF
C9, C13 — 50 µF, 50 V Electrolytic
C11, C12 — 680 pF Feed Through
L1 — #16 AWG, 1-1/4 Turns, 0.3″ ID
L2 — #16 AWG Hairpin 1″ long
L3 — #14 AWG Hairpin 0.8″ long
L4 — #14 AWG Hairpin 1.1″ long
RFC1 — Ferroxcube VK200-19/4B
RFC2 — 18 Turns #18 AWG Enameled, 0.3″ ID
R1 — 10 kΩ, 10 Turns Bourns
R2 — 1.8 kΩ, 1/4 Watt
R3 — 10 kΩ, 1/2 Watt
Z1 — 1N5925A Motorola Zener

Figure 1. 150 MHz Test Circuit

TYPICAL CHARACTERISTICS

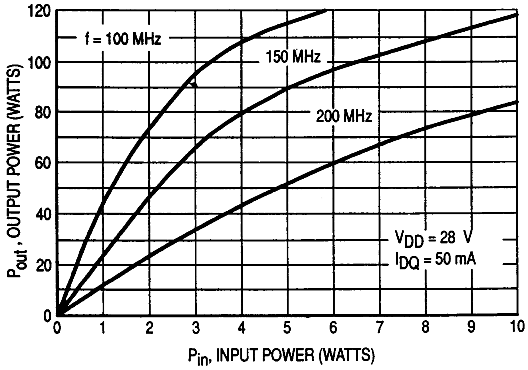

Figure 2. Output Power versus Input Power

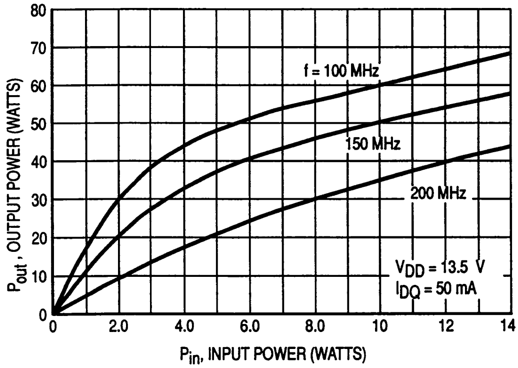

Figure 3. Output Power versus Input Power

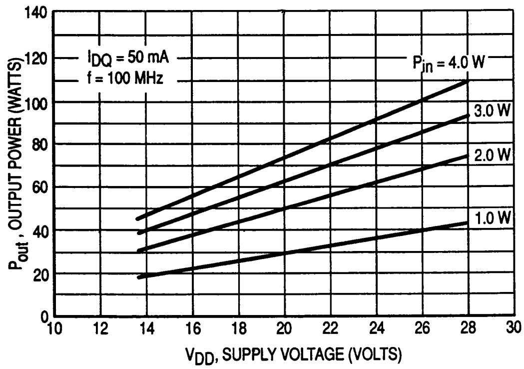

Figure 4. Output Power versus Supply Voltage

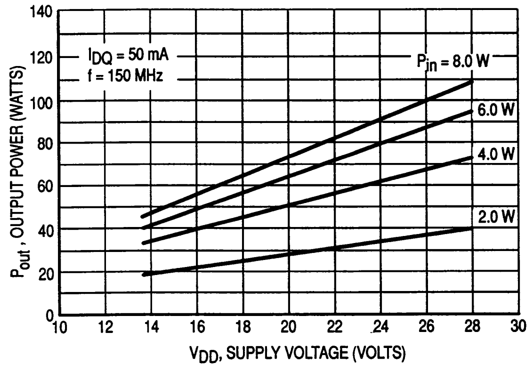

Figure 5. Output Power versus Supply Voltage

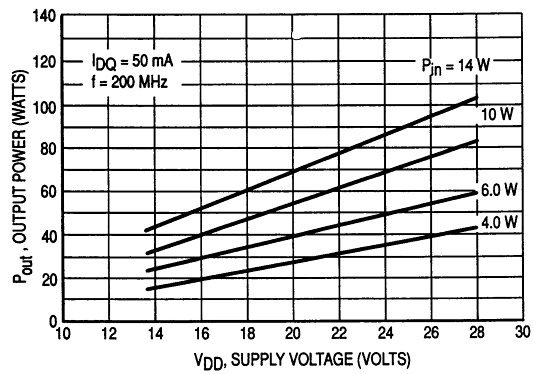

Figure 6. Output Power versus Supply Voltage

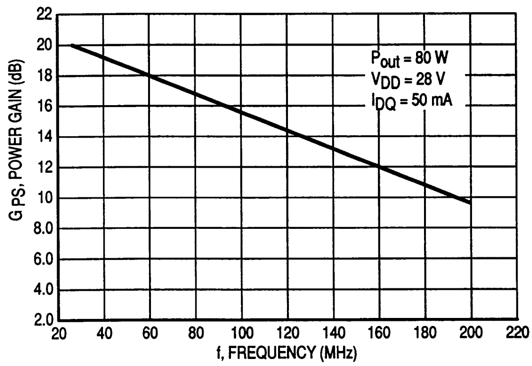

Figure 7. Power Gain versus Frequency

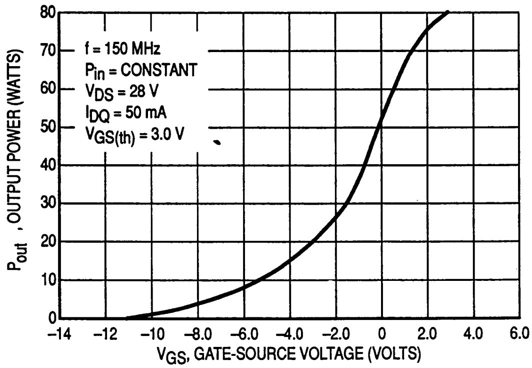

Figure 8. Output Power versus Gate Voltage

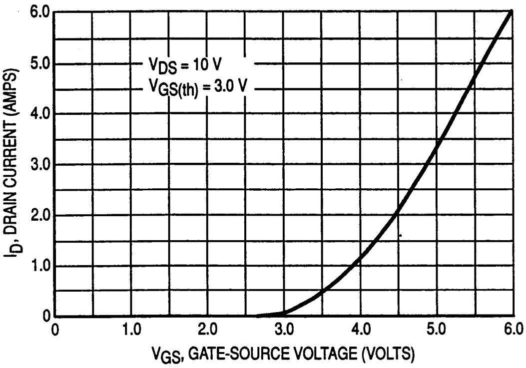

Figure 9. Drain Current versus Gate Voltage

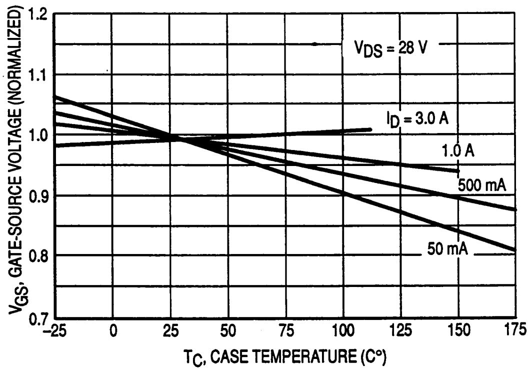

Figure 10. Gate-Source Voltage versus Case Temperature

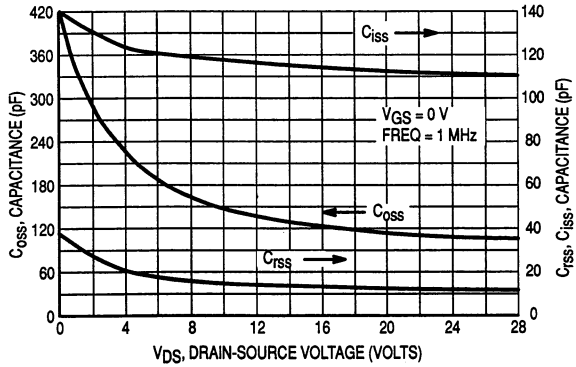

Figure 11. Capacitance versus Drain Voltage

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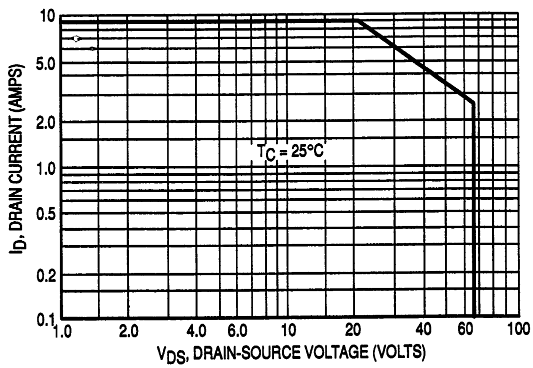


Figure 12. DC Safe Operating Area

DESIGN CONSIDERATIONS

The MRF173/CQ is a RF MOSFET power N-channel enhancement mode field-effect transistor (FET) designed for VHF power amplifier applications. Motorola's RF MOSFETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V-groove power FETs.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF173/CQ is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF173/CQ was characterized at $I_{DQ} = 50$ mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF173/CQ may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems. (see Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar VHF transistors are suitable for MRF173/CQ. See Motorola Application Note AN721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of RF MOSFETs helps ease the task of broadband network design. Both small-signal scattering parameters and large-signal impedances are provided. While the s-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF MOS power FETs.

2

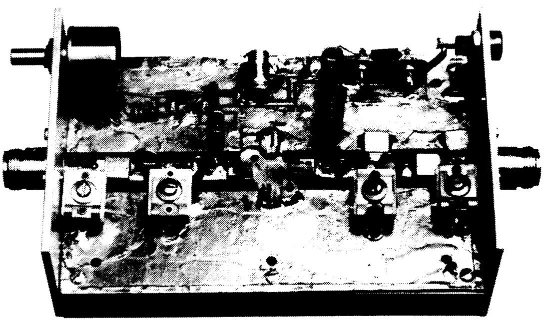


Figure 13. Test Circuit — MRF173

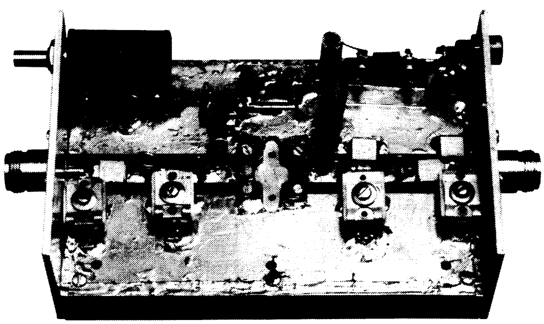


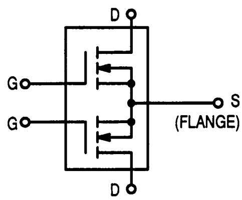
Figure 14. Test Circuit — MRF173CQ

MRF175GV
MRF175GU

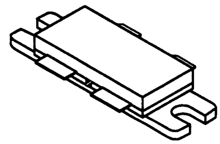
The RF MOSFET Line
RF Power
Field-Effect Transistors
N-Channel Enhancement-Mode

. . . designed for broadband commercial and military applications using push pull circuits at frequencies to 500 MHz. The high power, high gain and broadband performance of these devices makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance
  MRF175GV @ 28 V, 225 MHz ("V" Suffix)
    Output Power — 200 Watts
    Power Gain — 14 dB Typ
    Efficiency — 65% Typ
  MRF175GU @ 28 V, 400 MHz ("U" Suffix)
    Output Power — 150 Watts
    Power Gain — 12 dB Typ
    Efficiency — 55% Typ
- 100% Ruggedness Tested At Rated Output Power
- Low Thermal Resistance
- Low C_{rss} — 20 pF Typ @ V_{DS} = 28 V



**200/150 WATTS, 28 V, 500 MHz
N-CHANNEL MOS
BROADBAND
RF POWER FETs**



CASE 375, STYLE 2

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	26	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	400 2.27	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.44	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

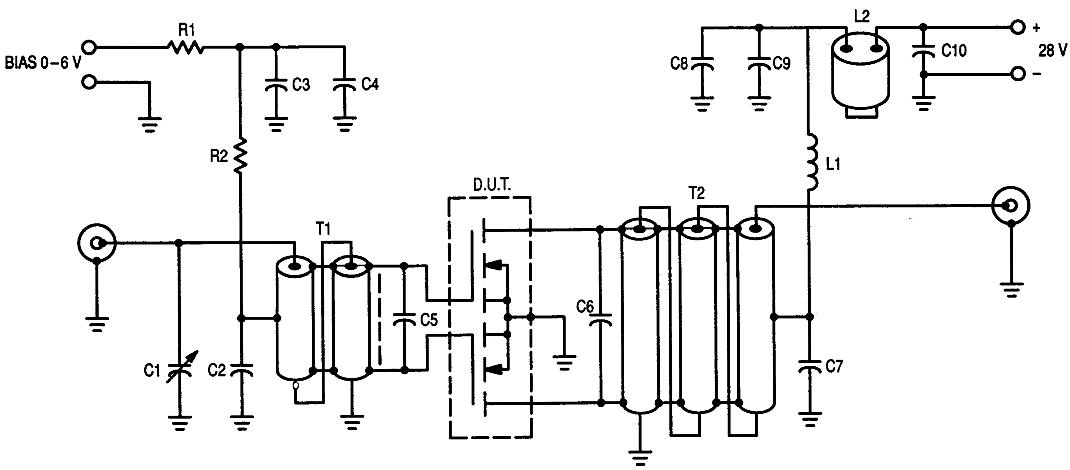
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 50 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	2.5	mAdc
Gate-Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V, I_D = 5.0 A)	$V_{DS(on)}$	—	—	1.5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.5 A)	g_{fs}	2.0	3.0	—	mhos
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	180	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	200	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	20	—	pF
FUNCTIONAL CHARACTERISTICS — MRF175GV (2) (Figure 1)					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 200 W, f = 225 MHz, I_{DQ} = 2.0 x 100 mA)	G_{ps}	12	14	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 200 W, f = 225 MHz, I_{DQ} = 2.0 x 100 mA)	η	55	65	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 200 W, f = 225 MHz, I_{DQ} = 2.0 x 100 mA, VSWR 10:1 at all Phase Angles)	ψ	No Degradation in Output Power			

NOTES:
1. Each side of device measured separately.
2. Measured in push-pull configuration.



C1 — Arco 404, 8.0–60 pF
C2, C3, C7, C8 — 1000 pF Chip
C4, C9 — 0.1 µF Chip
C5 — 180 pF Chip
C6 — 100 pF and 130 pF Chips in Parallel
C10 — 0.47 µF Chip, Kemet 1215 or Equivalent
L1 — 10 Turns AWG #16 Enamel Wire, Close Wound, 1/4″ I.D.
L2 — Ferrite Beads of Suitable Material for 1.5–2.0 µH Total Inductance

Board material — .062″ fiberglass (G10), Two sided, 1 oz. copper, $\varepsilon_r \cong 5$

Unless otherwise noted, all chip capacitors are ATC Type 100 or Equivalent.

R1 — 100 Ohms, 1/2 W
R2 — 1.0 k Ohm, 1/2 W
T1 — 4:1 Impedance Ratio RF Transformer. Can Be Made of 25 Ohm Semirigid Coax, 47–52 Mils O.D.
T2 — 1:9 Impedance Ratio RF Transformer. Can Be Made of 15–18 Ohms Semirigid Coax, 62–90 Mils O.D.

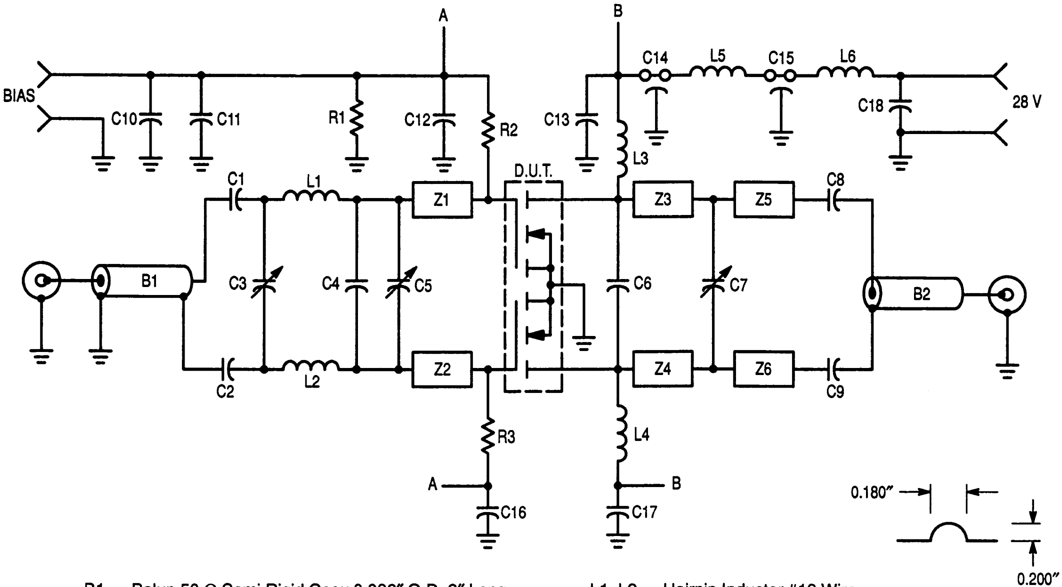
NOTE: For stability, the input transformer T1 should be loaded with ferrite toroids or beads to increase the common mode inductance. For operation below 100 MHz. The same is required for the output transformer.

Figure 1. 225 MHz Test Circuit

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL CHARACTERISTICS — MRF175GU (1) (Figure 2)					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 150 W, f = 400 MHz, I_{DQ} = 2.0 x 100 mA)	G_{ps}	10	12	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 150 W, f = 400 MHz, I_{DQ} = 2.0 x 100 mA)	η	50	55	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 150 W, f = 400 MHz, I_{DQ} = 2.0 x 100 mA, VSWR 10:1 at all Phase Angles)	ψ	No Degradation in Output Power			

NOTE:
1. Measured in push-pull configuration.



B1 — Balun 50 Ω Semi Rigid Coax 0.086″ O.D. 2″ Long
B2 — Balun 50 Ω Semi Rigid Coax 0.141″ O.D. 2″ Long
C1, C2, C8, C9 — 270 pF ATC Chip Cap
C3, C5, C7 — 1.0–20 pF Trimmer Cap
C4 — 15 pF ATC Chip Cap
C6 — 33 pF ATC Chip Cap
C10, C12, C13, C16, C17 — 0.01 µF Ceramic Cap
C11 — 1.0 µF 50 V Tantalum
C14, C15 — 680 pF Feedthru Cap
C18 — 20 µF 50 V Tantalum
L1, L2 — Hairpin Inductor #18 Wire
L3, L4 — 12 Turns #18 Enameled Wire 0.340″ I.D.
L5 — Ferroxcube VK200 20/4B
L6 — 3 Turns #16 Enameled Wire 0.340″ I.D.
R1 — 1.0 kΩ 1/4 W Resistor
R2, R3 — 10 kΩ 1/4 W Resistor
Z1, Z2 — Microstrip Line 0.400″ x 0.250″
Z3, Z4 — Microstrip Line 0.870″ x 0.250″
Z5, Z6 — Microstrip Line 0.500″ x 0.250″
Board material — 0.060″ Teflon-fiberglass, ε_r = 2.55, copper clad both sides, 2 oz. copper.

Figure 2. 400 MHz Test Circuit

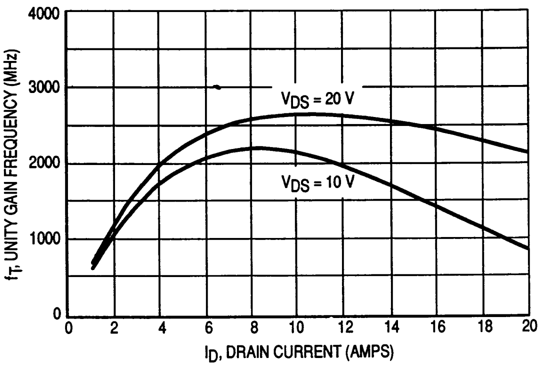


Figure 3. Common Source Unity Current Gain Frequency versus Drain Current

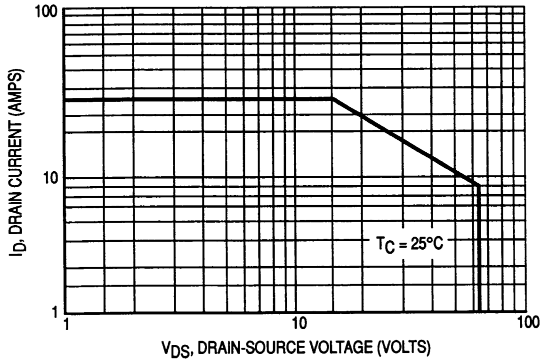


Figure 4. DC Safe Operating Area

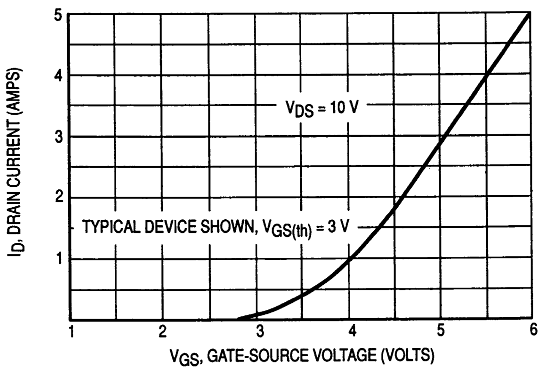


Figure 5. Drain Current versus Gate Voltage (Transfer Characteristics)

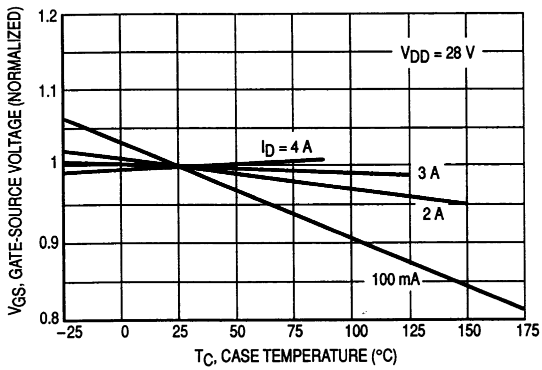


Figure 6. Gate-Source Voltage versus Case Temperature

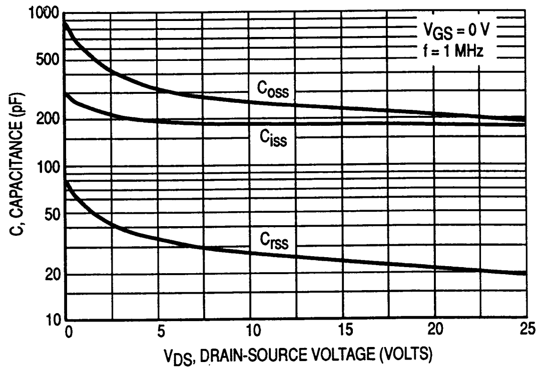


Figure 7. Capacitance versus Drain-Source Voltage*

* Data shown applies to each half of MRF175GV/GU.

TYPICAL CHARACTERISTICS
MRF175GV

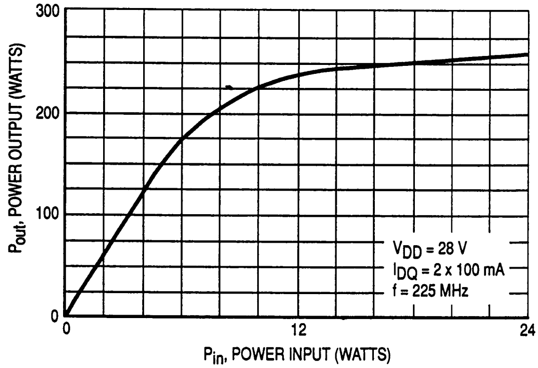


Figure 8. Power Input versus Power Output

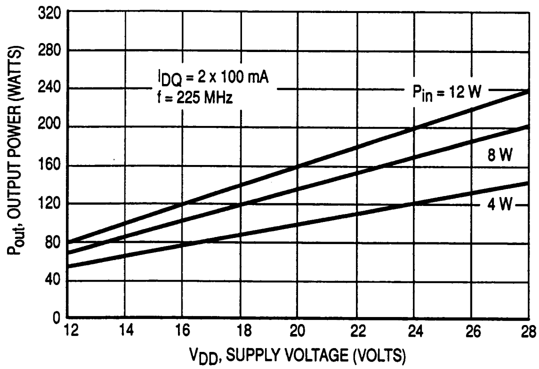


Figure 9. Output Power versus Supply Voltage

MRF175GU

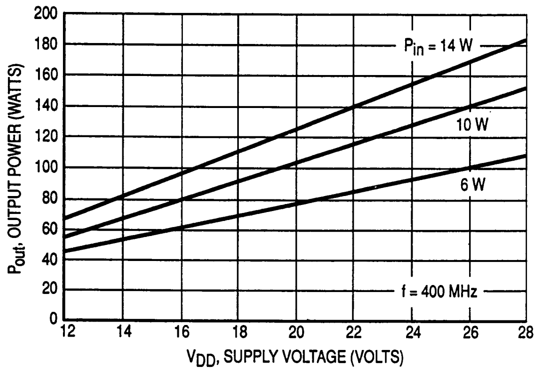


Figure 10. Output Power versus Supply Voltage

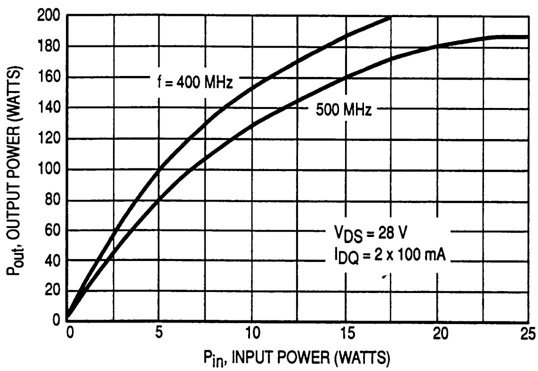


Figure 11. Output Power versus Input Power

MRF175GV

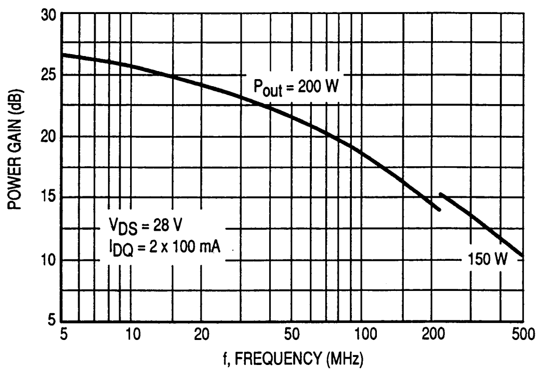
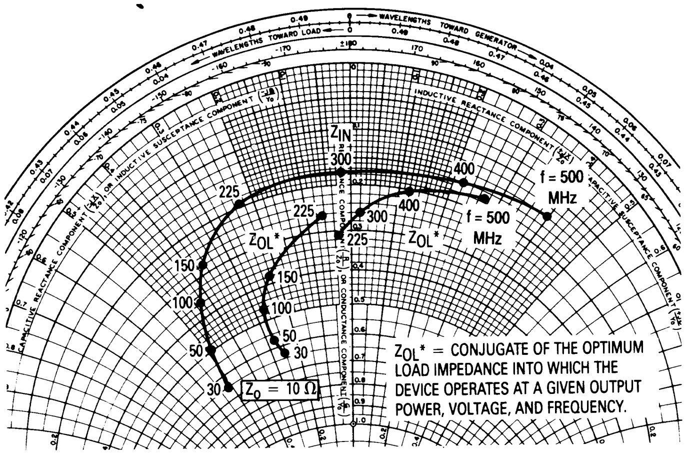


Figure 12. Power Gain versus Frequency

INPUT AND OUTPUT IMPEDANCE



V_{DD} = 28 V I_{DQ} = 2 x 100 mA

f MHz	Z_{IN} OHMS	Z_{OL}* OHMS
(P_{out} = 150 W)		
225	1.95 - j2.30	3.10 - j0.25
300	1.75 - j0.20	2.60 + j0.20
400	1.60 + j2.20	2.00 + j1.20
500	1.35 + j4.00	1.70 + j2.70
(P_{out} = 200 W)		
30	6.50 - j5.10	6.30 - j2.50
50	5.00 - j4.80	5.75 - j2.75
100	3.60 - j4.20	4.60 - j2.65
150	2.80 - j3.60	2.60 - j2.20
225	1.95 - j2.30	2.60 - j0.60

NOTE: Input and output impedance values given are measured from gate to gate and drain to drain respectively.

Figure 13. Series Equivalent Input/Output Impedance

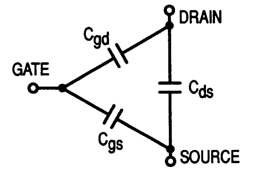
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain-to-source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



$C_{iss} = C_{gd} + C_{gs}$
$C_{oss} = C_{gd} + C_{ds}$
$C_{rss} = C_{gd}$

The C_{iss} given in the electrical characteristics table was measured using method 2 above. It should be noted that C_{iss}, C_{oss}, C_{rss} are measured at zero drain current and are provided for general information about the device. They are not RF design parameters and no attempt should be made to use them as such.

LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain, data presented in Figure 3 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate-source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating (or any of the maximum ratings on the front page). Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of this device are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate-to-source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with grounded equipment.

DESIGN CONSIDERATIONS

The MRF175G is a RF power N-channel enhancement mode field-effect transistor (FETs) designed for HF, VHF and UHF power amplifier applications. Motorola RF MOSFETs feature a vertical structure with a planar design.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal.

DC BIAS

The MRF175G is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF175G was characterized at I_{DQ} = 100 mA, each side, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias sytem.

GAIN CONTROL

Power output of the MRF176 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

2

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

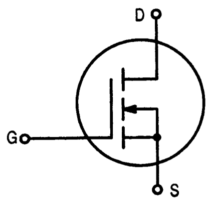
MRF175LV
MRF175LU

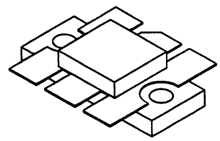
The RF MOSFET Line
RF Power
Field-Effect Transistors
N-Channel Enhancement-Mode

100 W, 28 V, 400 MHz
N-CHANNEL
BROADBAND
RF POWER FETs

. . . designed for broadband commercial and military applications using single ended circuits at frequencies to 400 MHz. The high power, high gain and broadband performance of each device makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance
  - MRF175LV @ 28 V, 225 MHz ("V" Suffix)
    - Output Power — 100 Watts
    - Power Gain — 14 dB Typ
    - Efficiency — 65% Typ
  - MRF175LU @ 28 V, 400 MHz ("U" Suffix)
    - Output Power — 100 Watts
    - Power Gain — 10 dB Typ
    - Efficiency — 55% Typ
- 100% Ruggedness Tested At Rated Output Power
- Low Thermal Resistance
- Low C_{rss} — 20 pF Typ @ V_{DS} = 28 V





CASE 333, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	13	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

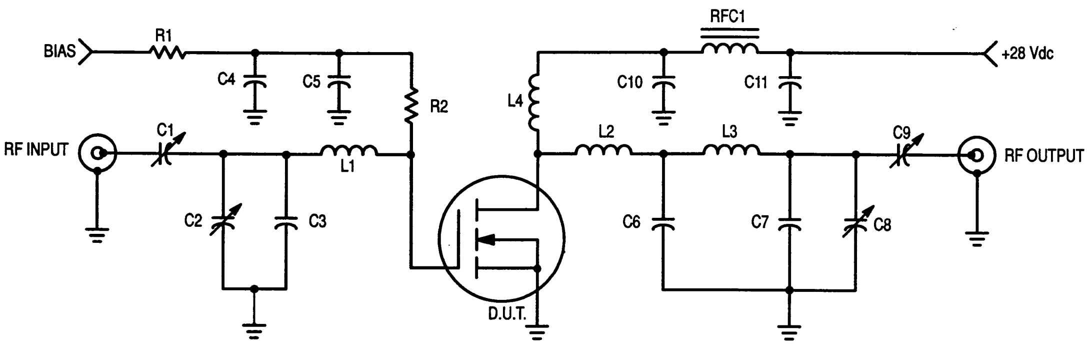
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 50 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc

(continued)

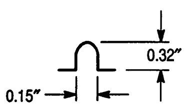
ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V, I_D = 5.0 A)	$V_{DS(on)}$	—	—	1.5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.5 A)	g_{fs}	2.0	3.0	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	180	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	200	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	20	—	pF
FUNCTIONAL CHARACTERISTICS — MRF175LV (Figure 1)					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 225 MHz, I_{DQ} = 100 mA)	G_{ps}	12	14	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 225 MHz, I_{DQ} = 100 mA)	η	55	65	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 225 MHz, I_{DQ} = 100 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			
FUNCTIONAL CHARACTERISTICS — MRF175LU (Figure 2)					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 400 MHz, I_{DQ} = 100 mA)	G_{ps}	8.0	10	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 400 MHz, I_{DQ} = 100 mA)	η	50	55	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 400 MHz, I_{DQ} = 100 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			



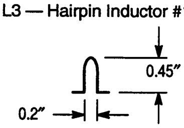
C1, C2, C8 — Arco 463 or Equivalent
C3, C7 — 25 pF Unelco Cap
C4 — 1000 pF Chip Cap
C5 — 0.01 µF Chip Cap
C6 — 250 pF Unelco Cap
C9 — Arco 462 or Equivalent
C10 — 1000 pF ATC Chip Cap
C11 — 10 µF 100 V Electrolytic

L1 — Hairpin Inductor #18 Wire



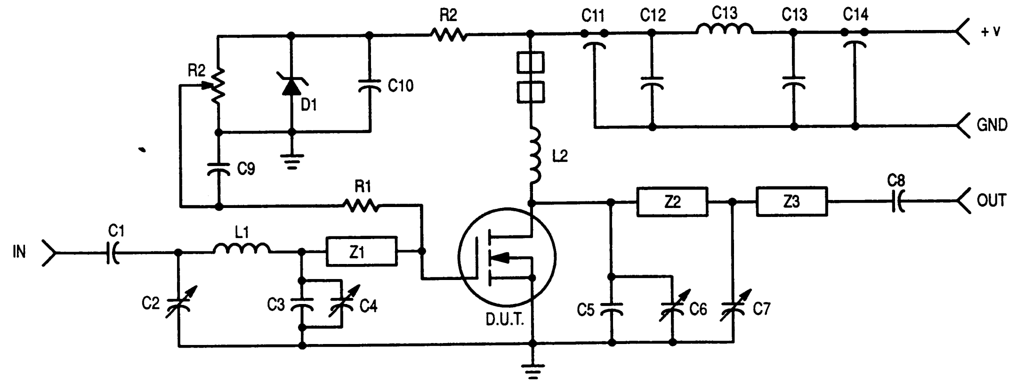
L2 — Stripline Inductor 0.200″ x 0.500″

L3 — Hairpin Inductor #16 Wire



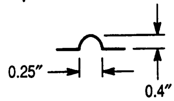
L4 — 2 Turns #16 Wire 5/16″ ID
RFC1 — VK200-4B
R1 — 1.0 k 1/4 W Resistor
R2 — 100 Ω Resistor

Figure 1. 225 MHz Test Circuit



C1, C8 — 270 pF ATC Chip Cap
C2, C4, C6, C7 — 1.0–20 pF Trimmer Cap
C3 — 15 pF Mini Unelco Cap
C5 — 33 pF Mini Unelco Cap
C9, C10, C12 — 0.1 µF Ceramic Cap
C11, C14 — 680 pF Feed Thru Cap
C13 — 50 µF Tantalum Cap

D1 — 1N5352 Zener Diode
L1 — Hairpin Inductor #18 Wire



L2 — 12 Turns #18 Wire 0.450″ ID
L3 — Ferroxcube VK200 20/4B

R1 — 10 k 1/4 W Resistor
R2 — 10 k Variable Resistor
R3 — 1.5 k 1/4 W Resistor
Z1 — Microstrip Line 0.950″ x 0.250″
Z2 — Microstrip Line 1″ x 0.250″
Z3 — Microstrip Line 0.550″ x 0.250″
Board Material — 0.062″ Teflon — fiberglass, ε_r = 2.56, 1 oz. copper clad both sides

Figure 2. 400 MHz Test Circuit

2

TYPICAL CHARACTERISTICS

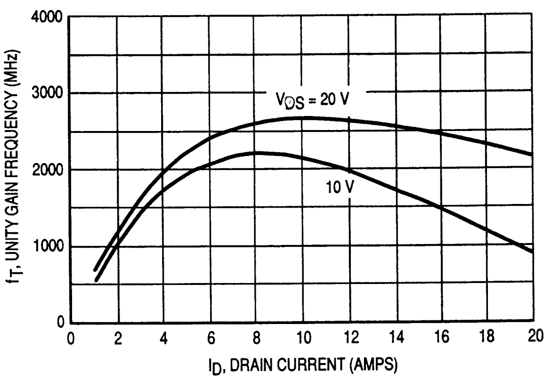


Figure 3. Common Source Unity Current Gain Frequency versus Drain Current

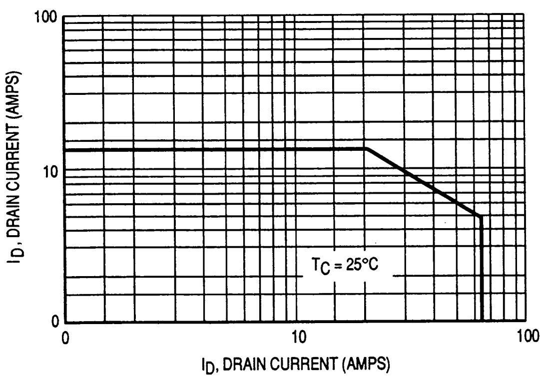


Figure 4. DC Safe Operating Area

TYPICAL CHARACTERISTICS

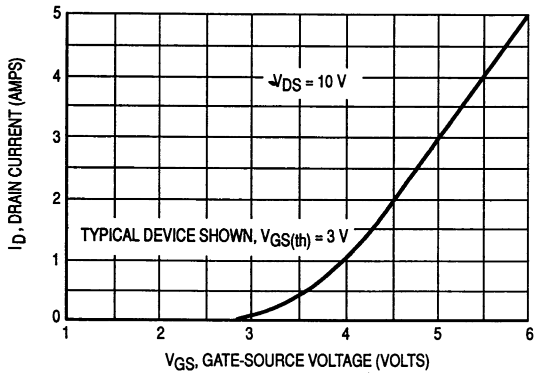


Figure 5. Drain Current versus Gate Voltage (Transfer Characteristics)

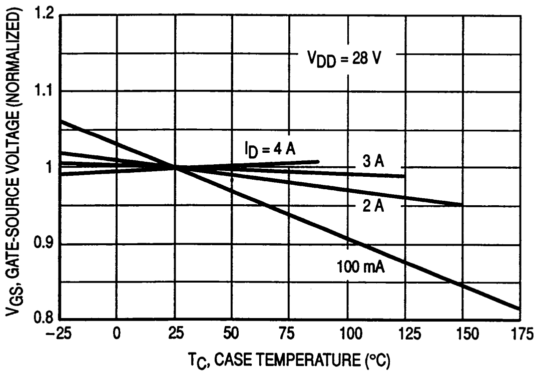


Figure 6. Gate-Source Voltage versus Case Temperature

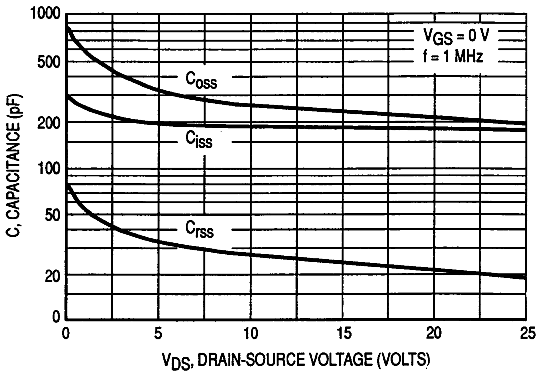


Figure 7. Capacitance versus Drain-Source Voltage

2

TYPICAL CHARACTERISTICS

MRF175LV

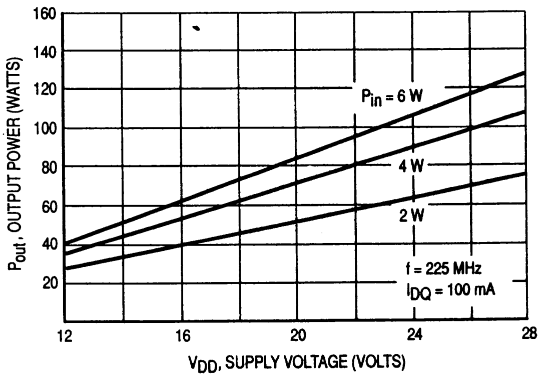


Figure 8. Output Power versus Supply Voltage

MRF175LU

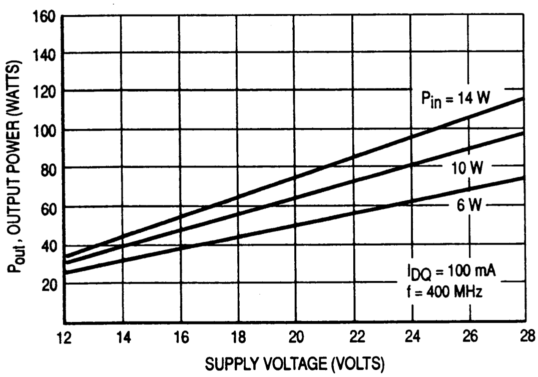


Figure 9. Output Power versus Supply Voltage

2

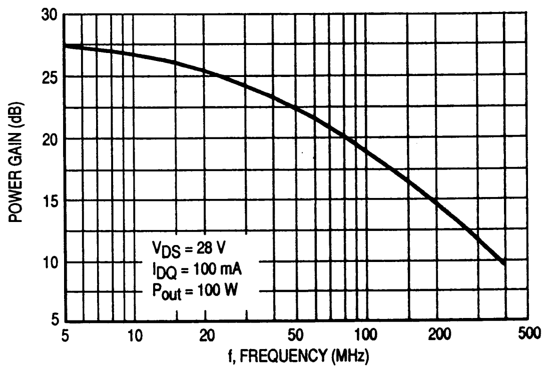
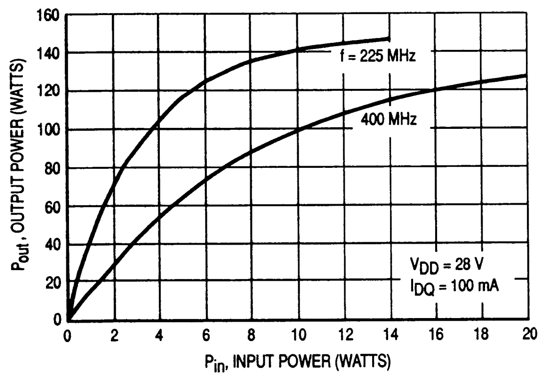


Figure 10. Power Gain versus Frequency



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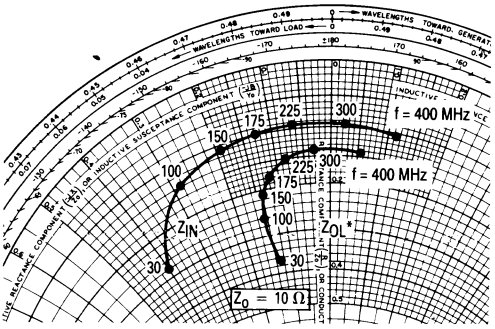
INPUT AND OUTPUT IMPEDANCE



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(P_{out} = 100 W)

f MHz	Z_{IN} Ohms	Z_{OL}* Ohms
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150	1.10 – j1.90	2.10 – j1.40
175	1.00 – j1.25	1.80 – j1.20
225	0.95 – j0.65	1.50 – j0.80
300	0.95 + j0.20	1.35 – j0.30
400	1.05 + j1.15	1.45 + j0.55

Z_{OL}* = CONJUGATE OF THE OPTIMUM LOAD IMPEDANCE INTO WHICH THE DEVICE OPERATES AT A GIVEN OUTPUT POWER, VOLTAGE, AND FREQUENCY.

2

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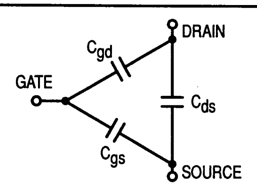

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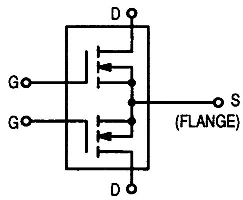
2

MRF176GV
MRF176GU

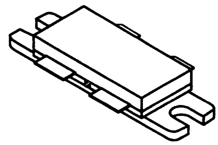
The RF MOSFET Line
RF Power
Field-Effect Transistors
N-Channel Enhancement-Mode

. . . designed for broadband commercial and military applications using push pull circuits at frequencies to 500 MHz. The high power, high gain and broadband performance of these devices makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Electrical Performance
  - MRF176GV @ 50 V, 225 MHz ("V" Suffix)
    - Output Power — 200 Watts
    - Power Gain — 17 dB Typ
    - Efficiency — 55% Typ
  - MRF176GU @ 50 V, 400 MHz ("U" Suffix)
    - Output Power — 150 Watts
    - Power Gain — 14 dB Typ
    - Efficiency — 50% Typ
- 100% Ruggedness Tested At Rated Output Power
- Low Thermal Resistance
- Low C_{rss} — 7.0 pF Typ @ V_{DS} = 50 V



**200/150 W, 50 V, 500 MHz
N-CHANNEL MOS
BROADBAND
RF POWER FETs**



CASE 375, STYLE 2

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	125	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	16	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	400 2.27	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.44	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)	I_{DSS}	—	—	2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc

NOTE:
1. Each side of device measured separately.

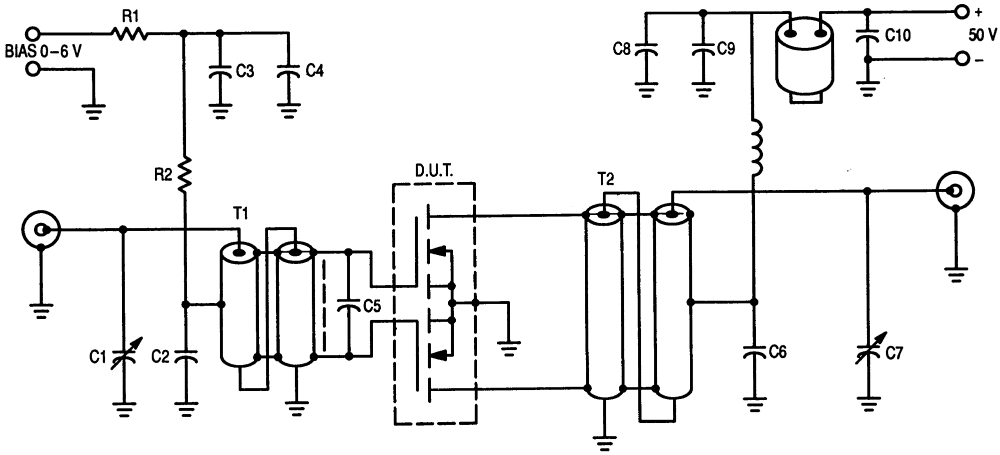
(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V, I_D = 5.0 A)	$V_{DS(on)}$	—	—	5.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.5 A)	g_{fs}	2.0	3.0	—	mhos
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	180	—	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	110	—	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	7.0	—	pF
FUNCTIONAL CHARACTERISTICS — MRF176GV (2) (Figure 1)					
Common Source Power Gain (V_{DD} = 50 Vdc, P_{out} = 200 W, f = 225 MHz, I_{DQ} = 2.0 x 100 mA)	G_{ps}	15	17	—	dB
Drain Efficiency (V_{DD} = 50 Vdc, P_{out} = 200 W, f = 225 MHz, I_{DQ} = 2.0 x 100 mA)	η	50	55	—	%
Electrical Ruggedness (V_{DD} = 50 Vdc, P_{out} = 200 W, f = 225 MHz, I_{DQ} = 2.0 x 100 mA, VSWR 10:1 at all Phase Angles)	ψ	No Degradation in Output Power			

NOTES:
1. Each side of device measured separately.
2. Measured in push-pull configuration.

2



C1 — Arco 404, 8.0–60 pF
C2, C3, C6, C8 — 1000 pF Chip
C4, C9 — 0.1 µF Chip
C5 — 180 pF Chip
C7 — Arco 403, 3.0–35 pF
C10 — 0.47 µF Chip, Kemet 1215 or Equivalent
L1 — 10 Turns AWG #16 Enameled Wire, Close Wound, 1/4″ I.D.

Board material — .062″ fiberglass (G10), Two sided, 1 oz. copper, $\varepsilon_r \cong 5$

Unless otherwise noted, all chip capacitors are ATC Type 100 or Equivalent

L2 — Ferrite Beads of Suitable Material for 1.5–2.0 µH, Total Inductance
R1 — 100 Ohms, 1/2 W
R2 — 1.0 kOhms, 1/2 W
T1 — 4:1 Impedance Ratio RF Transformer. Can Be Made of 25 Ohm Semirigid Co-Ax, 47–62 Mils O.D.
T2 — 1:4 Impedance Ratio RF Transformer. Can Be Made of 25 Ohm Semirigid Co-Ax, 62–90 Mils O.D.

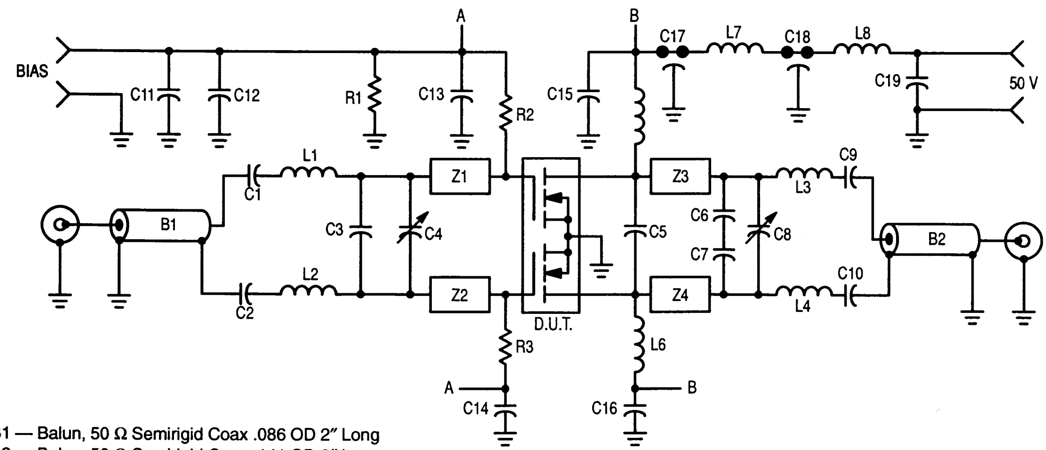
NOTE: For stability, the input transformer T1 should be loaded with ferrite toroids or beads to increase the common mode inductance. For operation below 100 MHz. The same is required for the output transformer.

Figure 1. 225 MHz Test Circuit

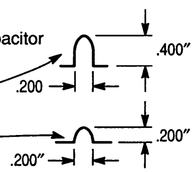
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL CHARACTERISTICS — MRF176GU (1) (Figure 2)					
Common Source Power Gain (V_{DD} = 50 Vdc, P_{out} = 150 W, f = 400 MHz, I_{DQ} = 2.0 x 100 mA)	G_{ps}	12	14	—	dB
Drain Efficiency (V_{DD} = 50 Vdc, P_{out} = 150 W, f = 400 MHz, I_{DQ} = 2.0 x 100 mA)	η	45	50	—	%
Electrical Ruggedness (V_{DD} = 50 Vdc, P_{out} = 150 W, f = 400 MHz, I_{DQ} = 2.0 x 100 mA, VSWR 10:1 at all Phase Angles)	ψ	No Degradation in Output Power			

NOTE:
1. Measured in push-pull configuration.



B1 — Balun, 50 Ω Semirigid Coax .086 OD 2″ Long
B2 — Balun, 50 Ω Semirigid Coax .141 OD 2″ Long
C1, C2, C9, C10 — 270 pF ATC Chip Capacitor
C3 — 15 pF ATC Chip Cap
C4, C8 — 1.0–20 pF Piston Trimmer Cap
C5 — 27 pF ATC Chip Cap
C6, C7 — 22 pF Mini Unelco Capacitor
C11, C13, C14, C15, C16 — 0.01 µF Ceramic Capacitor
C12 — 1.0 µF 50 V Tantalum Cap
C17, C18 — 680 pF Feedthru Capacitor
C19 — 10 µF 100 V Tantalum Cap
L1, L2 — Hairpin Inductor #18 W
L3, L4 — Hairpin Inductor #18 W



L5, L6 — 13T #18 W .250 ID
L7 — Ferroxcube VK-200 20/4B
L8 — 3T #18 W .340 ID
R1 — 1.0 kΩ 1/4 W Resistor
R2, R3 — 10 kΩ 1/4 W Resistor
Z1, Z2 — Microstrip Line .400L x .250W
Z3, Z4 — Microstrip Line .450L x .250W

Ckt Board Material — .060″ teflon-fiberglass, copper clad both sides, 2 oz. copper, ε_r = 2.55

Figure 2. 400 MHz Test Circuit

TYPICAL CHARACTERISTICS

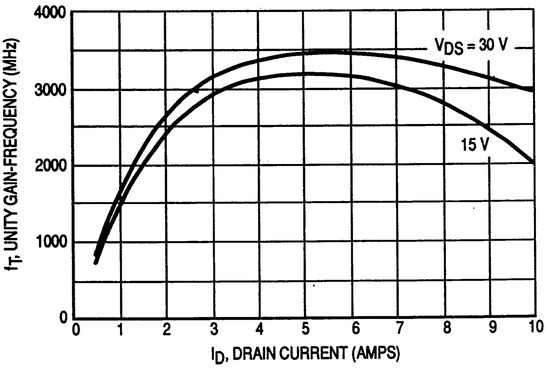


Figure 3. Common Source Unity Current Gain* Gain-Frequency versus Drain Current

* Data shown applies to each half of MRF176GV/GU

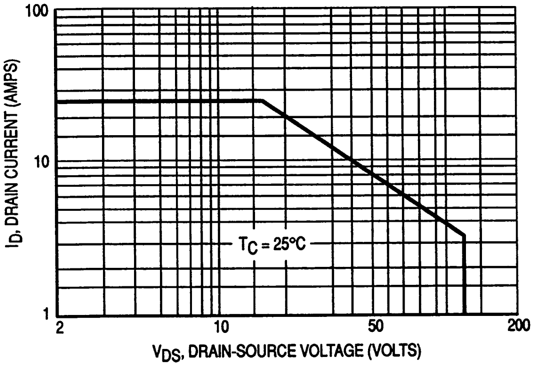
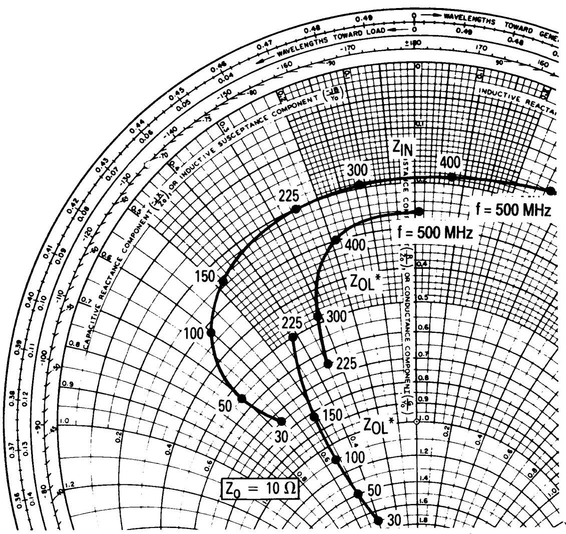


Figure 4. DC Safe Operating Area



INPUT AND OUTPUT IMPEDANCE
MRF176GU/GV
V_{DD} = 50 V I_{DQ} = 2 x 100 mA

f MHz	Z_{IN} OHMS	Z_{OL}* OHMS
(P_{out} = 150 W)		
225	2.05 - j2.50	6.50 - j3.50
300	2.00 - j1.10	4.80 - j3.10
400	1.85 + j0.75	3.00 - j1.90
500	1.60 + j2.70	2.60 + j0.10
(P_{out} = 200 W)		
30	7.50 - j6.50	17.00 - j4.00
50	5.50 - j7.00	14.00 - j5.00
100	3.20 - j6.00	11.00 - j5.20
150	2.50 - j4.80	8.20 - j5.00
225	2.05 - j2.50	5.00 - j4.20

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

NOTE: Input and output impedance values given are measured from gate to gate and drain to drain respectively.

Figure 5. Series Equivalent Input/Output Impedance

TYPICAL CHARACTERISTICS

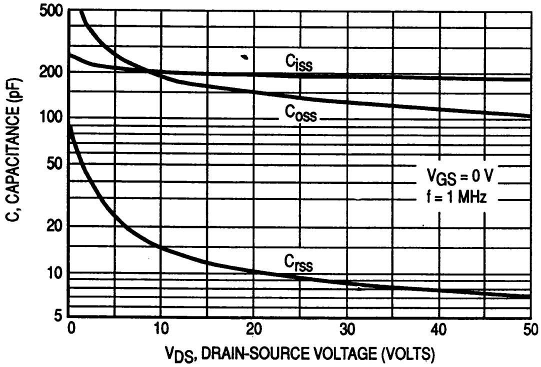


Figure 6. Capacitance versus Drain-Source Voltage*

* Data shown applies to each half of MRF176GV/GU

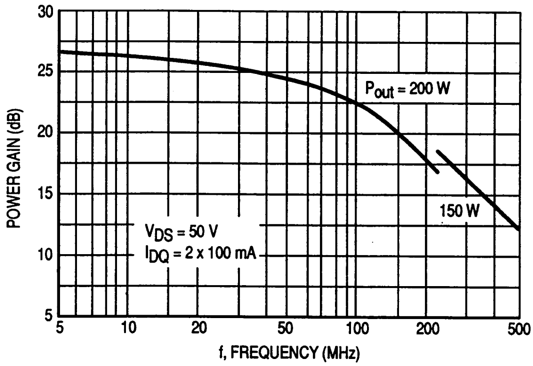


Figure 7. Power Gain versus Frequency

MRF176GV

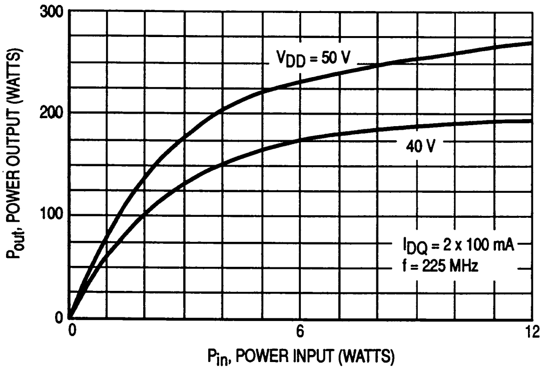


Figure 8. Power Input versus Power Output

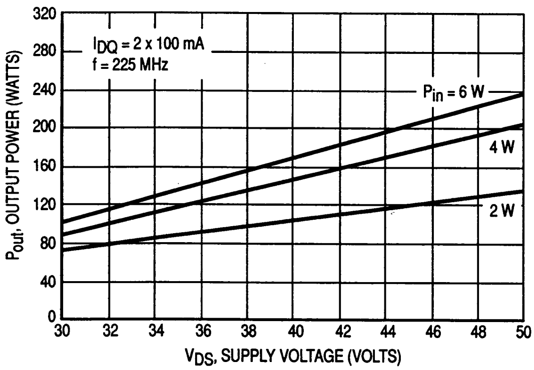


Figure 9. Output Power versus Supply Voltage

2

TYPICAL CHARACTERISTICS
MRF176GU

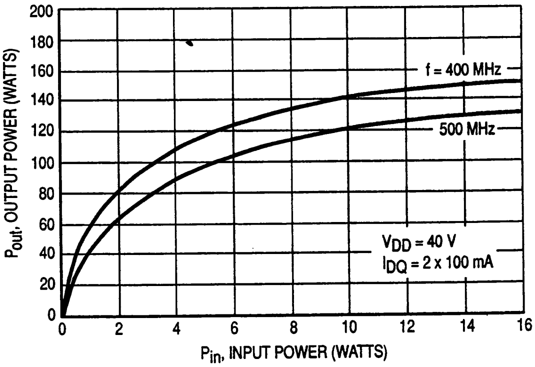


Figure 10. Output Power versus Input Power

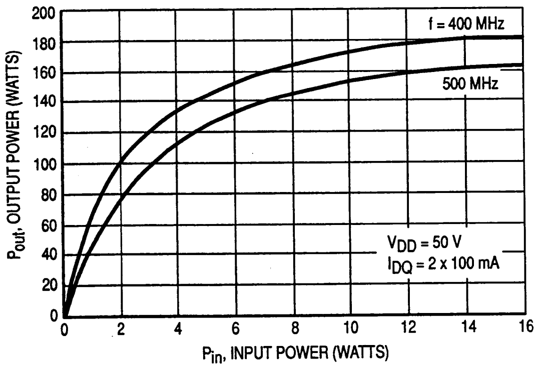


Figure 11. Output Power versus Input Power

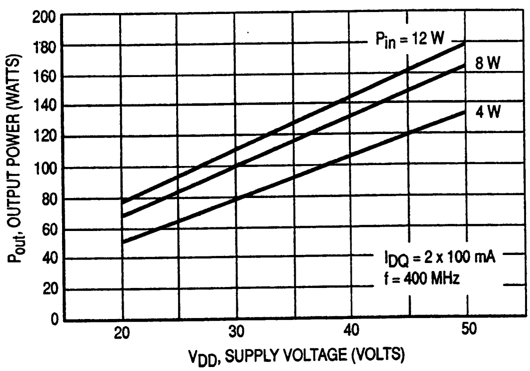


Figure 12. Output Power versus Supply Voltage

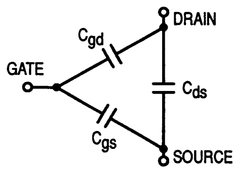
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain-to-source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



$C_{iss} = C_{gd} + C_{gs}$
$C_{oss} = C_{gd} + C_{ds}$
$C_{rss} = C_{gd}$

The C_{iss} given in the electrical characteristics table was measured using method 2 above. It should be noted that C_{iss}, C_{oss}, C_{rss} are measured at zero drain current and are provided for general information about the device. They are not RF design parameters and no attempt should be made to use them as such.

LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain, data presented in Figure 3 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate-source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating (or any of the maximum ratings on the front page). Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of this device are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — This device does not have an internal monolithic zener diode from gate-to-source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

HANDLING CONSIDERATIONS

The gate of the MOSFET, which is electrically isolated from the rest of the die by a very thin layer of SiO_2, may be damaged if the power MOSFET is handled or installed improperly. Exceeding the 40 V maximum gate-to-source voltage rating, $V_{GS(max)}$, can rupture the gate insulation and destroy the FET. RF Power MOSFETs are not nearly as susceptible as CMOS devices to damage due to static discharge because the input capacitances of power MOSFETs are much larger and absorb more energy before being charged to the gate breakdown voltage. However, once breakdown begins, there is enough energy stored in the gate-source capacitance to ensure the complete perforation of the gate oxide. To avoid the possibility of device failure caused by static discharge, precautions similar to those taken with small-signal MOSFET and CMOS devices apply to power MOSFETs.

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with grounded equipment.

The gate of the power MOSFET could still be in danger after the device is placed in the intended circuit. If the gate may see voltage transients which exceed $V_{GS(max)}$, the circuit designer should place a 40 V zener across the gate and source terminals to clamp any potentially destructive spikes. Using a resistor to keep the gate-to-source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

DESIGN CONSIDERATIONS

The MRF176G is a RF power N-channel enhancement mode field-effect transistor (FETs) designed for VHF and

UHF power amplifier applications. Motorola RF MOSFETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V-groove MOS power FETs.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF176G is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF176G was characterized at I_{DQ} = 100 mA, each side, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias sytem.

GAIN CONTROL

Power output of the MRF176 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

2

MRF177
MRF177M*

*Motorola Preferred Device

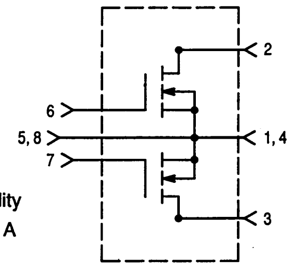
**100 W, 28 V, 400 MHz
N-CHANNEL
BROADBAND
RF POWER MOSFETs**

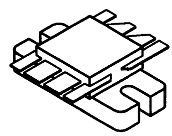
The RF MOSFET Line
RF Power Field Effect Transistors
N-Channel Enhancement Mode MOSFETs

Designed for broadband commercial and military applications up to 400 MHz frequency range. Primarily used as drivers or output amplifiers in push-pull configurations. Can be used in manual gain control, ALC and modulation circuits.

- Typical Performance at 400 MHz, 28 V:
  Output Power — 100 W
  Gain — 12 dB
  Efficiency — 60%
- Low Thermal Resistance
- Low C_{rss} — 10 pF Typ @ V_{DS} = 28 Volts
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability
- Excellent Thermal Stability; Suited for Class A Operation

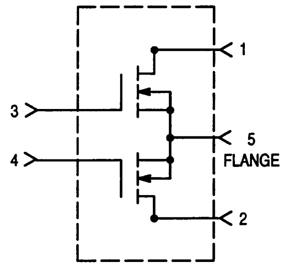
CASE 744A-01

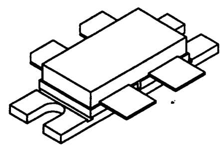




CASE 744A-01, STYLE 2
MRF177

CASE 390B-01





CASE 390B-01, STYLE 1
MRF177M

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	16	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Temperature Range	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.65	°C/W

NOTE:
1. Total device dissipation rating applies only when the device is operated as an RF push-pull amplifier.

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic (2)	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 50 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	2.0	mAdc
Gate-Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS (2)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 50 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V, I_D = 3.0 A)	$V_{DS(on)}$	—	—	1.4	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.0 A)	g_{fs}	1.8	2.2	—	mhos
DYNAMIC CHARACTERISTICS (2)					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	110	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	105	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	10	—	pF
FUNCTIONAL CHARACTERISTICS (Figures 7 & 8) (4)					
Common Source Power Gain (3) (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 400 MHz, I_{DQ} = 200 mA)	G_{PS}	10	12	—	dB
Drain Efficiency (3) (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 400 MHz, I_{DQ} = 200 mA)	η	55	60	—	%
Electrical Ruggedness (3) (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 400 MHz, I_{DQ} = 200 mA, Load VSWR = 30:1, All Phase Angles At Frequency of Test)	ψ	No Degradation in Output Power Before & After Test			
TYPICAL INPUT/OUTPUT DEVICE IMPEDANCES					
MRF177					
Series Equivalent Input Impedance (V_{DD} = 28 V, I_{DQ} = 200 mA, P_{out} = 100 W, f = 400 MHz)	Z_{in}	—	2.35 + j0.4	—	Ohms
Series Equivalent Output Impedance (V_{DD} = 28 V, I_{DQ} = 200 mA, P_{out} = 100 W, f = 400 MHz)	Z_{out}	—	3.2 – j1.38	—	Ohms
MRF177M					
Series Equivalent Input Impedance (V_{DD} = 28 V, I_{DQ} = 200 mA, P_{out} = 100 W, f = 400 MHz)	Z_{in}	—	2.64 + j1.64	—	Ohms
Series Equivalent Output Impedance (V_{DD} = 28 V, I_{DQ} = 200 mA, P_{out} = 100 W, f = 400 MHz)	Z_{out}	—	3.15 + j0.05	—	Ohms

NOTES:
1. Note each transistor chip measured separately
2. Both transistor chips operating in push-pull amplifier
3. RF functional specification is the same for MRF177 & MRF177M

2

TYPICAL CHARACTERISTICS

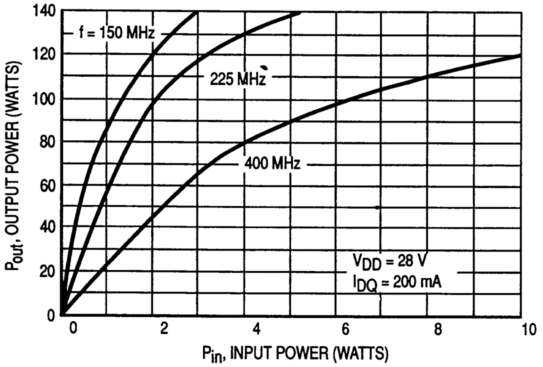


Figure 1. Output Power versus Input Power

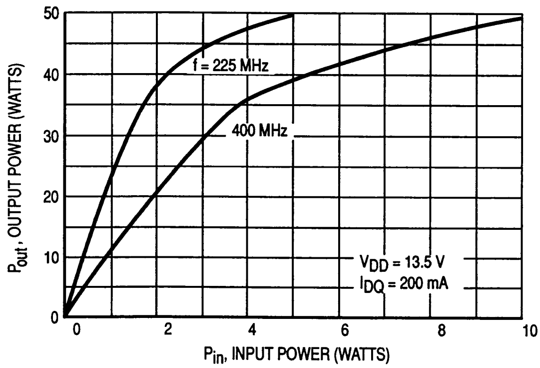


Figure 2. Output Power versus Input Power

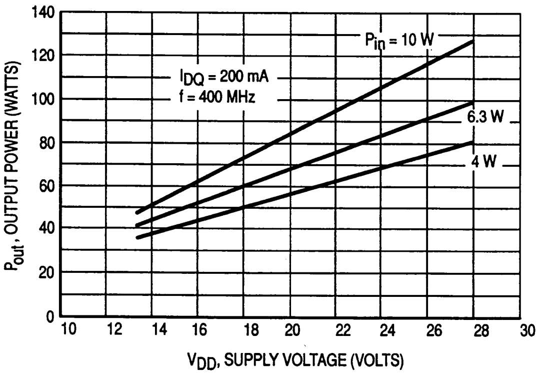


Figure 3. Output Power versus Supply Voltage

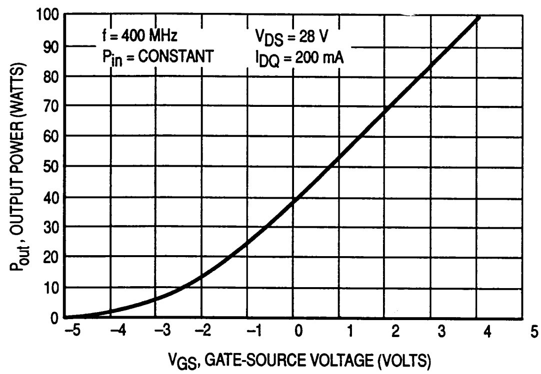


Figure 4. Output Power versus Gate Voltage

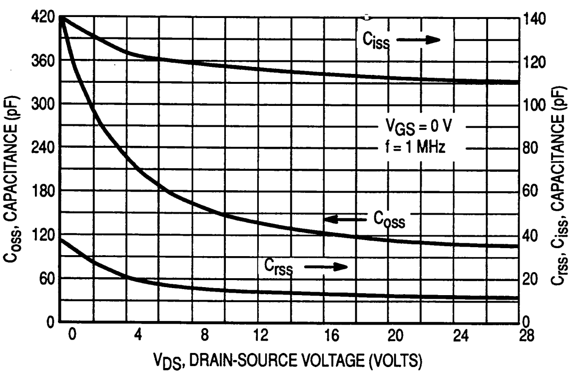


Figure 5. Capacitance versus Drain Voltage

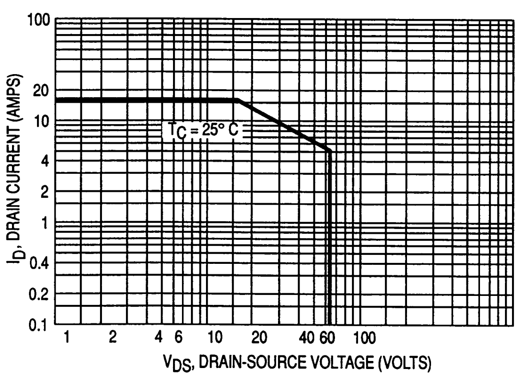
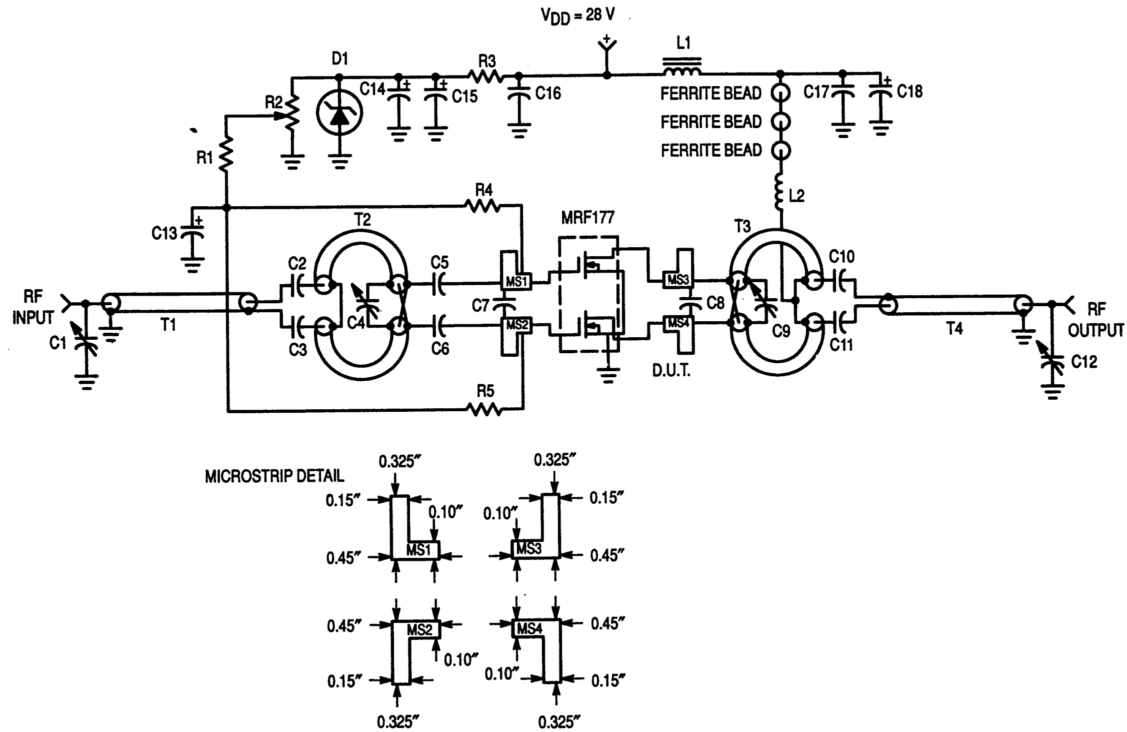


Figure 6. DC Safe Operating Area

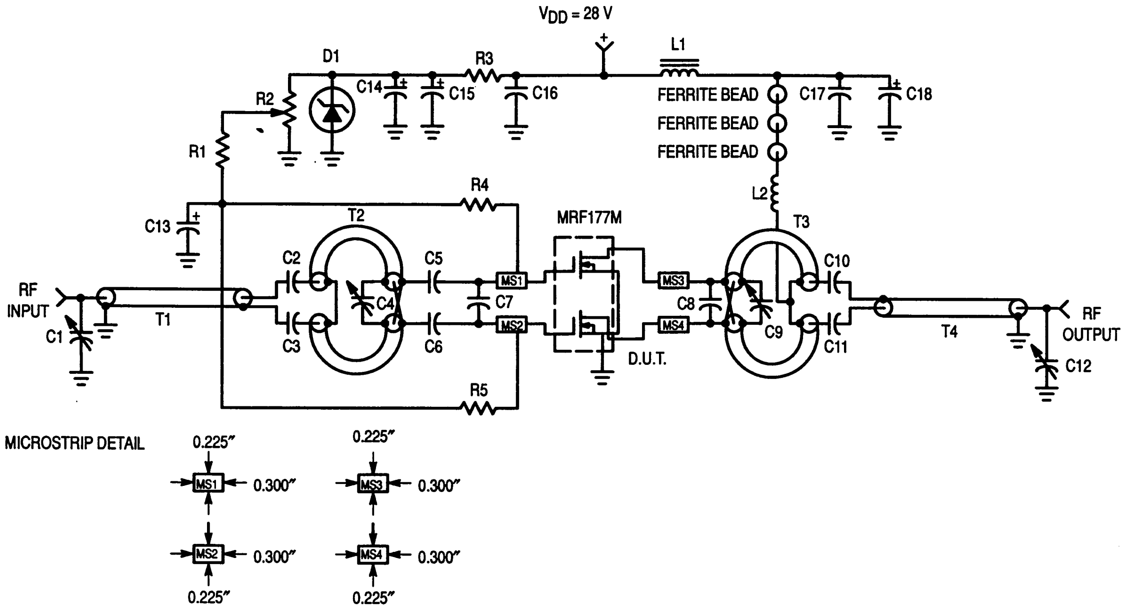
2



C1, C12	1–10 pF JOHANSON OR EQUIVALENT
C2, C3, C5, C6, C10, C11	270 pF ATC 100 MIL CHIP CAP
C4, C9	1–20 pF
C7	36 pF CHIP CAP
C8	10 pF CHIP CAP
C13, C14	0.1 μFD @ 50 Vdc
C15, C18	10 μFD @ 50 Vdc
C16	500 pF BUTTON
C17	1000 pF UNCASED MICA

D1	1N5347B, 20 Vdc
L1	1-TURN NO. 18, 0.25″, 2-HOLE FERRITE BEAD
L2	8-1/2 TURNS NO. 18, CLOSE WOUND .375″ DIA.
R1, R4, R5	10 kΩ @ 1/2 W RESISTOR
R2	10 kΩ, 10 TURN RESISTOR
R3	2.0 kΩ @ 1/2 W RESISTOR
T1	1-1/2 T, 50 Ω COAX, .034″ DIA. ON DUAL 0.5″ FERRITE CORE
T2	2.0″ 25 Ω COAX, .075″ DIA.
T3	2.1″ 10 Ω COAX, .075″ DIA.
T4	4.0″ 50 Ω COAX, .0865″ DIA.
BOARD	.0625″, Cu-Clad, Teflon Fiberglass, $\varepsilon_r = 2.55$

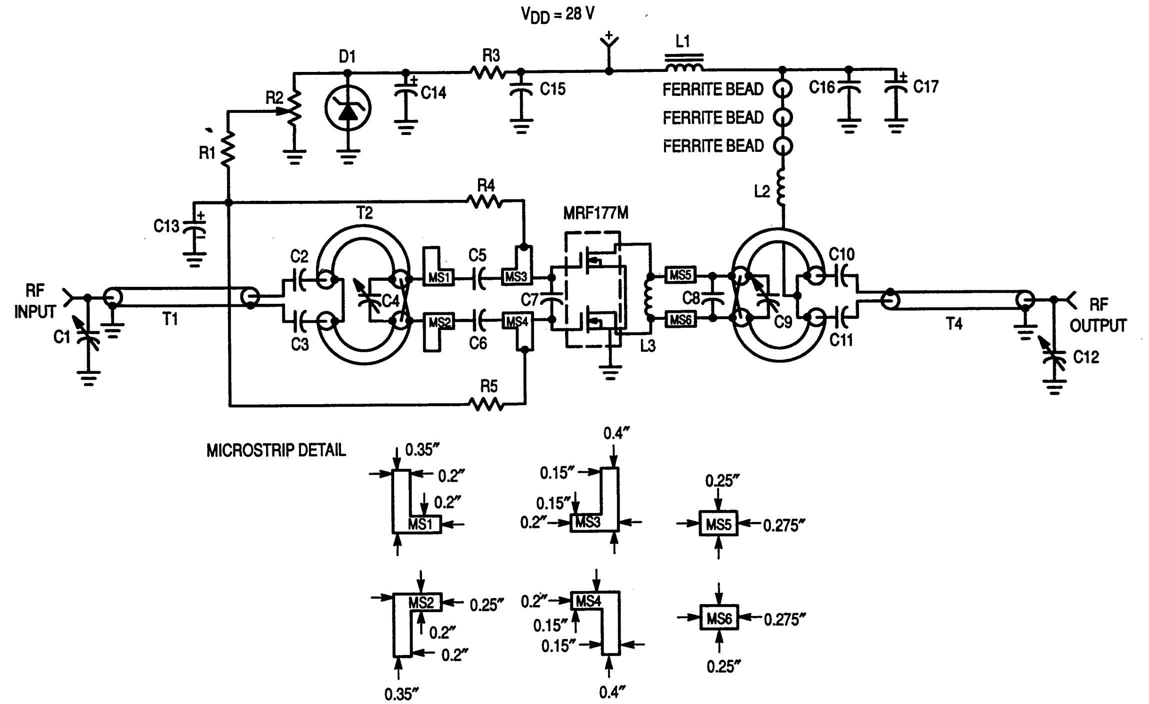
Figure 7. Test Circuit Electrical Schematic — MRF177



C1, C12	1–10 pF JOHANSON OR EQUIVALENT
C2, C3, C5, C6, C10, C11	270 pF ATC 100 MIL CHIP CAP
C4, C9	1–20 pF
C7	36 pF CHIP CAP
C8	10 pF CHIP CAP
C13, C14	0.1 μFD @ 50 Vdc
C15, C18	10 μFD @ 50 Vdc
C16	500 pF BUTTON
C17	1000 pF UNCASED MICA
D1	1N5347B, 20 Vdc MOTOROLA ZENER
L1	1-TURN NO. 18, 0.25″, 2-HOLE FERRITE BEAD
L2	8-1/2 TURNS NO. 18, CLOSE WOUND .375″ DIA.
R1, R4, R5	10 kΩ @ 1/2 W RESISTOR
R2	10 kΩ, 10 TURN RESISTOR
R3	2.0 kΩ @ 1/2 W RESISTOR
T1	1-1/2 T, 50 Ω COAX, .034″ DIA. ON DUAL 0.5″ FERRITE CORE
T2	2.0″ 25 Ω COAX, .075″ DIA.
T3	2.1″ 10 Ω COAX, .075″ DIA.
T4	4.0″ 50 Ω COAX, .0865″ DIA.
BOARD	.0625″, Cu-Clad, Teflon Fiberglass, ε_r = 2.55

Figure 8. Test Fixture Electrical Schematic — MRF177M

2



C1, C12	1–10 pF JOHANSON OR EQUIVALENT
C2, C3, C5, C6, C10, C11	270 pF ATC 100 MIL CHIP CAP
C4, C9	1–20 pF
C7	43 pF CHIP CAP
C8	10 pF CHIP CAP
C13, C14	0.1 μFD @ 50 Vdc
C15	500 pF BUTTON
C16	1000 pF UNCASED MICA
C17	10 μFD @ 50 Vdc

D1	1N5347B, 20 Vdc MOTOROLA ZENER
L1	1-TURN NO. 18, 0.25″, 2-HOLE FERRITE BEAD
L2	8-1/2 TURNS NO. 18, CLOSE WOUND .375″ DIA.
L3	4-TURNS NO. 22, 1/8″ DIA., 0.25″ LONG
R1, R4, R5	10 kΩ @ 1/2 W RESISTOR
R2	10 kΩ, 10 TURN RESISTOR
R3	2.0 kΩ @ 1/2 W RESISTOR
T1	1-1/2 T, 50 Ω COAX, .034″ DIA. ON DUAL 0.5″ FERRITE CORE
T2	2.0″ 25 Ω COAX, .075″ DIA.
T3	2.1″ 10 Ω COAX, .075″ DIA.
T4	4.0″ 50 Ω COAX, .0865″ DIA.
BOARD	.0625″, Cu-Clad, Teflon Fiberglass, $\varepsilon_r = 2.55$

Figure 9. Broadband Amplifier Schematic — MRF177M

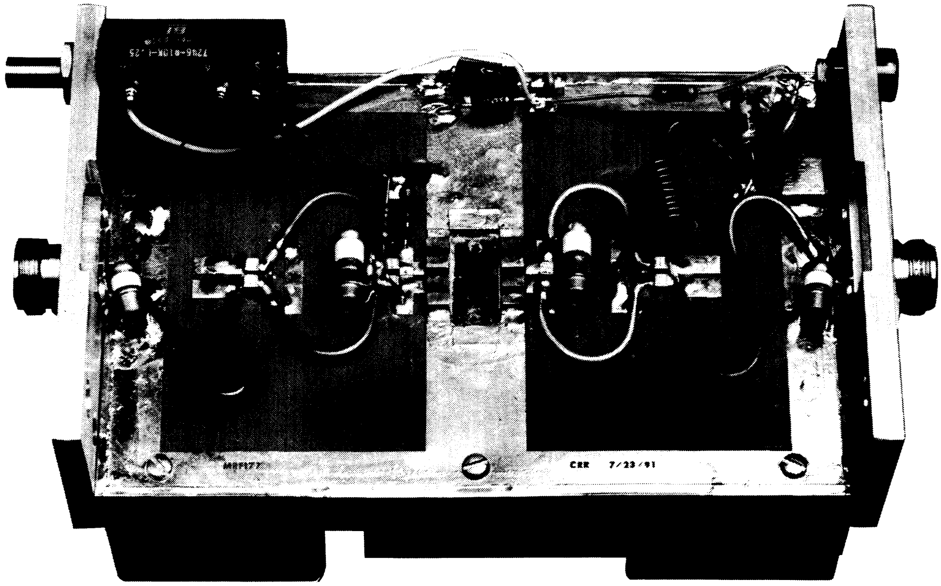
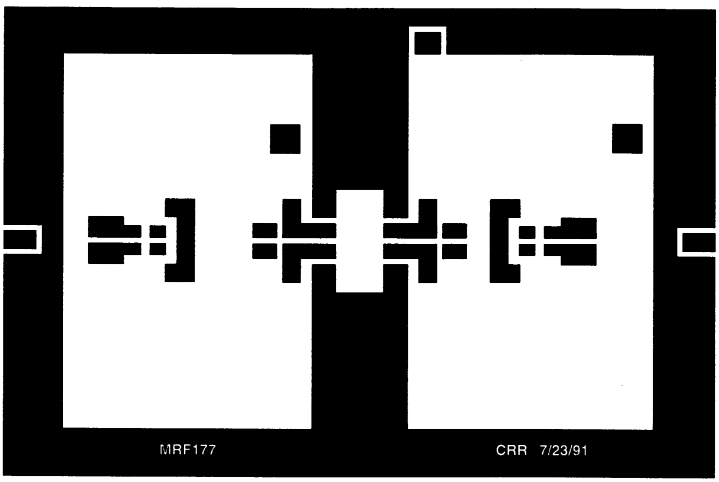


Figure 10. Test Fixture — MRF177

2



(Not to Scale)

Figure 11. Photomaster for MRF177 Test Fixture

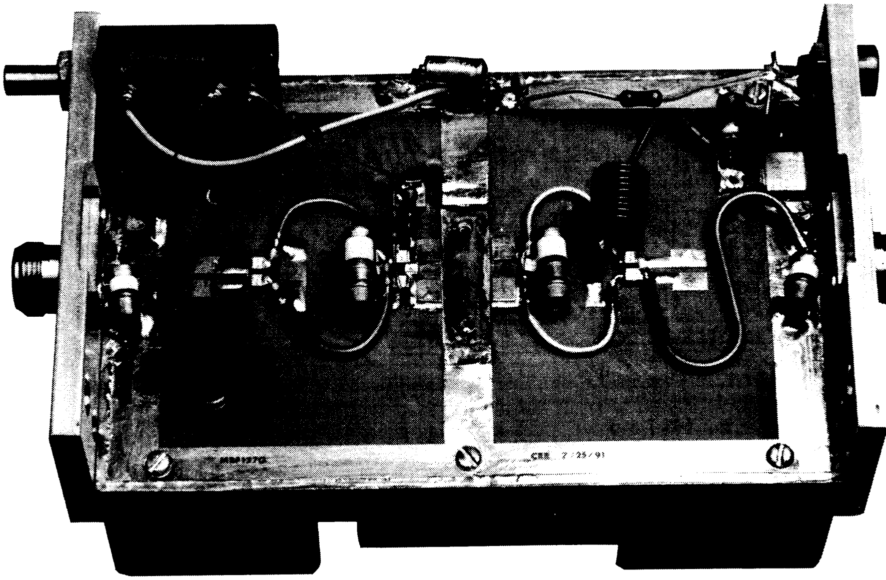
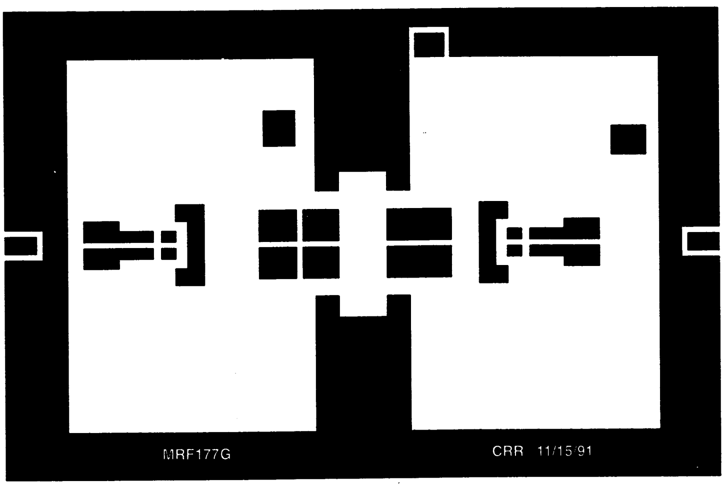


Figure 12. Test Fixture — MRF177M



(Not to Scale)

Figure 13 — Photomaster for MRF177M Test Fixture

MRF182

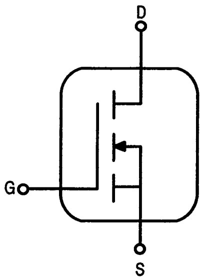
Motorola Preferred Device

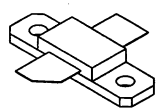
Advance Information

The RF MOSFET Line
RF Power
Field Effect Transistors
N-Channel Enhancement-Mode Lateral MOSFETs

30 W, 1.0 GHz, 28 VOLTS
LATERAL N-CHANNEL
BROADBAND RF POWER
MOSFET

- High gain, rugged device
- Broadband performance from HF to 1 GHz.
- Bottom side source eliminates DC isolators, reducing common mode inductances.





CASE 360B, STYLE 1

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 1 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	1	mAdc
Gate-Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1	µAdc

(continued)

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 50 mA)	$V_{GS(th)}$	1	3	5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V, I_D = 1 A)	$V_{DS(on)}$	—	0.34	—	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 3 A)	g_{fs}	—	1.8	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	53	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	26	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	2.6	—	pF
FUNCTIONAL CHARACTERISTICS					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 30 W, I_{DQ} = 50 mA, f = 1 GHz)	G_{ps}	—	13	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 30 W, I_{DQ} = 50 mA, f = 1 GHz)	η	—	55	—	%
Series Equivalent Input Impedance (V_{DD} = 28 Vdc, P_{out} = 30 W, I_{DQ} = 50 mA, f = 1 GHz)	Z_{in}	—	0.63 + j1.1	—	ohms
Series Equivalent Output Impedance (V_{DD} = 28 Vdc, P_{out} = 30 W, I_{DQ} = 50 mA, f = 1 GHz)	Z_{out}	—	1.70 – j2.3	—	ohms

TYPICAL CHARACTERISTICS

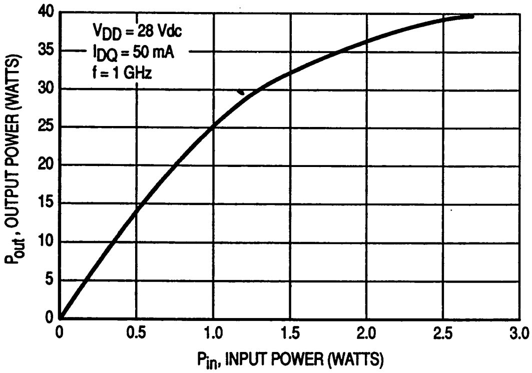


Figure 1. Output Power versus Input Power at 1 GHz

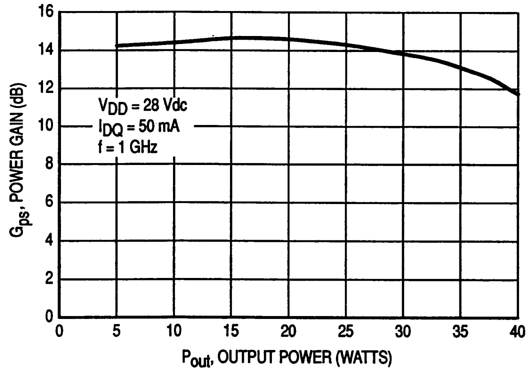


Figure 2. Power Gain versus Output Power at 1 GHz

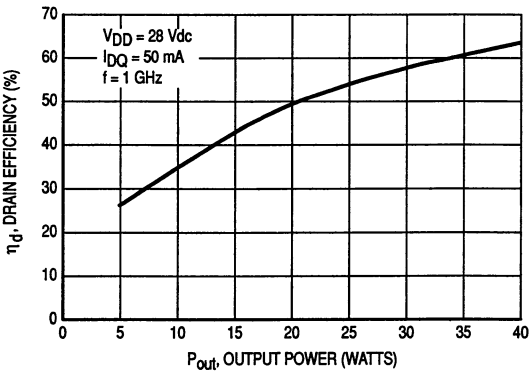


Figure 3. Drain Efficiency versus Output Power at 1 GHz

2

MRF183

Motorola Preferred Device

Advance Information

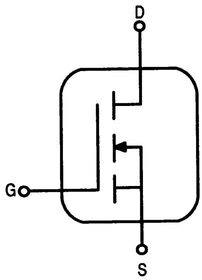
The RF MOSFET Line

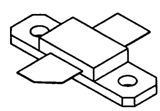
RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

45 W, 1.0 GHz, 28 VOLTS
LATERAL N-CHANNEL
BROADBAND RF POWER
MOSFET

- High gain, rugged device
- Broadband performance from HF to 1 GHz.
- Bottom side source eliminates DC isolators, reducing common mode inductances.





CASE 360B, STYLE 1

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 1 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	1	mAdc
Gate-Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1	µAdc

(continued)

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 75 mA)	$V_{GS(th)}$	1	3	5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V, I_D = 1 A)	$V_{DS(on)}$	—	0.23	—	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 3 A)	g_{fs}	—	2.6	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	82	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	38	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	3.8	—	pF
FUNCTIONAL CHARACTERISTICS					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 45 W, I_{DQ} = 75 mA, f = 1 GHz)	G_{ps}	—	12	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 45 W, I_{DQ} = 75 mA, f = 1 GHz)	η	—	55	—	%
Series Equivalent Input Impedance (V_{DD} = 28 Vdc, P_{out} = 45 W, I_{DQ} = 75 mA, f = 1 GHz)	Z_{in}	—	0.65 + j0.24	—	ohms
Series Equivalent Output Impedance (V_{DD} = 28 Vdc, P_{out} = 45 W, I_{DQ} = 75 mA, f = 1 GHz)	Z_{out}	—	1.38 – j1.89	—	ohms

TYPICAL CHARACTERISTICS

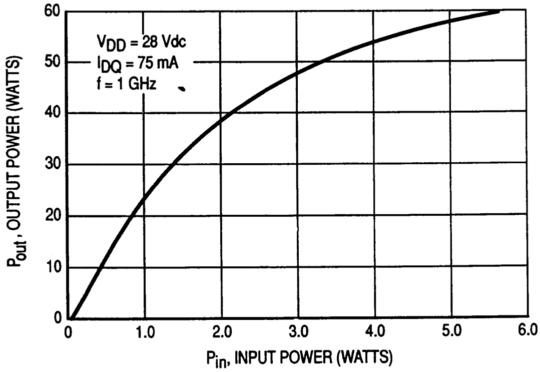


Figure 1. Output Power versus Input Power at 1 GHz

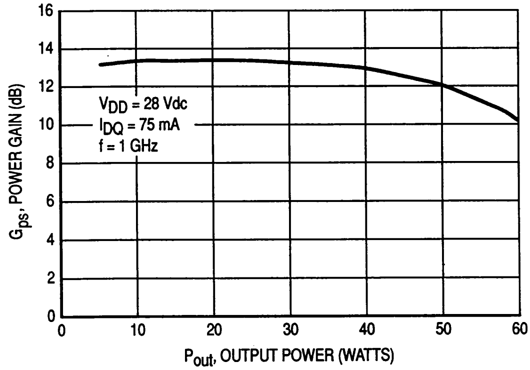


Figure 2. Power Gain versus Output Power at 1 GHz

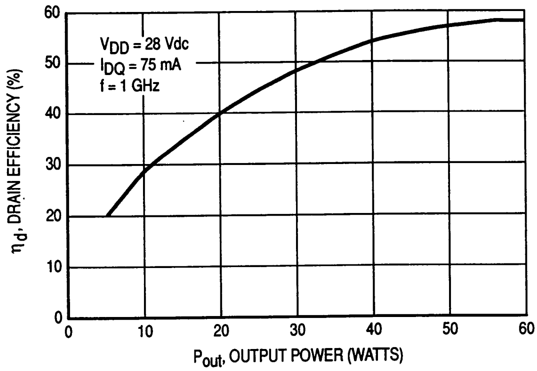


Figure 3. Drain Efficiency versus Output Power at 1 GHz