

The RF MOSFET Line  
**RF Power Field Effect Transistor**  
**N-Channel Enhancement-Mode**

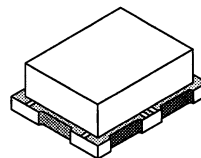
The MRF5003 is designed for broadband commercial and industrial applications at frequencies to 520 MHz. The high gain and broadband performance of this device makes it ideal for large-signal, common source amplifier applications in 7.5 Volt and 12.5 Volt mobile, portable, and base station FM equipment.

- Guaranteed Performance at 512 MHz, 7.5 Volts  
 Output Power = 3.0 Watts  
 Power Gain = 9.5 dB  
 Efficiency = 45%
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- S-Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- All Gold Metal for Ultra Reliability
- Capable of Handling 20:1 VSWR, @ 15.5 Vdc, 512 MHz, 2.0 dB Overdrive
- Suitable for 12.5 Volt Applications
- True Surface Mount Package
- Available in Tape and Reel

**MRF5003**

Motorola Preferred Device

**3.0 W, 7.5 V, 512 MHz**  
**N-CHANNEL**  
**BROADBAND**  
**RF POWER FET**



CASE 430, STYLE 2

**2**

**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DSS</sub>	36	Vdc
Drain-Gate Voltage (R <sub>GS</sub> = 1.0 Meg Ohm)	V <sub>DGR</sub>	36	Vdc
Gate-Source Voltage	V <sub>GS</sub>	±20	Vdc
Drain Current — Continuous	I <sub>D</sub>	1.7	Adc
Total Device Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C	P <sub>D</sub>	12.5 0.07	Watts W/°C
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Operating Junction Temperature	T <sub>J</sub>	200	°C

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R <sub>θJC</sub>	14	°C/W

**NOTE — CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Preferred devices are Motorola recommended choices for future use and best overall value.

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

Drain-Source Breakdown Voltage ( $V_{GS} = 0$ , $I_D = 2.5$ mAdc)	$V_{(BR)DSS}$	36	—	—	Vdc
Zero Gate Voltage Drain Current ( $V_{DS} = 15$ Vdc, $V_{GS} = 0$ )	$I_{DSS}$	—	—	1.0	mAdc
Gate-Source Leakage Current ( $V_{GS} = 20$ Vdc, $V_{DS} = 0$ )	$I_{GSS}$	—	—	1.0	$\mu\text{Adc}$

**ON CHARACTERISTICS**

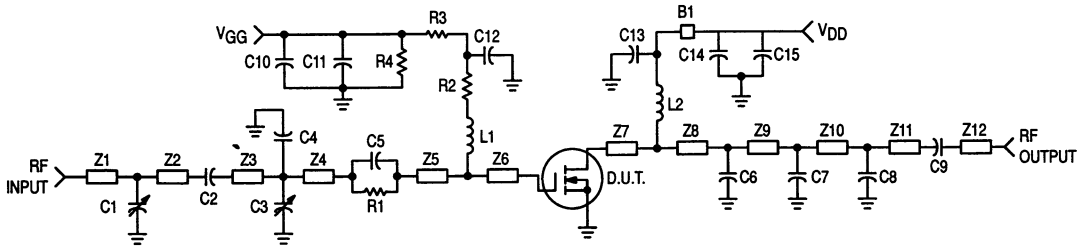
Gate Threshold Voltage ( $V_{DS} = 10$ Vdc, $I_D = 5.0$ mAdc)	$V_{GS(th)}$	1.25	2.25	3.5	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10$ Vdc, $I_D = 0.5$ Adc)	$V_{DS(on)}$	—	—	0.375	Vdc
Forward Transconductance ( $V_{DS} = 10$ Vdc, $I_D = 0.5$ Adc)	$g_{fs}$	0.6	—	—	mho

**DYNAMIC CHARACTERISTICS**

Input Capacitance ( $V_{DS} = 12.5$ Vdc, $V_{GS} = 0$ , $f = 1.0$ MHz)	$C_{iss}$	—	16.5	—	pF
Output Capacitance ( $V_{DS} = 12.5$ Vdc, $V_{GS} = 0$ , $f = 1.0$ MHz)	$C_{oss}$	—	37	—	pF
Reverse Transfer Capacitance ( $V_{DS} = 12.5$ Vdc, $V_{GS} = 0$ , $f = 1.0$ MHz)	$C_{rss}$	3.5	4.4	5.4	pF

**FUNCTIONAL TESTS** (In Motorola Test Fixture)

Common-Source Amplifier Power Gain ( $V_{DD} = 7.5$ Vdc, $P_{out} = 3.0$ W, $I_{DQ} = 50$ mA)	$f = 512$ MHz $f = 175$ MHz	$G_{ps}$	9.5 —	10.5 15	— —	dB
Drain Efficiency ( $V_{DD} = 7.5$ Vdc, $P_{out} = 3.0$ W, $I_{DQ} = 50$ mA)	$f = 512$ MHz $f = 175$ MHz	$h$	45 —	50 55	— —	%



- |  |  |                                  |                                    |
|--|--|----------------------------------|------------------------------------|
| C1, C3, C7, C8   | 0 to 20 pF Johanson                                | Z1                               | 0.350" x 0.08" Microstrip          |
| C2, C9   | 56 pF, 100 mil Chip                                | Z2                               | 0.190" x 0.08" Microstrip          |
| C4   | 10 pF, 100 mil Chip                                | Z3                               | 0.800" x 0.08" Microstrip          |
| C5   | 47 pF, Miniature Clamped Mica Capacitor            | Z4                               | 0.380" x 0.08" Microstrip          |
| C6   | 22 pF, 100 mil Chip                                | Z5                               | 0.150" x 0.08" Microstrip          |
| C10, C15   | 10 $\mu$ F, 50 V, Electrolytic                     | Z6                               | 0.285" x 0.08" Microstrip          |
| C11, C14   | 0.1 $\mu$ F, Capacitor                             | Z7                               | 0.340" x 0.08" Microstrip          |
| C12  | 1000 pF, 100 mil Chip                              | Z8                               | 0.070" x 0.08" Microstrip          |
| C13  | 160 pF, 100 mil Chip                               | Z9                               | 0.280" x 0.08" Microstrip          |
| R1   | 35 $\Omega$ , 1/4 W Carbon                         | Z10                              | 0.840" x 0.08" Microstrip          |
| R2   | 30 $\Omega$ , 0.1 W Chip                           | Z11                              | 0.180" x 0.08" Microstrip          |
| R3   | 1.0 k $\Omega$ , 0.1 W Chip                        | Z12                              | 0.600" x 0.08" Microstrip          |
| R4   | 1.0 M $\Omega$ , 1/4 W Carbon                      | L1                               | 7 Turns, 0.076" ID, #24 AWG Enamel |
| B1   | Fair Rite Products Short Ferrite Bead (2743021446) | L2                               | 5 Turns, 0.126" ID, #20 AWG Enamel |
| Board — Glass Teflon <sup>®</sup> , 31 mils                                |  | Input/Output Connectors — Type N |                                    |
| Note: Plated ceramic part locators (0.1" x 0.15") soldered onto Z6 and Z7. |  |                                  |                                    |

Figure 1. 512 MHz Narrowband Test Circuit

### TYPICAL CHARACTERISTICS

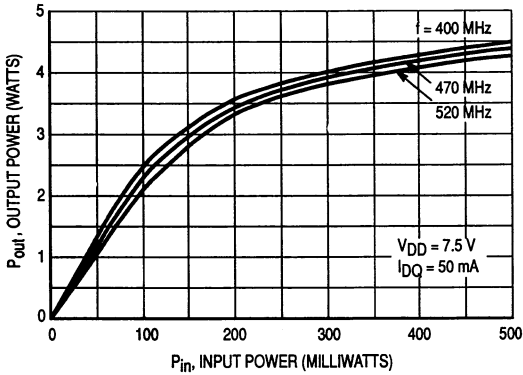


Figure 2. Output Power versus Input Power

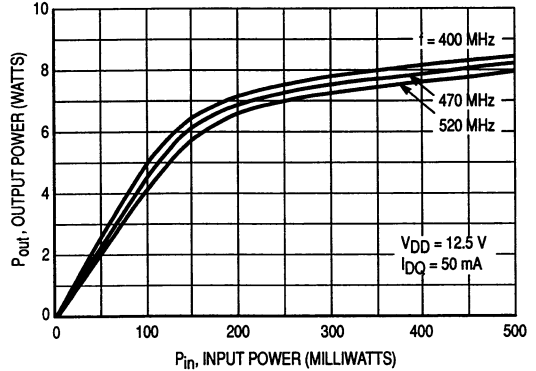


Figure 3. Output Power versus Input Power

## TYPICAL CHARACTERISTICS

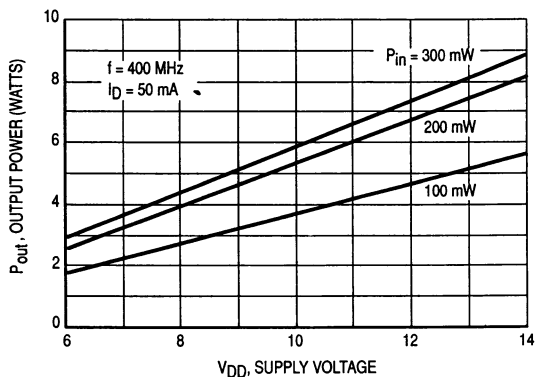


Figure 4. Output Power versus Supply Voltage

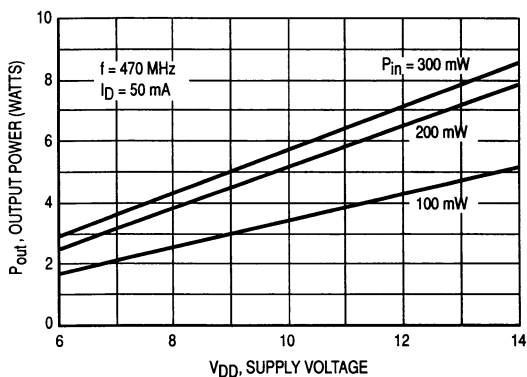


Figure 5. Output Power versus Supply Voltage

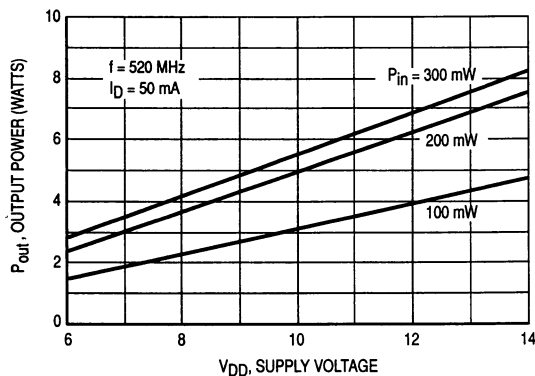


Figure 6. Output Power versus Supply Voltage

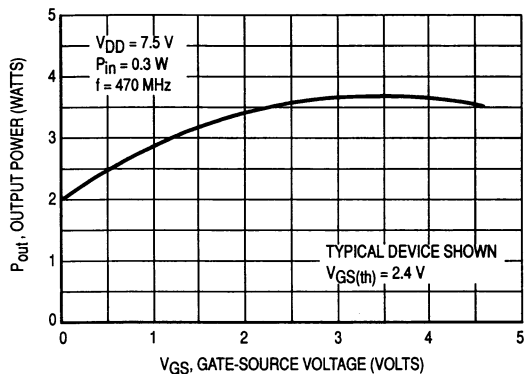


Figure 7. Output Power versus Gate Voltage

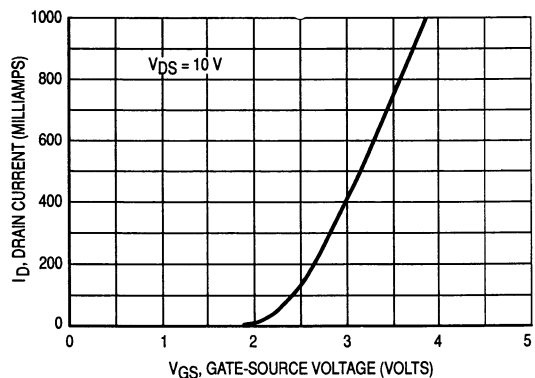


Figure 8. Drain Current versus Gate Voltage  
(Typical Device Shown)

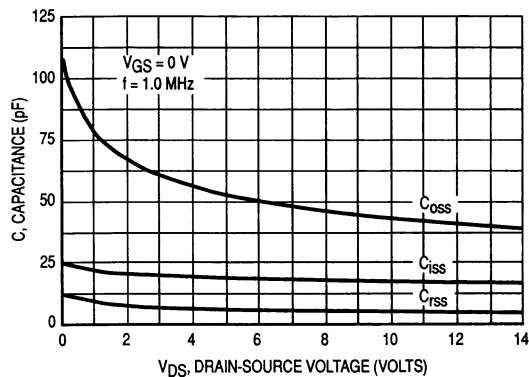


Figure 9. Capacitance versus Voltage

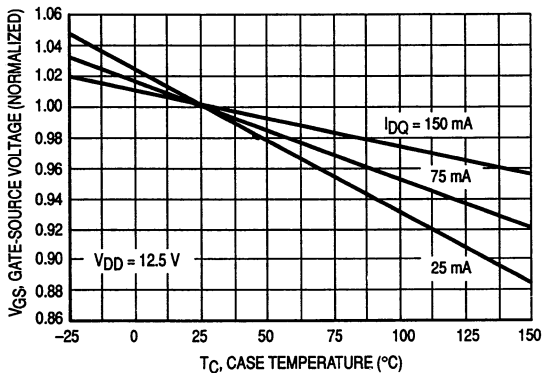


Figure 10. Gate-Source Voltage versus Case Temperature

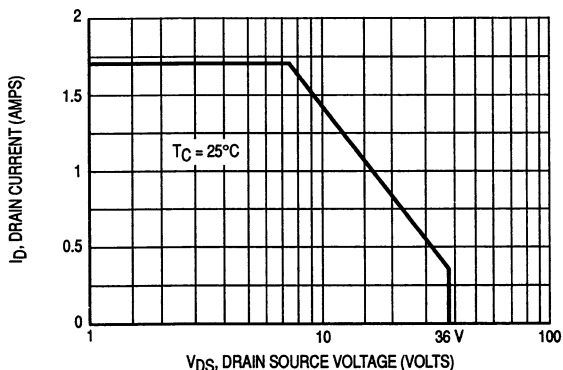
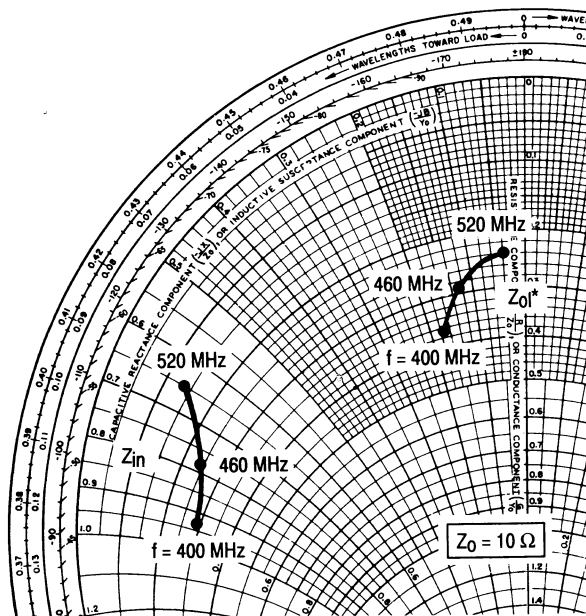


Figure 11. Maximum Rated Forward Biased Safe Operating Area



$V_{DD} = 7.5\text{ V}$   $I_{DQ} = 50\text{ mA}$   $P_{out} = 3.0\text{ W}$

f MHz	$Z_{in}$ $\Omega$	$Z_{ol}^*$ $\Omega$
400	2.8 - j9.2	3.6 - j1.7
430	2.7 - j8.5	3.3 - j1.5
460	2.5 - j7.8	2.7 - j1.1
490	2.0 - j7.2	2.5 - j0.8
520	1.3 - j6.5	2.4 - j0.5

$Z_{in}$  = Conjugate of source impedance with parallel 35  $\Omega$  resistor and 47 pF capacitor in series with gate

$Z_{ol}^*$  = Conjugate of the load impedance at given output power, voltage, frequency, and  $\eta_D > 50\%$

Note:  $Z_{ol}^*$  was chosen based on tradeoffs between gain, drain efficiency, and device stability.

Figure 12. Series Equivalent Input and Output Impedance

**Table 1. Common Source Scattering Parameters ( $V_{DS} = 10\text{ V}$ )**

**$I_D = 50\text{ mA}$**

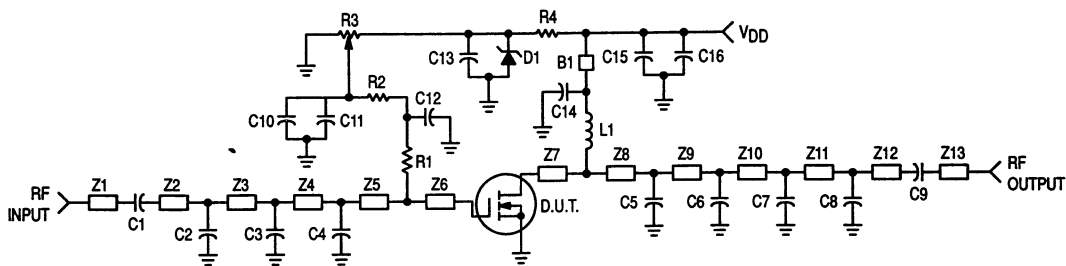
f	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	S <sub>11</sub>	∠φ	S <sub>21</sub>	∠φ	S <sub>12</sub>	∠φ	S <sub>22</sub>	∠φ
50	0.69	-90	10.8	117	0.07	29	0.74	-119
100	0.58	-120	6.0	96	0.08	10	0.78	-146
200	0.58	-139	3.0	75	0.08	-7	0.81	-161
300	0.64	-147	1.9	61	0.07	-16	0.84	-166
400	0.70	-152	1.3	50	0.06	-21	0.86	-169
500	0.75	-157	0.99	41	0.05	-24	0.88	-172
700	0.82	-165	0.61	28	0.03	-15	0.92	-176
850	0.86	-171	0.45	21	0.02	13	0.94	-179
1000	0.89	-176	0.34	16	0.02	47	0.95	178

**$I_D = 500\text{ mA}$**

f	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	S <sub>11</sub>	∠φ	S <sub>21</sub>	∠φ	S <sub>12</sub>	∠φ	S <sub>22</sub>	∠φ
50	0.76	-124	15.0	109	0.04	23	0.76	-151
100	0.72	-150	7.9	94	0.04	12	0.81	-165
200	0.72	-163	4.0	80	0.04	6	0.83	-172
300	0.73	-168	2.6	71	0.04	5	0.84	-175
400	0.75	-171	1.9	62	0.04	7	0.85	-176
500	0.77	-173	1.5	55	0.03	12	0.86	-178
700	0.81	-177	0.97	42	0.03	29	0.89	-180
850	0.84	-180	0.75	35	0.03	44	0.90	178
1000	0.86	177	0.60	29	0.04	55	0.92	176

**$I_D = 1.0\text{ A}$**

f	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	S <sub>11</sub>	∠φ	S <sub>21</sub>	∠φ	S <sub>12</sub>	∠φ	S <sub>22</sub>	∠φ
50	0.80	-125	14.6	110	0.04	23	0.75	-155
100	0.76	-150	7.8	95	0.04	10	0.81	-167
200	0.76	-164	3.9	81	0.04	1	0.83	-173
300	0.77	-169	2.6	71	0.04	-3	0.84	-175
400	0.79	-172	1.9	63	0.03	-5	0.85	-176
500	0.80	-174	1.4	56	0.03	-5	0.86	-177
700	0.83	-178	0.95	43	0.03	-1	0.88	-179
850	0.85	179	0.73	35	0.02	9	0.90	179
1000	0.87	177	0.58	28	0.02	22	0.91	178



- |          |  |                         |                                     |
|----------|--|-------------------------|-------------------------------------|
| C1, C9   | 100 pF 100 mil Chip                                | C13                     | 0.1 $\mu$ F, 100 mil Chip           |
| C2       | 16 pF, 100 mil Chip                                | C14                     | 160 pF, 100 mil Chip                |
| C3       | 24 pF, 100 mil Chip                                | R1                      | 43 $\Omega$ , 0.1 W Chip Resistor   |
| C4       | 68 pF, 100 mil Chip                                | R2                      | 1000 $\Omega$ , 0.1 W Chip Resistor |
| C5       | 51 pF, 100 mil Chip                                | R3                      | 10 k $\Omega$ Potentiometer         |
| C6       | 39 pF, 100 mil Chip                                | R4                      | 3000 $\Omega$ , 0.1 W Chip Resistor |
| C7       | 6.2 pF, 100 mil Chip                               | L1                      | 5 Turns, 0.126" ID, #20 AWG Enamel  |
| C8       | 9.1 pF, 100 mil Chip                               | Z1 to Z13               | See Photomaster                     |
| C10, C15 | 39000 pF, 100 mil Chip                             | D1                      | 1N4734 Motorola Zener               |
| C11, C16 | 10 $\mu$ F, 50 V Electrolytic                      | Board                   | — G10, 1/32"                        |
| C12      | 10000 pF, 100 mil Chip                             | Input/Output Connectors | — SMA                               |
| B1       | Fair Rite Products Short Ferrite Bead (2743021446) |                         |                                     |

Figure 13. Schematic of Broadband Demonstration Amplifier

## PERFORMANCE CHARACTERISTICS OF BROADBAND DEMONSTRATION AMPLIFIER

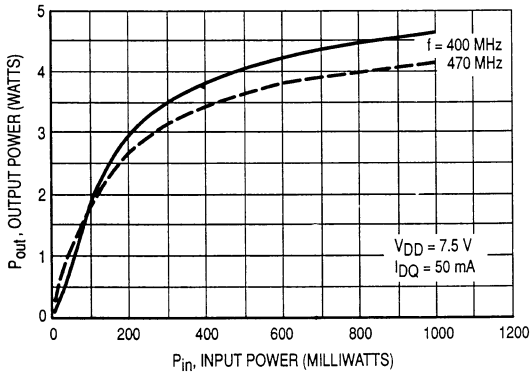


Figure 14. Output Power versus Input Power

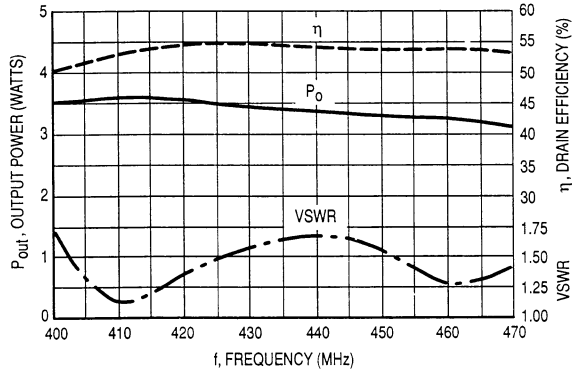


Figure 15. Output Power, Drain Efficiency and VSWR versus Frequency

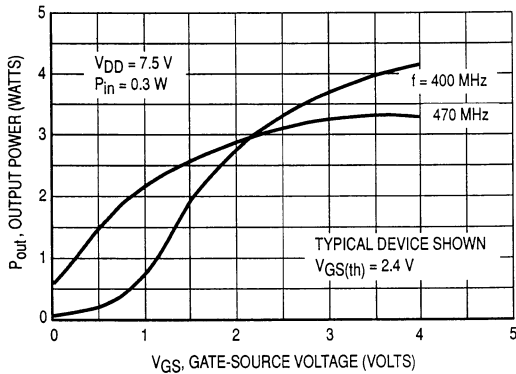


Figure 16. Output Power versus Gate Voltage

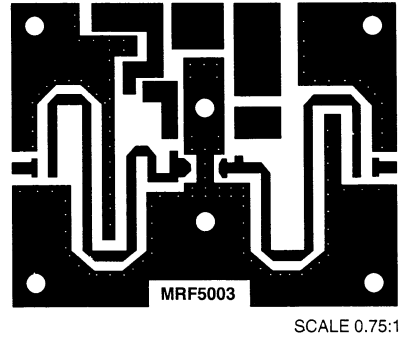


Figure 17. Photomaster for 400–470 MHz Broadband Demonstration Amplifier

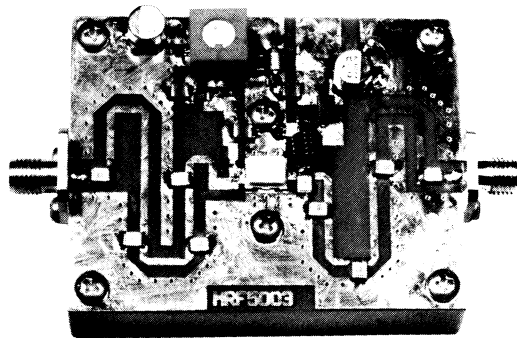


Figure 18. 512 MHz Broadband Test Circuit



## DESIGN CONSIDERATIONS

The MRF5003 is a common-source, RF power, N-Channel enhancement mode, Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET). Motorola RF MOSFETs feature a vertical structure with a planar design. Motorola Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts.

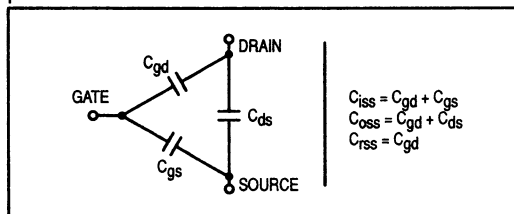
The major advantages of RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

## MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate-to-drain ( $C_{gd}$ ), and gate-to-source ( $C_{gs}$ ). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain-to-source ( $C_{ds}$ ). These capacitances are characterized as input ( $C_{iss}$ ), output ( $C_{oss}$ ) and reverse transfer ( $C_{rss}$ ) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The  $C_{iss}$  can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



## DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full-on condition. This on-resistance,  $R_{DS(on)}$ , occurs in the linear region of the output characteristic and is specified at a specific gate-source voltage and drain current. The drain-source voltage under these conditions is termed  $V_{DS(on)}$ . For MOSFETs,  $V_{DS(on)}$  has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

## GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of  $10^9 \Omega$  — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate-to-source threshold voltage,  $V_{GS(th)}$ .

**Gate Voltage Rating** — Never exceed the gate voltage rating. Exceeding the rated  $V_{GS}$  can result in permanent damage to the oxide layer in the gate region.

**Gate Termination** — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

**Gate Protection** — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended with appropriate RF decoupling.

Using a resistor to keep the gate-to-source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

## DC BIAS

Since the MRF5003 is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. See Figure 8 for a typical plot of drain current versus gate voltage. RF power FETs operate optimally with a quiescent drain current ( $I_{DQ}$ ), whose value is application dependent. The MRF5003 was characterized at  $I_{DQ} = 50$  mA, which is the suggested value of bias current for typical applications. For special applications such as linear amplification,  $I_{DQ}$  may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

## GAIN CONTROL

Power output of the MRF5003 may be controlled from its rated value down to zero (negative gain) with a low power dc control signal, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. Figure 16 is an example of output power variation with gate-source bias voltage. This characteristic is very dependent on frequency and load line.

## MOUNTING

The specified maximum thermal resistance of  $14^\circ\text{C/W}$  assumes a majority of the  $0.100'' \times 0.200''$  source contact on the back side of the package is in good contact with an appropriate heat sink. In the test fixture shown in Figure 1, the device is clamped directly to a copper pedestal. In the demonstration amplifier, the device was mounted on top of the G10 circuit board and heat removal was accomplished through several solder filled plated through holes. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package.

## AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for the MRF5003. For examples see Motorola Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors". Both small-signal S-parameters and large-signal impedances are provided. While the S-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF power MOSFETs.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of the MRF5003 yield a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input

shunt resistive loading, or output to input feedback. Different stabilizing techniques were applied to the test fixture and demonstration amplifiers. The RF test fixture implements a parallel resistor and capacitor in series with the gate while the demonstration amplifier utilizes a  $43\ \Omega$  shunt resistor from gate to ground. Both circuits have a load line selected for a higher efficiency, lower gain, and more stable operating region.

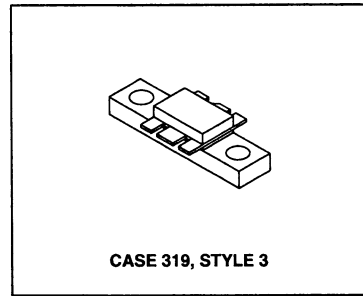
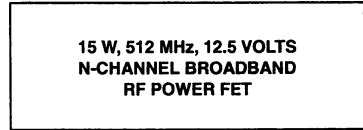
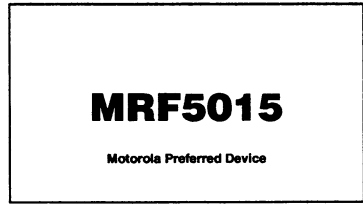
Two port stability analysis with the MRF5003 S-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, "RF Small-Signal Design Using Two-Port Parameters", for a discussion of two port network theory and stability.

*Advance Information*

**The RF MOSFET Line**  
**RF Power Field Effect Transistor**  
**N-Channel Enhancement-Mode**

Designed for broadband commercial and industrial applications at frequencies to 520 MHz. The high gain and broadband performance of this device makes it ideal for large-signal, common source amplifier applications in 12.5 volt mobile, and base station FM equipment.

- Guaranteed Performance at 512 MHz, 12.5 Volts  
 Output Power — 15 Watts  
 Power Gain — 10 dB Min  
 Efficiency — 50% Min
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- S-Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- All Gold Metal for Ultra Reliability
- Capable of Handling 20:1 VSWR, @ 15.5 Vdc, 512 MHz, 2 dB Overdrive



**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V <sub>CEO</sub>	20	Vdc
Drain-Source Voltage	V <sub>DSS</sub>	36	Vdc
Drain-Gate Voltage (R <sub>GS</sub> = 1 MΩ)	V <sub>DGR</sub>	36	Vdc
Gate-Source Voltage	V <sub>GS</sub>	± 20	Vdc
Drain Current — Continuous	I <sub>D</sub>	6	Adc
Total Device Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C	P <sub>D</sub>	50 0.29	Watts W/°C
Storage Temperature Range	T <sub>stg</sub>	- 65 to +150	°C
Operating Junction Temperature	T <sub>J</sub>	200	°C

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R <sub>θJC</sub>	3.5	°C/W

**ELECTRICAL CHARACTERISTICS** (T<sub>C</sub> = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

Drain-Source Breakdown Voltage (V <sub>GS</sub> = 0, I <sub>D</sub> = 5 mAdc)	V <sub>(BR)DSS</sub>	36	—	—	Vdc
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 15 Vdc, V <sub>GS</sub> = 0)	I <sub>DSS</sub>	—	—	5	mAdc
Gate-Source Leakage Current (V <sub>GS</sub> = 20 Vdc, V <sub>DS</sub> = 0)	I <sub>GSS</sub>	—	—	2	μAdc

(continued)

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

This document contains information on a new product. Specifications and information herein are subject to change without notice.  
 Preferred devices are Motorola recommended choices for future use and best overall value.

**ELECTRICAL CHARACTERISTICS — continued** ( $T_C = 25^\circ\text{C}$  unless otherwise noted.)

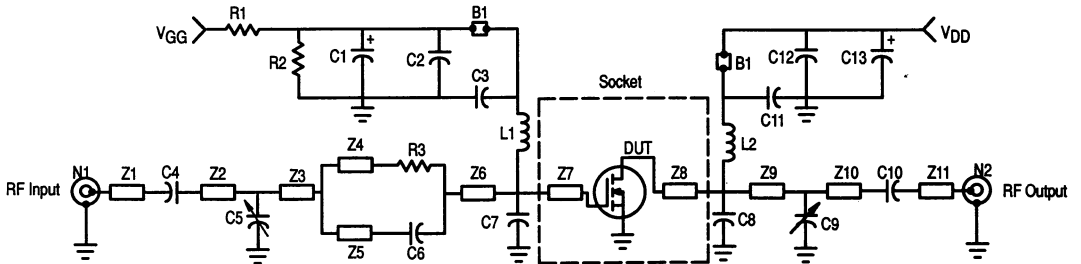
Characteristic	Symbol	Min	Typ	Max	Unit
<b>ON CHARACTERISTICS</b>					
Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 10\text{ mA}$ )	$V_{GS(th)}$	1.25	2.3	3.5	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 1\text{ Adc}$ )	$V_{DS(on)}$	—	—	0.375	Vdc
Forward Transconductance ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 1\text{ Adc}$ )	$g_{fs}$	1.2	—	—	S

**DYNAMIC CHARACTERISTICS**

Input Capacitance ( $V_{DS} = 12.5\text{ Vdc}$ , $V_{GS} = 0$ , $f = 1\text{ MHz}$ )	$C_{iss}$	—	33	—	pF
Output Capacitance ( $V_{DS} = 12.5\text{ Vdc}$ , $V_{GS} = 0$ , $f = 1\text{ MHz}$ )	$C_{oss}$	—	74	—	pF
Reverse Transfer Capacitance ( $V_{DS} = 12.5\text{ Vdc}$ , $V_{GS} = 0$ , $f = 1\text{ MHz}$ )	$C_{rss}$	7	8.8	10.8	pF

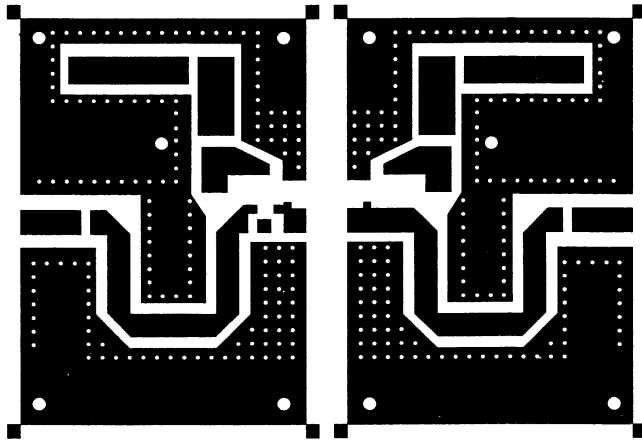
**FUNCTIONAL TESTS** (in Motorola Test Fixture)

Common-Source Amplifier Power Gain ( $V_{DD} = 12.5\text{ Vdc}$ , $P_{out} = 15\text{ W}$ , $I_{DQ} = 100\text{ mA}$ ) $f = 512\text{ MHz}$ $f = 175\text{ MHz}$	$G_{ps}$	10 —	11.5 15	— —	dB
Drain Efficiency ( $V_{DD} = 12.5\text{ Vdc}$ , $P_{out} = 15\text{ W}$ , $I_{DQ} = 100\text{ mA}$ ) $f = 512\text{ MHz}$ $f = 175\text{ MHz}$	$\eta$	50 —	55 55	— —	%
Load Mismatch ( $V_{DD} = 15.5\text{ Vdc}$ , 2 dB Overdrive, $f = 512\text{ MHz}$ , Load VSWR = 20:1, All Phase Angles at Frequency of Test)	$\psi$	No Degradation in Output Power			



B1, B2	Ferrite Bead, Fair Rite Products	R3	160 $\Omega$ , 0.1 W Chip
C1, C13	10 $\mu\text{F}$ , 50 V, Electrolytic	Z1, Z11	Transmission Line*
C2, C12	0.1 $\mu\text{F}$ , Chip Capacitor	Z2	Transmission Line*
C3, C4, C10, C11	120 pF, Chip Capacitor	Z3	Transmission Line*
C5, C9	0 to 20 pF, Trimmer Capacitor	Z4	Transmission Line*
C6	36 pF, Chip Capacitor	Z5	Transmission Line*
C7	43 pF, Chip Capacitor	Z6	Transmission Line*
C8	30 pF, Chip Capacitor	Z7, Z8	Transmission Line+
L1, L2	7 Turns, 24 AWG 0.116" ID	Z9	Transmission Line*
N1, N2	Type N Flange Mount	Z10	Transmission Line*
R1	1 k $\Omega$ , 1/4 W, Carbon	Board	Glass Teflon® 0.060"
R2	470 k $\Omega$ , 1/4 W, Carbon		+ Part of Capacitor Mount Socket
			*See Photomaster

**Figure 1. 512 MHz Narrowband Test Circuit Electrical Schematic**



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Figure 2. Photomaster for 512 MHz Narrowband Test Fixture

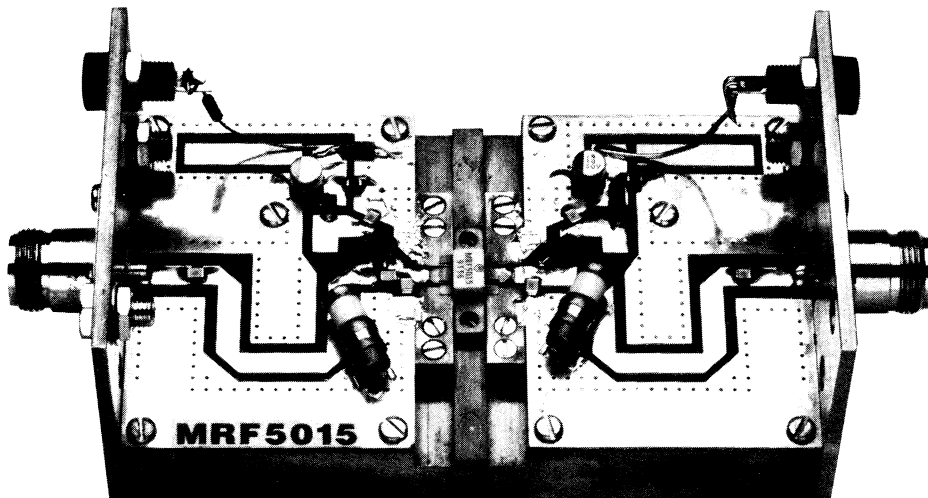


Figure 3. Test Fixture

## TYPICAL CHARACTERISTICS

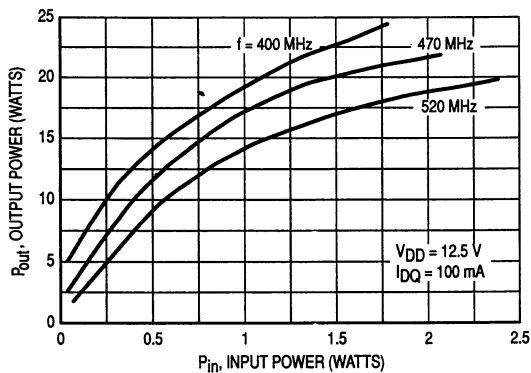


Figure 4. Output Power versus Input Power

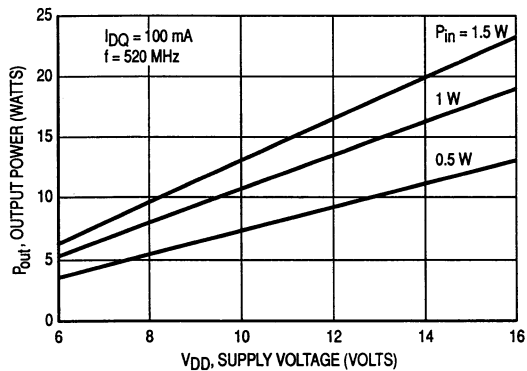


Figure 5. Output Power versus Supply Voltage

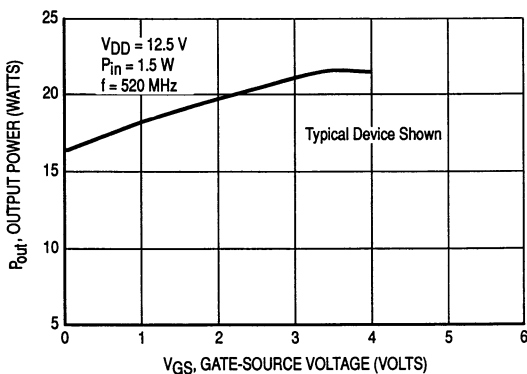


Figure 6. Output Power versus Gate Voltage

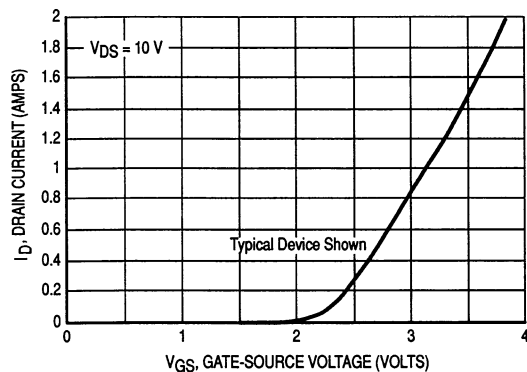


Figure 7. Drain Current versus Gate Voltage

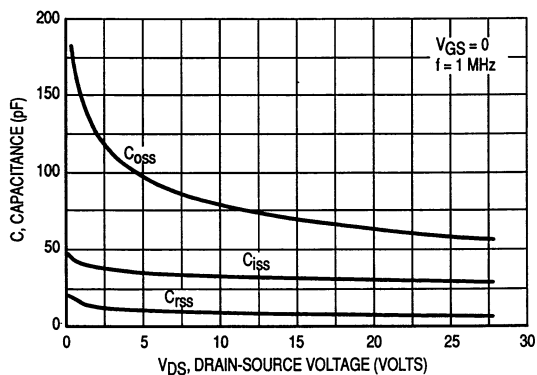


Figure 8. Capacitance versus Voltage

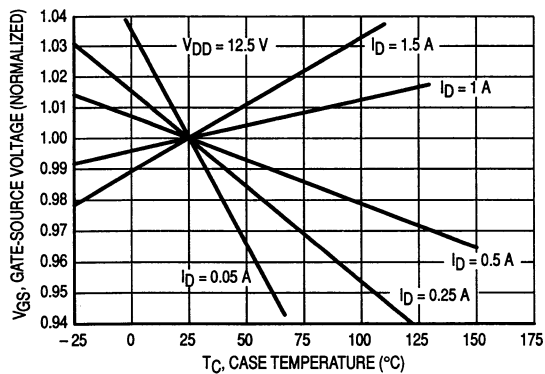


Figure 9. Gate-Source Voltage versus Case Temperature

### TYPICAL CHARACTERISTICS

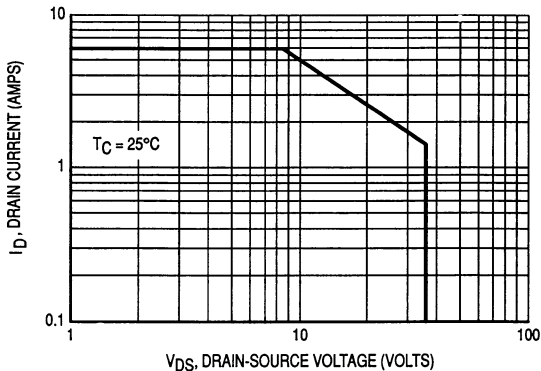
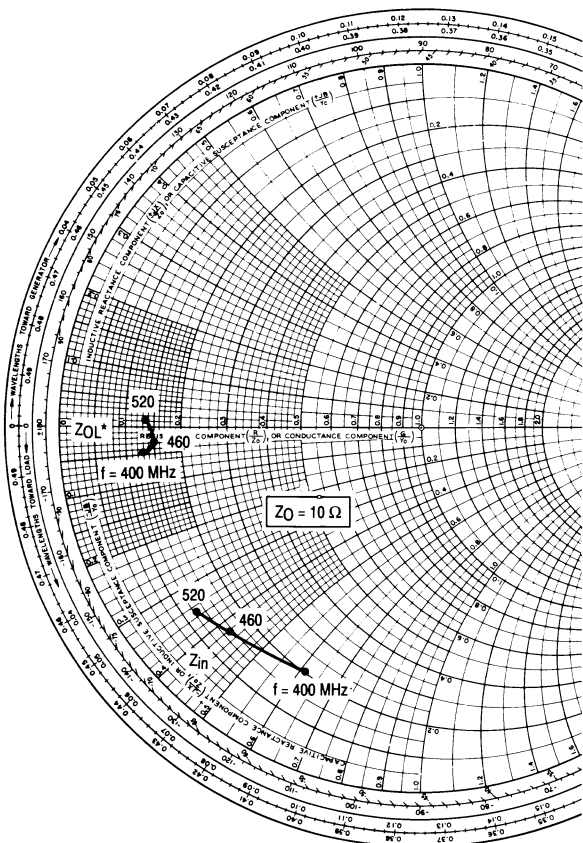


Figure 10. DC Safe Operating Area



$V_{DD} = 12.5 \text{ V}$ ,  $I_{DQ} = 100 \text{ mA}$ ,  $P_{out} = 15 \text{ W}$

f (MHz)	$Z_{in}$ ( $\Omega$ )	$Z_{OL}^*$ ( $\Omega$ )
400	$2.0 - j6.1$	$1.3 - j0.4$
420	$1.8 - j5.3$	$1.4 - j0.4$
440	$1.6 - j4.7$	$1.5 - j0.4$
460	$1.5 - j4.2$	$1.5 - j0.3$
480	$1.4 - j3.8$	$1.5 - j0.2$
500	$1.3 - j3.6$	$1.4 - j0.1$
520	$1.2 - j3.5$	$1.3 + j0.1$

$Z_{in}$  = Conjugate of source impedance with parallel  $160 \Omega$  resistor and  $36 \text{ pF}$  capacitor in series with gate.

$Z_{OL}^*$  = Conjugate of the load impedance at given output power, voltage and frequency that produces maximum gain.

Figure 11. Series Equivalent Input and Output Impedance

**Table 1. Common Source Scattering Parameters ( $V_{DS} = 12.5\text{ V}$ )**

**$I_D = 50\text{ mA}$**

f	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	MHz	S <sub>11</sub>	∠φ	S <sub>21</sub>	∠φ	S <sub>12</sub>	∠φ	S <sub>22</sub>
50	0.63	-123	8	100	0.063	11	0.79	-149
100	0.62	-142	4	82	0.063	-6	0.82	-162
200	0.70	-152	1.8	61	0.056	-23	0.86	-169
300	0.78	-157	1.1	47	0.046	-35	0.90	-171
400	0.84	-162	0.70	36	0.037	-42	0.93	-174
500	0.88	-165	0.49	28	0.029	-46	0.94	-175
700	0.93	-171	0.28	17	0.016	-45	0.97	-179
850	0.95	-175	0.20	13	0.010	-31	0.97	179
1000	0.96	-178	0.15	10	0.007	11	0.98	178

**$I_D = 100\text{ mA}$**

f	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	MHz	S <sub>11</sub>	∠φ	S <sub>21</sub>	∠φ	S <sub>12</sub>	∠φ	S <sub>22</sub>
50	0.67	-136	9.1	99	0.047	10	0.82	-158
100	0.66	-153	4.6	84	0.048	-3	0.85	-168
200	0.71	-160	2.2	66	0.043	-17	0.87	-172
300	0.77	-163	1.3	54	0.037	-26	0.90	-174
400	0.82	-165	0.89	44	0.031	-32	0.92	-175
500	0.86	-168	0.64	36	0.025	-35	0.94	-177
700	0.91	-173	0.37	25	0.015	-30	0.96	-179
850	0.93	-176	0.27	20	0.010	-11	0.97	179
1000	0.95	-179	0.20	16	0.009	25	0.98	177

**$I_D = 500\text{ mA}$**

f	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	MHz	S <sub>11</sub>	∠φ	S <sub>21</sub>	∠φ	S <sub>12</sub>	∠φ	S <sub>22</sub>
50	0.81	-150	11.1	98	0.027	11	0.85	-168
100	0.81	-164	5.6	86	0.027	2	0.87	-174
200	0.82	-170	2.7	73	0.025	-5	0.88	-176
300	0.84	-173	1.7	63	0.023	-9	0.89	-177
400	0.86	-174	1.2	55	0.020	-9	0.91	-178
500	0.88	-175	0.92	47	0.018	-7	0.92	-179
700	0.91	-178	0.57	35	0.013	7	0.94	180
850	0.93	180	0.43	29	0.013	26	0.95	178
1000	0.94	178	0.33	23	0.014	44	0.96	177

**$I_D = 2.5\text{ A}$**

f	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	MHz	S <sub>11</sub>	∠φ	S <sub>21</sub>	∠φ	S <sub>12</sub>	∠φ	S <sub>22</sub>
50	0.86	-144	10.1	101	0.022	15	0.85	-171
100	0.85	-161	5.2	88	0.022	5	0.87	-175
200	0.86	-170	2.5	74	0.021	-1	0.89	-177
300	0.87	-173	1.6	64	0.019	-4	0.90	-178
400	0.89	-175	1.1	55	0.017	-2	0.91	-178
500	0.91	-176	0.84	48	0.015	2	0.93	-179
700	0.93	-179	0.52	37	0.013	22	0.95	179
850	0.94	179	0.39	30	0.014	39	0.96	178
1000	0.95	177	0.30	26	0.016	52	0.96	176

2



## DESIGN CONSIDERATIONS

The MRF5015 is a common-source, RF power, N-Channel enhancement mode, Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET). Motorola RF MOSFETs feature a vertical structure with a planar design. Motorola Application Note AN211A, "FETs in Theory and Practice," is suggested reading for those not familiar with the construction and characteristics of FETs.

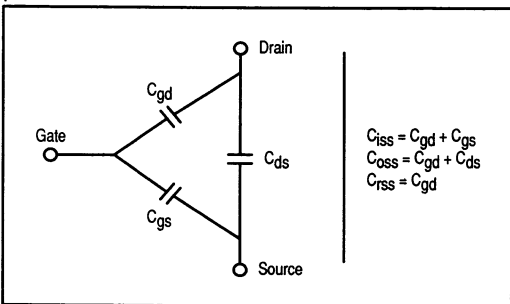
This device was designed primarily for 12.5 volt VHF and UHF power amplifier applications. The major advantages of RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

## MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate-to-drain ( $C_{gd}$ ), and gate-to-source ( $C_{gs}$ ). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain-to-source ( $C_{ds}$ ). These capacitances are characterized as input ( $C_{iss}$ ), output ( $C_{oss}$ ) and reverse transfer ( $C_{rss}$ ) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The  $C_{iss}$  can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



## DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full-on condition. This on-resistance,  $R_{ds(on)}$ , occurs in the linear region of the output characteristic and is specified at a specific gate-source voltage and drain current. The drain-source voltage under these conditions is termed  $V_{ds(on)}$ . For MOSFETs,  $V_{ds(on)}$  has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

## GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high, on the order of  $10^9 \Omega$ , resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate-to-source threshold voltage,  $V_{GS(th)}$ .

**Gate Voltage Rating** – Never exceed the gate voltage rating. Exceeding the rated  $V_{GS}$  can result in permanent damage to the oxide layer in the gate region.

**Gate Termination** – The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating must be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

**Gate Protection** – These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended with appropriate RF decoupling networks.

Using a resistor to keep the gate-to-source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

## DC BIAS

Since the MRF5015 is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. See Figure 7 for a typical plot of drain current versus gate voltage. RF power FETs operate optimally with a quiescent drain current ( $I_{DQ}$ ), whose value is application dependent. The MRF5015 was characterized at  $I_{DQ} = 100$  mA, which is the suggested value of bias current for typical applications. For special applications such as linear amplification,  $I_{DQ}$  may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws essentially no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

## GAIN CONTROL

Power output of the MRF5015 may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. Figure 6 is an example of output power variation with gate-source bias voltage with  $P_{in}$  held constant. This characteristic is very dependent on frequency and load line.

## AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for the MRF5015. For examples see Motorola Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Both small-signal S-parameters and large-signal impedances are provided. While the S-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF power MOSFETs.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of MRF5015

yield a device quite capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. Different stabilizing techniques may be required depending on the desired gain and bandwidth of the application. The RF test fixture implements a parallel resistor and capacitor in series with the gate to improve stability and input impedance Q.

Two port stability analysis with the MRF5015 S-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, "RF Small-Signal Design Using Two-Port Parameters," for a discussion of two port network theory and stability.

*Advance Information*  
**The RF MOSFET Line**  
**RF Power Field Effect Transistor**  
**N-Channel Enhancement-Mode**

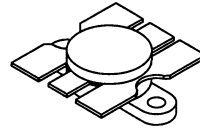
Designed for broadband commercial and industrial applications at frequencies to 520 MHz. The high gain and broadband performance of this device makes it ideal for large-signal, common source amplifier applications in 12.5 volt mobile, and base station FM equipment.

- Guaranteed Performance at 512 MHz, 12.5 Volt  
 Output Power — 35 Watts  
 Power Gain — 6.5 dB Min  
 Efficiency — 50% Min
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- S-Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- All Gold Metal for Ultra Reliability
- Capable of Handling 20:1 Load VSWR, @ 15.5 Volt, 512 MHz, 2 dB Overdrive

**MRF5035**

Motorola Preferred Device

**35 W, 12.5 VOLTS, 512 MHz  
 N-CHANNEL BROADBAND  
 RF POWER FET**



**CASE 316, STYLE 3**

**2**

**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	36	Vdc
Drain-Gate Voltage (RGS = 1 M $\Omega$ )	$V_{DGR}$	36	Vdc
Gate-Source Voltage	$V_{GS}$	$\pm 20$	Vdc
Drain Current — Continuous	$I_D$	15	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	97 0.56	Watts W/ $^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	- 65 to +150	$^\circ\text{C}$
Operating Junction Temperature	$T_J$	200	$^\circ\text{C}$

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.8	$^\circ\text{C}/\text{W}$

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

Drain-Source Breakdown Voltage ( $V_{GS} = 0, I_D = 20 \text{ mAdc}$ )	$V_{(BR)DSS}$	36	—	—	Vdc
Zero Gate Voltage Drain Current ( $V_{DS} = 15 \text{ Vdc}, V_{GS} = 0$ )	$I_{DSS}$	—	—	5	mAdc
Gate-Source Leakage Current ( $V_{GS} = 20 \text{ Vdc}, V_{DS} = 0$ )	$I_{GSS}$	—	—	5	$\mu\text{Adc}$

(continued)

**NOTE — CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

This document contains information on a new product. Specifications and information herein are subject to change without notice.  
 Preferred devices are Motorola recommended choices for future use and best overall value.

**ELECTRICAL CHARACTERISTICS — continued** ( $T_C = 25^\circ\text{C}$  unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>ON CHARACTERISTICS</b>					
Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 25\text{ mAdc}$ )	$V_{GS(th)}$	1.25	2.3	3.5	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 3\text{ Adc}$ )	$V_{DS(on)}$	—	—	0.422	Vdc
Forward Transconductance ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 3\text{ Adc}$ )	gfs	3.2	—	—	S

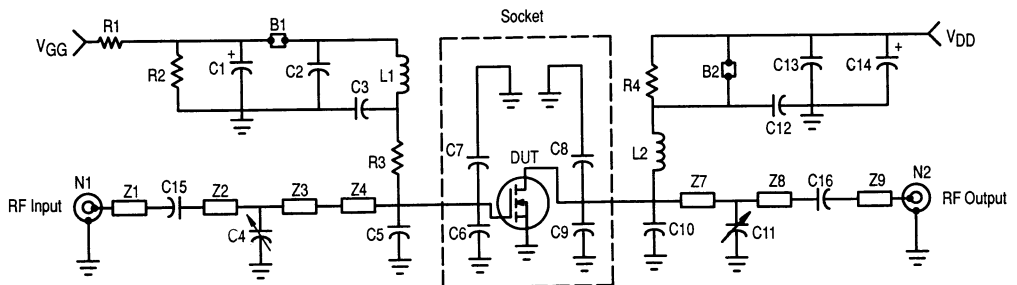
**DYNAMIC CHARACTERISTICS**

Input Capacitance ( $V_{DS} = 12.5\text{ Vdc}$ , $V_{GS} = 0$ , $f = 1\text{ MHz}$ )	$C_{iss}$	—	88	—	pF
Output Capacitance ( $V_{DS} = 12.5\text{ Vdc}$ , $V_{GS} = 0$ , $f = 1\text{ MHz}$ )	$C_{oss}$	—	197	—	pF
Reverse Transfer Capacitance ( $V_{DS} = 12.5\text{ Vdc}$ , $V_{GS} = 0$ , $f = 1\text{ MHz}$ )	$C_{rss}$	18	24	29	pF

**FUNCTIONAL TESTS** (In Motorola Test Fixture)

Common-Source Amplifier Power Gain ( $V_{DD} = 12.5\text{ Vdc}$ , $P_{out} = 35\text{ W}$ , $I_{DQ} = 400\text{ mA}$ )	$f = 512\text{ MHz}$ $f = 175\text{ MHz}$	$G_{ps}$	6.5 —	7.5 12	— —	dB
Drain Efficiency ( $V_{DD} = 12.5\text{ Vdc}$ , $P_{out} = 35\text{ W}$ , $I_{DQ} = 400\text{ mA}$ )	$f = 512\text{ MHz}$ $f = 175\text{ MHz}$	$\eta$	50 —	55 55	— —	%
Load Mismatch ( $V_{DD} = 15.5\text{ Vdc}$ , 2 dB Overdrive, $f = 512\text{ MHz}$ , Load VSWR = 20:1, All Phase Angles at Frequency of Test)		$\psi$	No Degradation in Output Power			

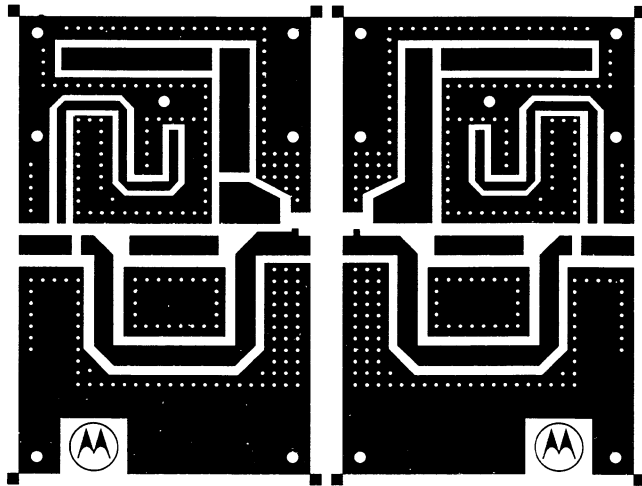
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**Components List**

B1, B2	Short Ferrite Bead, Fair Rite Products	N1, N2	Type N Flange Mount
C1, C14	10 $\mu\text{F}$ , 50 V, Electrolytic	R1	1 k $\Omega$ , 1/4 W, Carbon
C2	1500 pF, Chip Capacitor	R2	1 M $\Omega$ , 1/4 W, Carbon
C3	140 pF, Chip Capacitor	R3	100 $\Omega$ , 1/4 W, Carbon
C4, C11	0-10pF, Trimmer Capacitor	R4	110 $\Omega$ , 1/4 W, Carbon
C5	30 pF, Chip Capacitor	Z1, Z9	Transmission Line*
C6, C7	43 pF, Chip Capacitor	Z2	Transmission Line*
C8, C9	36 pF, Chip Capacitor	Z3	Transmission Line*
C10	3.6 pF, Chip Capacitor	Z4	Transmission Line*
C12, C15, C16	120 pF, Chip Capacitor	Z7	Transmission Line*
C13	0.1 $\mu\text{F}$ , Chip Capacitor	Z8	Transmission Line*
L1	5 Turns, 18 AWG, 0.116" ID	Board	Glass Teflon® 0.060"
L2	8 Turns, 20 AWG, 0.125" ID		*See Photomaster for Dimensions

**Figure 1. 512 MHz Narrowband Test Circuit Electrical Schematic**



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Figure 2. Photomaster for 512 MHz Narrowband Test Fixture

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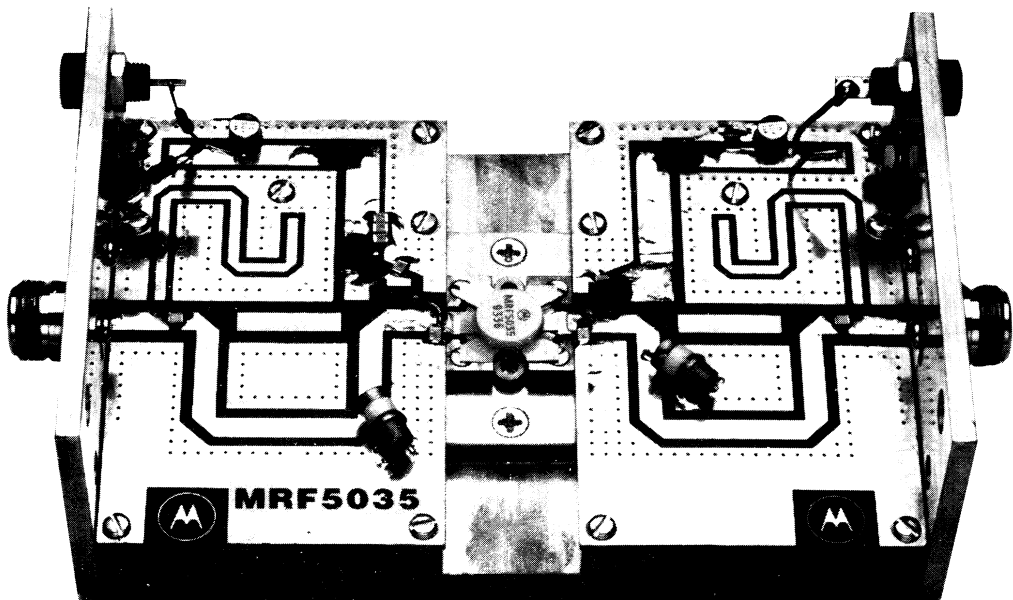


Figure 3. Test Fixture

## TYPICAL CHARACTERISTICS

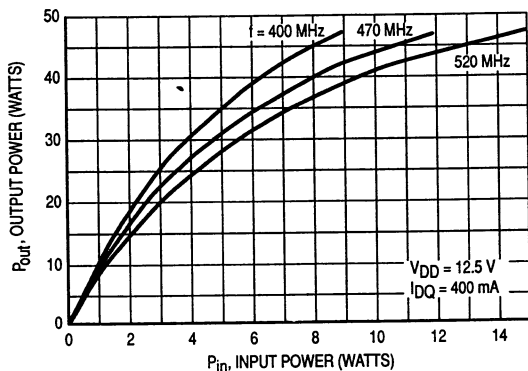


Figure 4. Output Power versus Input Power

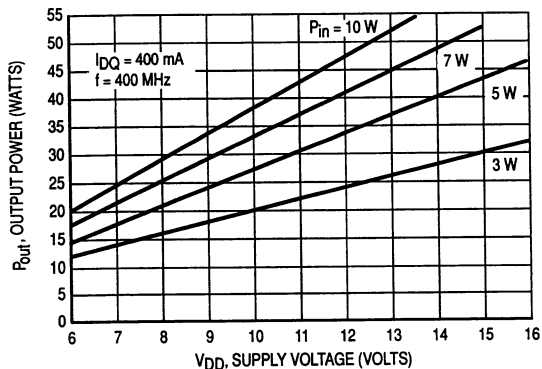


Figure 5. Output Power versus Supply Voltage

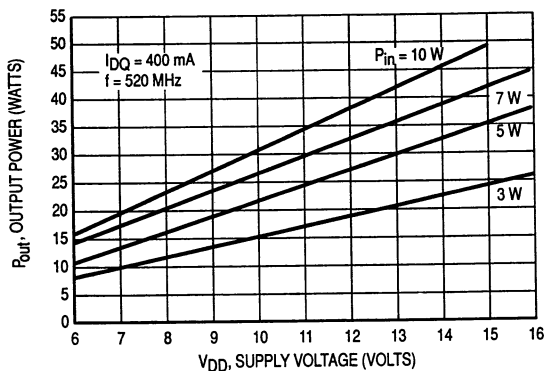


Figure 6. Output Power versus Supply Voltage

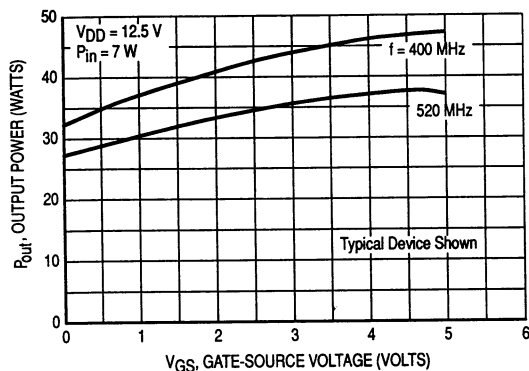


Figure 7. Output Power versus Gate Voltage

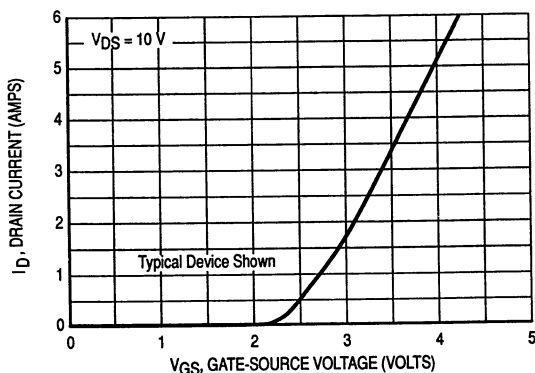


Figure 8. Drain Current versus Gate Voltage

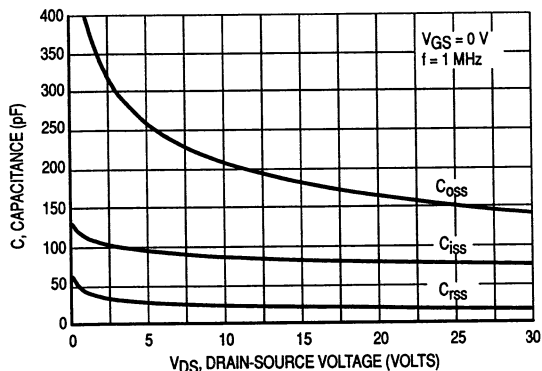


Figure 9. Capacitance versus Voltage

## TYPICAL CHARACTERISTICS

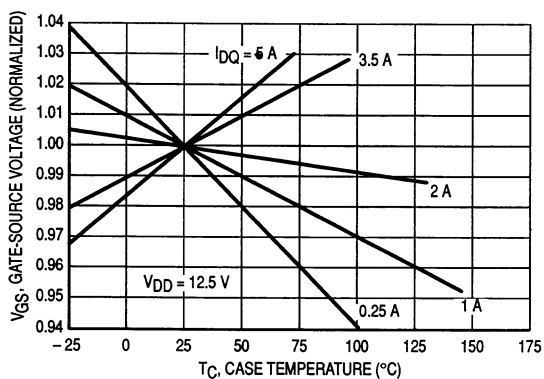


Figure 10. Gate-Source Voltage versus Case Temperature

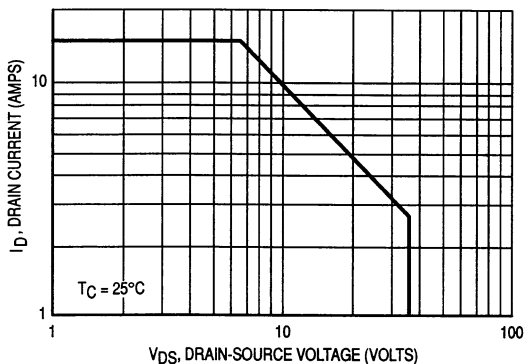


Figure 11. DC Safe Operating Area

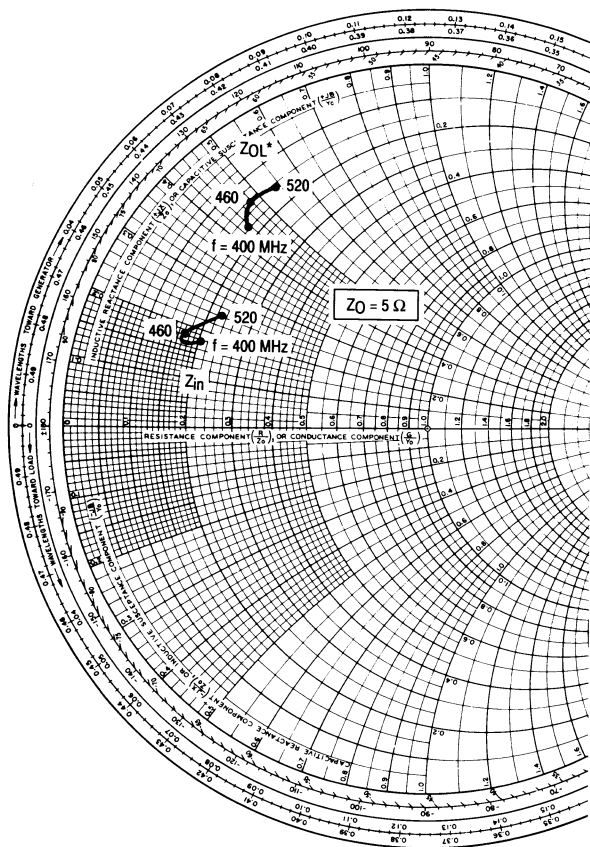


Figure 12. Series Equivalent Input and Output Impedance

$V_{DD} = 12.5 \text{ V}$ ,  $I_{DQ} = 400 \text{ mA}$ ,  $P_{in} = 7.8 \text{ W}$ ,  
Tune for Maximum Output Power

f (MHz)	$Z_{in}$ ( $\Omega$ )	$Z_{OL}^*$ ( $\Omega$ )
400	$1.0 + j0.89$	$0.87 + j2.1$
420	$0.90 + j0.83$	$0.79 + j2.2$
440	$0.83 + j0.81$	$0.73 + j2.3$
460	$0.82 + j0.83$	$0.71 + j2.4$
480	$0.87 + j0.90$	$0.71 + j2.5$
500	$0.97 + j1.0$	$0.74 + j2.6$
520	$1.1 + j1.2$	$0.80 + j2.7$

$Z_{in}$  = Conjugate of source impedance.

$Z_{OL}^*$  = Conjugate of the load impedance at given input power, voltage and frequency that produces maximum output power.

Table 1. Common Source Scattering Parameters ( $V_{DS} = 12.5\text{ V}$ )

$I_D = 100\text{ mA}$

f	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	MHz	S <sub>11</sub>	∠φ	S <sub>21</sub>	∠φ	S <sub>12</sub>	∠φ	S <sub>22</sub>
25	0.74	-153	6.9	94	0.039	6	0.87	-169
50	0.74	-164	3.4	82	0.039	-5	0.89	-174
100	0.77	-168	1.6	67	0.036	-16	0.90	-176
150	0.81	-170	1	56	0.032	-25	0.92	-178
200	0.85	-171	0.69	46	0.028	-31	0.93	-179
300	0.90	-174	0.38	32	0.019	-36	0.96	179
400	0.93	-178	0.24	22	0.013	-30	0.97	177
450	0.94	-179	0.20	19	0.010	-22	0.97	175
500	0.95	179	0.17	16	0.008	-8	0.98	174
600	0.96	176	0.12	13	0.008	27	0.98	172

$I_D = 400\text{ mA}$

f	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	MHz	S <sub>11</sub>	∠φ	S <sub>21</sub>	∠φ	S <sub>12</sub>	∠φ	S <sub>22</sub>
25	0.88	-163	7.8	94	0.018	7	0.93	-175
50	0.88	-172	3.9	87	0.018	3	0.93	-178
100	0.88	-176	1.9	77	0.018	-1	0.94	-180
150	0.89	-178	1.3	70	0.017	-2	0.94	179
200	0.89	-179	0.91	63	0.016	-1	0.94	178
300	0.91	180	0.57	51	0.014	3	0.95	177
400	0.92	178	0.39	41	0.012	14	0.96	175
450	0.93	177	0.33	37	0.012	22	0.96	174
500	0.94	176	0.29	33	0.012	29	0.97	173
600	0.95	174	0.22	27	0.014	42	0.97	171

$I_D = 1\text{ A}$

f	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	MHz	S <sub>11</sub>	∠φ	S <sub>21</sub>	∠φ	S <sub>12</sub>	∠φ	S <sub>22</sub>
25	0.92	-165	7.8	95	0.013	9	0.94	-177
50	0.91	-173	3.9	88	0.013	6	0.95	-179
100	0.92	-177	1.9	81	0.013	7	0.95	179
150	0.92	-179	1.3	75	0.013	9	0.95	179
200	0.92	180	0.95	69	0.012	12	0.95	178
300	0.93	178	0.61	59	0.012	21	0.96	176
400	0.94	176	0.43	50	0.013	32	0.96	174
450	0.94	175	0.38	46	0.013	37	0.97	174
500	0.94	174	0.33	43	0.014	42	0.97	173
600	0.95	173	0.26	36	0.016	49	0.97	171

$I_D = 5\text{ A}$

f	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	MHz	S <sub>11</sub>	∠φ	S <sub>21</sub>	∠φ	S <sub>12</sub>	∠φ	S <sub>22</sub>
25	0.94	-164	7.2	95	0.010	10	0.95	-178
50	0.94	-172	3.6	89	0.010	9	0.95	-180
100	0.94	-177	1.8	81	0.010	11	0.96	179
150	0.94	-179	1.2	76	0.011	16	0.96	178
200	0.94	179	0.89	70	0.011	21	0.96	177
300	0.95	177	0.57	61	0.011	31	0.96	176
400	0.95	176	0.42	52	0.013	41	0.97	174
450	0.95	175	0.36	48	0.013	45	0.97	173
500	0.96	174	0.32	45	0.014	48	0.97	172
600	0.96	172	0.26	39	0.017	54	0.97	171



## DESIGN CONSIDERATIONS

The MRF5035 is a common-source, RF power, N-Channel enhancement mode, Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET). Motorola RF MOSFETs feature a vertical structure with a planar design. Motorola Application Note AN211A, "FETs in Theory and Practice," is suggested reading for those not familiar with the construction and characteristics of FETs.

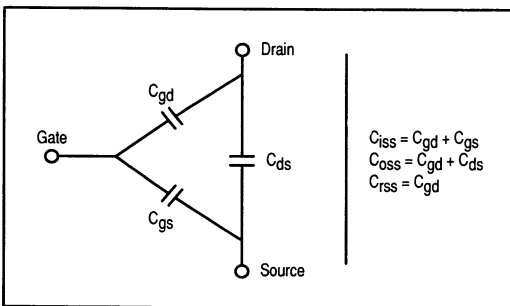
This device was designed primarily for 12.5 volt VHF and UHF Land Mobile FM power amplifier applications. The major advantages of RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

## MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate-to-drain ( $C_{gd}$ ), and gate-to-source ( $C_{gs}$ ). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain-to-source ( $C_{ds}$ ). These capacitances are characterized as input ( $C_{iss}$ ), output ( $C_{oss}$ ) and reverse transfer ( $C_{rss}$ ) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The  $C_{iss}$  can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



## DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full-on condition. This on-resistance,  $R_{ds(on)}$ , occurs in the linear region of the output characteristic and is specified

at a specific gate-source voltage and drain current. The drain-source voltage under these conditions is termed  $V_{ds(on)}$ . For MOSFETs,  $V_{ds(on)}$  has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

## GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high, on the order of  $10^9 \Omega$ , resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate-to-source threshold voltage,  $V_{GS(th)}$ .

**Gate Voltage Rating** – Never exceed the gate voltage rating. Exceeding the rated  $V_{GS}$  can result in permanent damage to the oxide layer in the gate region.

**Gate Termination** – The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating must be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

**Gate Protection** – These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended with appropriate RF decoupling networks.

Using a resistor to keep the gate-to-source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

## DC BIAS

Since the MRF5035 is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. See Figure 8 for a typical plot of drain current versus gate voltage. RF power FETs operate optimally with a quiescent drain current ( $I_{DQ}$ ), whose value is application dependent. The MRF5035 was characterized at  $I_{DQ} = 400 \text{ mA}$ , which is the suggested value of bias current for typical applications. For special applications such as linear amplification,  $I_{DQ}$  may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws essentially no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

## GAIN CONTROL

Power output of the MRF5035 may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. Figure 7 is an example of output power variation with gate-source bias voltage with  $P_{in}$  held constant. This characteristic is very dependent on frequency and load line.

## AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for the MRF5035. For examples see Motorola Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Both small-signal S-parameters and large-signal impedances are provided. While the S-parameters will not produce an exact design solution for high power operation, they do

yield a good first approximation. This is an additional advantage of RF power MOSFETs.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the high gain of the MRF5035 yield a device quite capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. Different stabilizing techniques may be required depending on the desired gain and bandwidth of the application. The RF test fixture implements a resistor in shunt with the gate to improve stability. Two port stability analysis with the MRF5035 S-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, "RF Small-Signal Design Using Two-Port Parameters," for a discussion of two port network theory and stability.