MTM1224, MTM1225
MTP1224, MTP1225

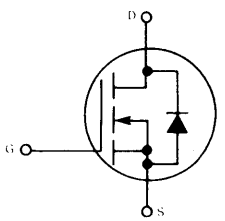
Designers Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds – Switching Times Specified at 100°C
- Designers Data – I_{DSS}, $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged – SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)}$ 4.0 Volts (max)

TMOS™

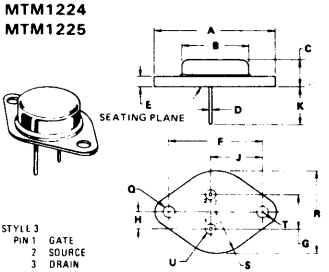


12 AMPERE

N-CHANNEL TMOS POWER FET

60 and 100 VOLTS

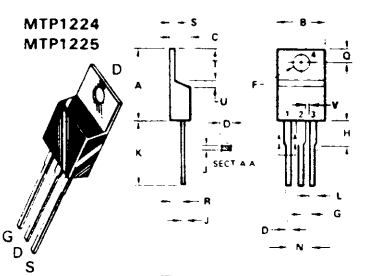
MTM1224
MTM1225



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.58	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120

CASE 1-04
TO-3 TYPE

MTP1224
MTP1225



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14		0.045	

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM1224 MTP1224	MTM1225 MTP1225	Unit
Drain – Source Voltage	V_{DSS}	60	100	Vdc
Drain – Gate Voltage	V_{DGO}	60	100	Vdc
Gate – Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 12 30		Adc
Gate Current – Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

TMOS is a trademark of Motorola Inc.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 mA)	MTM1224/MTP1224 MTM1225/MTP1225	$V_{(BR)DSS}$	 60 100	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 BV_{DSS}, V_{GS} = 0) T_C = 100°C		I_{DSS}	 — —	 0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	1.5	4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 6.0 Adc) (I_D = 12 Adc) (I_D = 6.0 Adc, T_C = 100°C)		$V_{DS(on)}$	 — — —	 1.5 3.0 2.5	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 6.0 Adc)		$r_{DS(on)}$	—	0.25	Ohms
Forward Transconductance (V_{DS} = 10 V, I_D = 6.0 A)		g_{fs}	3.0	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{iss}	—	1200	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{oss}	—	500	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{rss}	—	120	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time (V_{DS} = 25 V, I_D = 2.5 A, R_{gen} = 50 ohms)		$t_{d(on)}$	—	50	ns
Rise Time (V_{DS} = 25 V, I_D = 2.5 A, R_{gen} 50 ohms)		t_r	—	100	ns
Turn-Off Delay Time (V_{DS} = 25 V, I_D = 2.5 A, R_{gen} = 50 ohms)		$t_{d(off)}$	—	200	ns
Fall Time (V_{DS} = 25 V, I_D = 2.5 A, R_{gen} = 50 ohms)		t_f	—	100	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 12 A	V_{SD}	1.3	Vdc
Forward Turn-On Time	V_{GS} = 0	t_{on}	250	ns
Reverse Recovery Time	See Figures 17 and 18	t_{rr}	325	ns

*Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

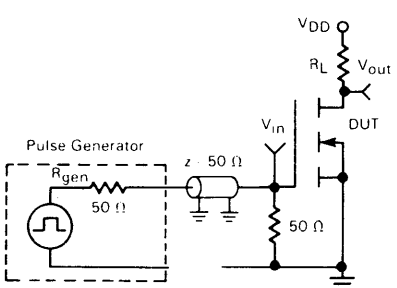
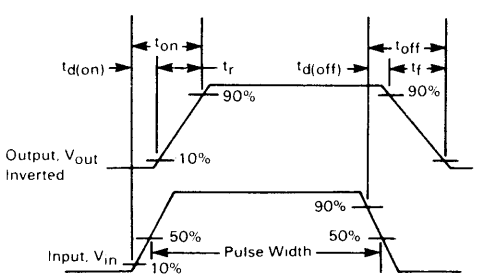


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

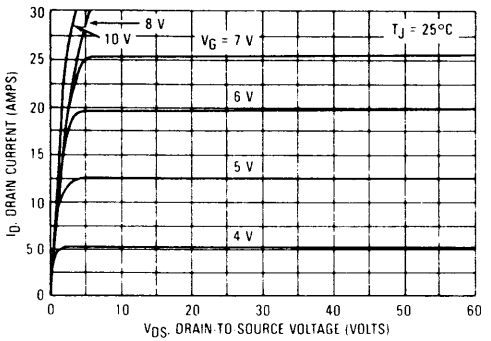


FIGURE 4 — ON-REGION CHARACTERISITCS

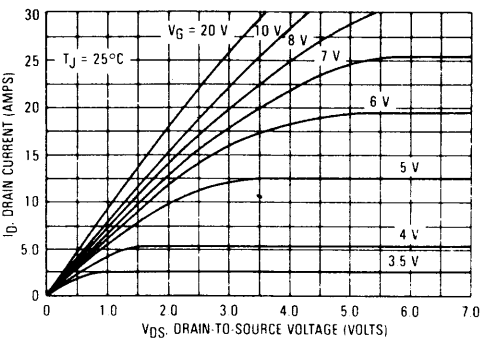


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

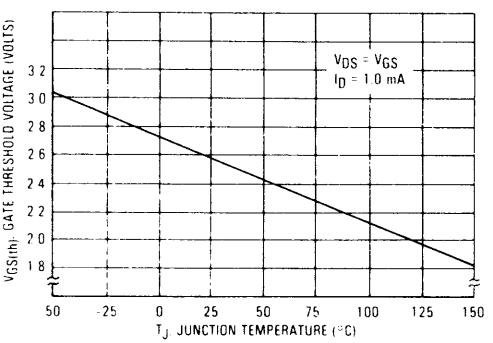


FIGURE 6 — TRANSFER CHARACTERISTICS

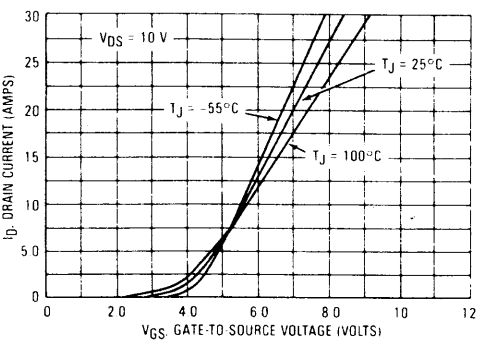


FIGURE 7 — ON-VOLTAGE versus TEMPERATURE

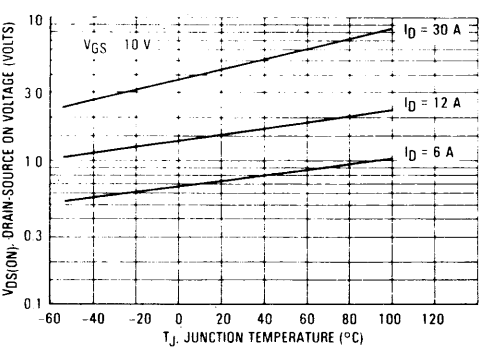
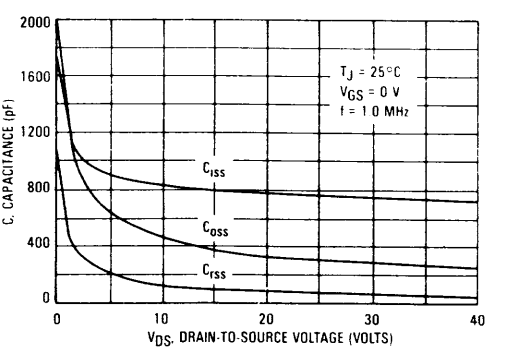


FIGURE 8 — CAPACITANCE VARIATION



3

TYPICAL CHARACTERISTICS

FIGURE 9 — ON-RESISTANCE versus DRAIN CURRENT

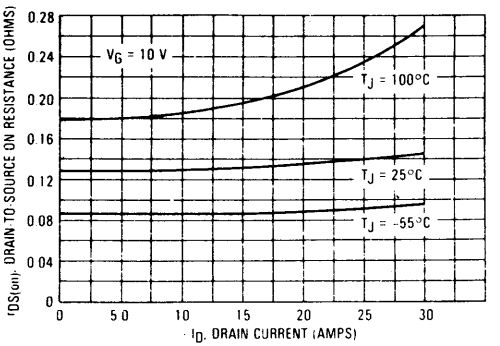
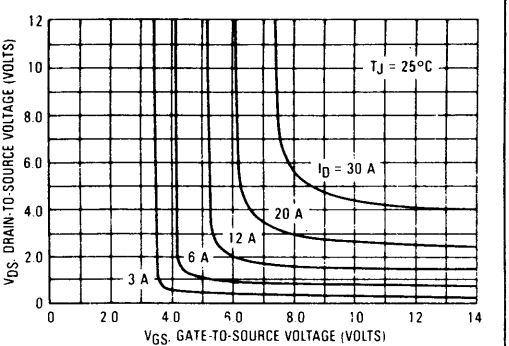


FIGURE 10 — ON-VOLTAGE VARIATION



THERMAL RESPONSE

FIGURE 11 — MTM1224/MTM1225

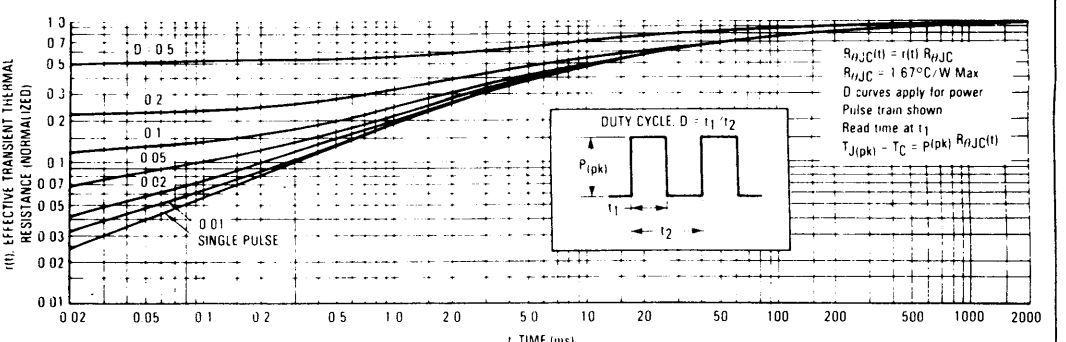
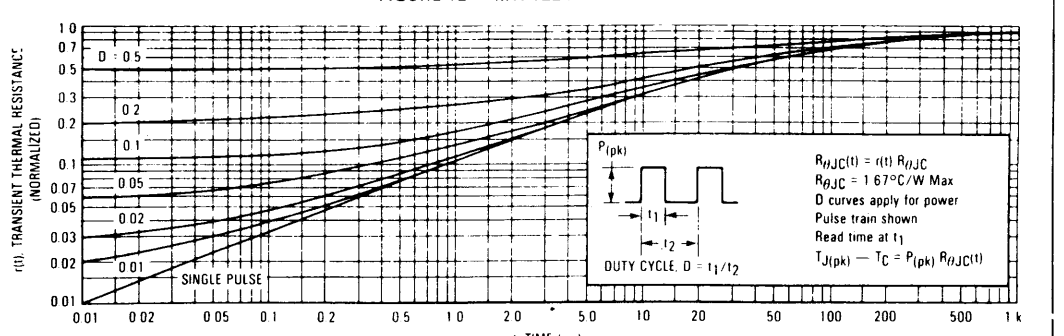


FIGURE 12 — MTP1224/MTP1225



SAFE OPERATING AREA INFORMATION

FIGURE 13 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

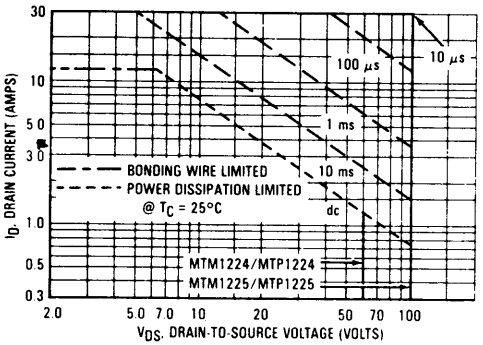
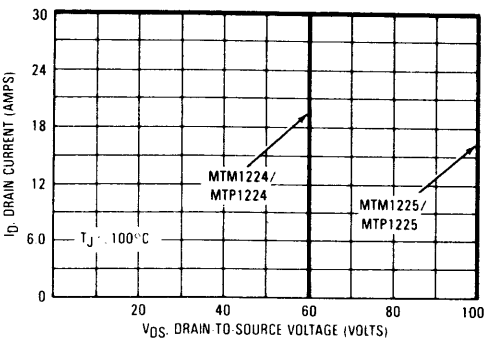


FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 13 is based on $T_C = 25°C$; $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 13 may be calculated for any case temperature with the aid of the following equation

$$I_D(T_C) = I_D(25°C)\left[1 - \frac{T_C - 25°C}{P_D R_{\theta JC}}\right]$$

where

$I_D(T_C)$ = the maximum allowable current at a case temperature, T_C

$I_D(25°C)$ = the maximum allowable current at a given voltage from Figure 13

P_D = the rated power dissipation at $T_C = 25°C$

$R_{\theta JC}$ = the rated steady state thermal resistance

For various pulse widths and duty cycles, substitute $R_{\theta JC}(t)$ determined from Figures 11 and 12 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

3

TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 500 mA. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 15. Reversal of the drain voltage will cause current flow in the reverse direction. This diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 15 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

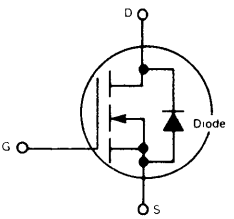


FIGURE 16 — DIODE TURN-ON TEST CIRCUIT

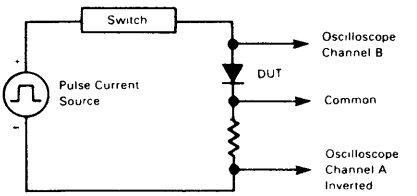


FIGURE 17 — DIODE TURN-ON WAVEFORMS

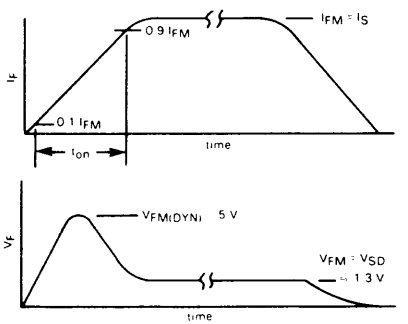


FIGURE 18 — REVERSE RECOVERY CHARACTERISTIC

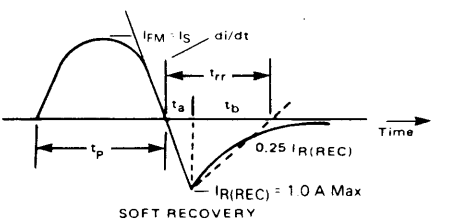
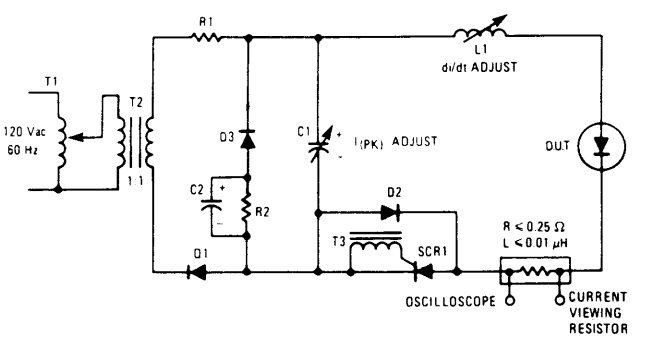


FIGURE 19 — JEDEC REVERSE RECOVERY CIRCUIT



R1 = 50 Ohms
R2 = 250 Ohms
D1 = 1N4723
D2 = 1N4001
D3 = 1N4933
SCR1 = MCR729-10
C1 = 0.5 to 50 μF
C2 ≈ 4000 μF
L1 = 1.0 - 27 μH
T1 = Variac Adjusts $I_{(PK)}$ and di/dt
T2 = 1:1
T3 = 1:1 (to trigger circuit)