MOTOROLA

MTM5N18, MTP5N18
MTM5N20, MTP5N20
MTM7N12, MTP7N12
MTM7N15, MTP7N15

Designer's Data Sheet

5 and 7 AMPERE
N-CHANNEL TMOS POWER FET
$r_{DS(on)}$ = 0.7 OHM
120 and 150 VOLTS

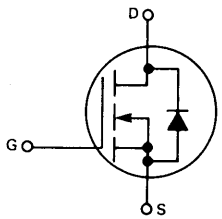
$r_{DS(on)}$ = 1.0 OHM
180 and 200 VOLTS

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

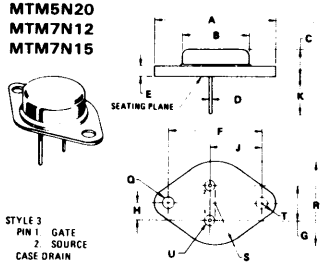
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads

TMOS™



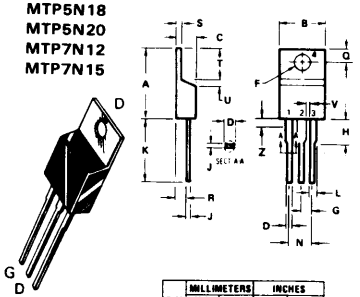
MTM5N18
MTM5N20
MTM7N12
MTM7N15



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	38.37	–	1.560
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.58	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120

CASE 1-05
TO-204AA

MTP5N18
MTP5N20
MTP7N12
MTP7N15



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM or MTP 7N12	7N15	5N18	5N20	Unit
Drain — Source Voltage	V_{DSS}	120	150	180	200	Vdc
Drain — Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	120	150	180	200	Vdc
Gate — Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous	I_D	7.0		5.0		Adc
Pulsed	I_{DM}	18		15		
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C	P_D	75				Watts
Derate above 25°C		0.6				W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

DS3555 R1

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM7N12/MTP7N12	$V_{(BR)DSS}$	120	—	Vdc
	MTM7N15/MTP7N15		150	—	
	MTM5N18/MTP5N18		180	—	
	MTM5N20/MTP5N20		200	—	
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
(T_J = 100°C)			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
(T_J = 100°C)			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3.5 Adc)	MTM7N12/MTM7N15 MTP7N12/MTP7N15	$r_{DS(on)}$	—	0.7	Ohms
(V_{GS} = 10 Vdc, I_D = 2.5 Adc)	MTM5N18/MTM5N20 MTP5N18/MTP5N20		—	1.0	
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 7.0 Adc)	MTM7N12/MTM7N15 MTP7N12/MTP7N15	$V_{DS(on)}$	—	5.9	Vdc
(I_D = 3.5 Adc, T_J = 100°C)	MTM5N18, MTM5N20 MTP5N18/MTP5N20		—	5.0	
(I_D = 5.0 Adc)	MTM7N12/MTM7N15 MTP7N12/MTP7N15		—	6.0	
(I_D = 2.5 Adc, T_J = 100°C)	MTM5N18/MTM5N20 MTP5N18/MTP5N20		—	5.0	
Forward Transconductance (V_{DS} = 15 V, I_D = 3.5 A)	MTM7N12/MTM7N15 MTP7N12/MTP7N15	g_{fs}	1.5	—	mhos
(V_{DS} = 15 V, I_D = 2.5 A)	MTM5N18/MTM5N20 MTP5N18/MTP5N20		1.5	—	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	400	pF
Output Capacitance		C_{oss}	—	175	pF
Reverse Transfer Capacitance		C_{rss}	—	30	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms, See Figures 1 and 2)	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	150	ns
Turn-Off Delay Time		$t_{d(off)}$	—	50	ns
Fall Time		t_f	—	50	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0, See Figures 18 and 19)	V_{SD}	2.0	Vdc
Forward Turn-On Time		t_{on}	200	ns
Reverse Recovery Time		t_{rr}	300	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

FIGURE 1 – SWITCHING TEST CIRCUIT

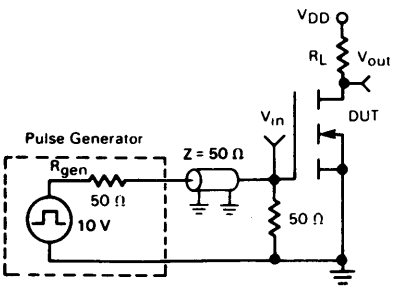
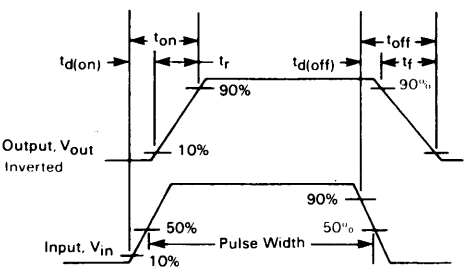


FIGURE 2 – SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

ON-REGION CHARACTERISTICS

FIGURE 3 — MTM5N18, MTM5N20
MTP5N18, MTP5N20

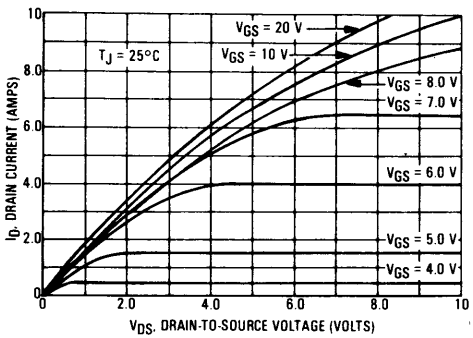
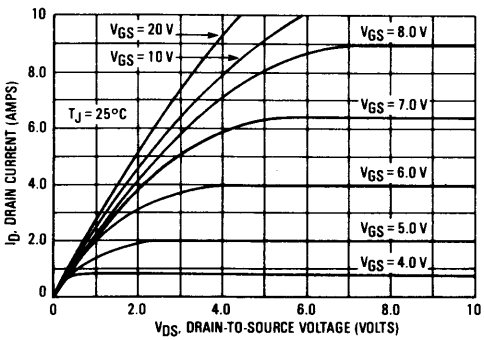


FIGURE 4 — MTM7N12, MTM7N15
MTP7N12, MTP7N15



TRANSFER CHARACTERISTICS

FIGURE 5 — MTM5N18, MTM5N20
MTP5N18, MTP5N20

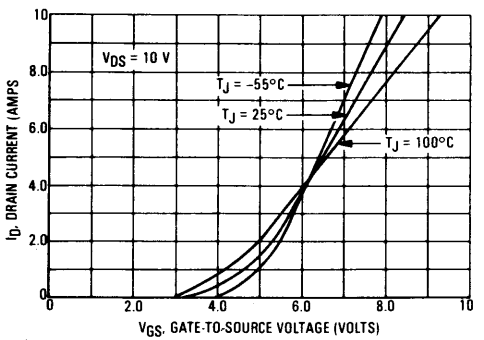
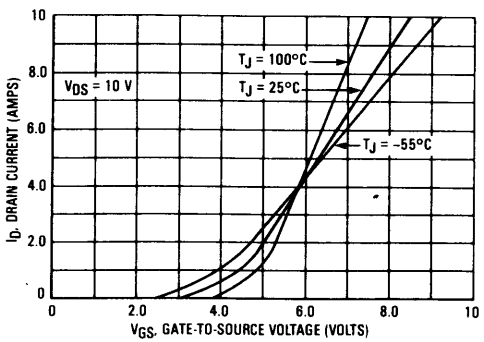


FIGURE 6 — MTM7N12, MTM7N15
MTP7N12, MTP7N15



ON-RESISTANCE versus DRAIN CURRENT

FIGURE 7 — MTM5N18, MTM5N20
MTP5N18, MTP5N20

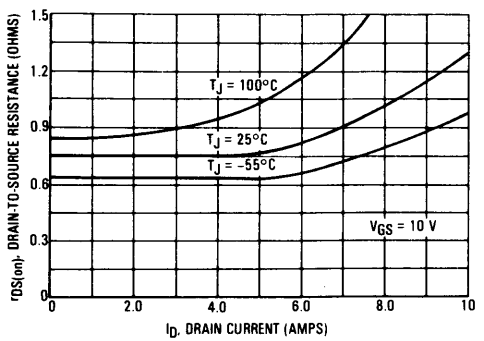
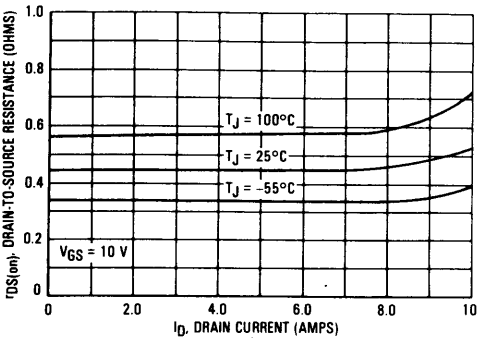


FIGURE 8 — MTM7N12, MTM7N15
MTP7N12, MTP7N15



TYPICAL CHARACTERISTICS

FIGURE 9 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

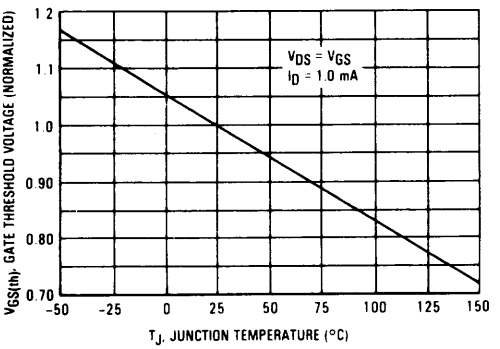
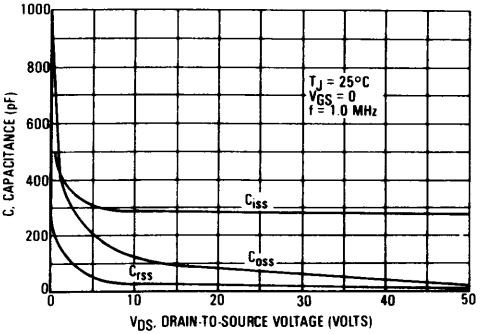


FIGURE 10 — CAPACITANCE VARIATION



THERMAL RESPONSE

FIGURE 11 — MTM7N12, MTM7N15, MTM5N18 AND MTM5N20

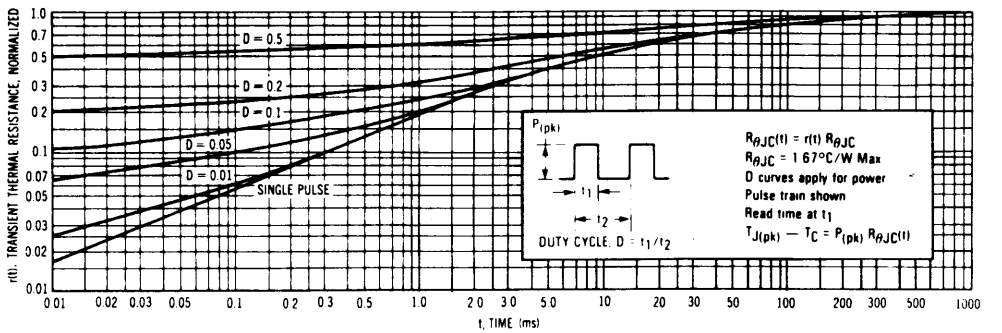
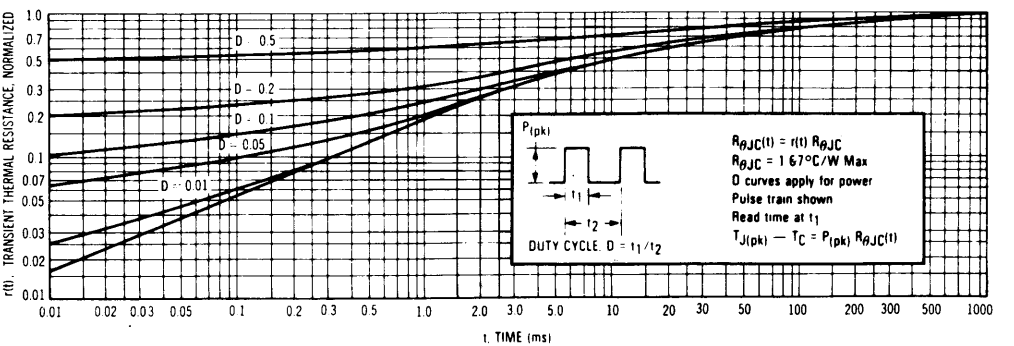


FIGURE 12 — MTP7N12, MTP7N15, MTP5N18 AND MTP5N20



3

SAFE OPERATING AREA INFORMATION

MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

FIGURE 13 — MTM5N18, MTM5N20
MTP5N18, MTP5N20

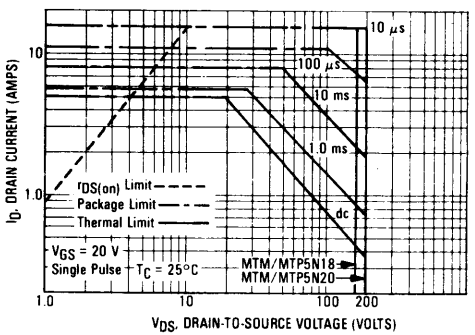
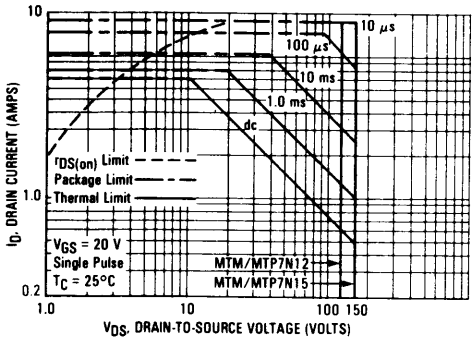


FIGURE 14 — MTM7N12, MTM7N15
MTP7N12, MTP7N15



FORWARD BIASED SAFE OPERATING AREA

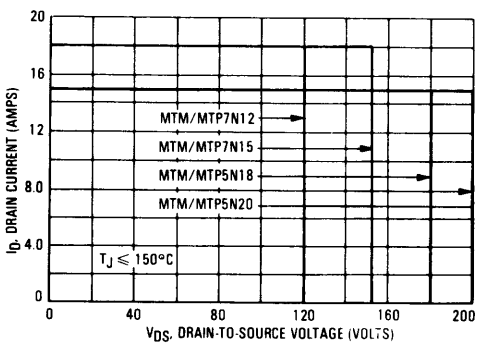
The dc data of Figures 13 and 14 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figures 13 and 14.
$T_{J(max)}$ = rated maximum junction temperature.
T_C = device case temperature.
P_D = rated power dissipation at T_C = 25°C.
$R_{\theta JC}$ = rated steady state thermal resistance
r(t) = normalized thermal response from Figures 11 and 12.

FIGURE 15 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 15, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 15 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

3

TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 16. Reversal of the drain voltage will cause current flow in the reverse direction. This diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 16 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

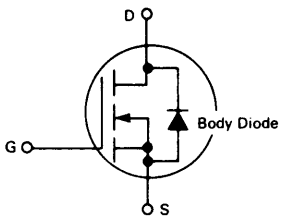


FIGURE 17 — DIODE TURN-ON TEST CIRCUIT

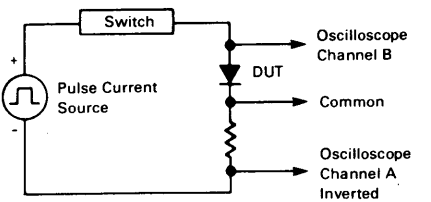


FIGURE 18 — BODY DIODE TURN-ON WAVEFORMS

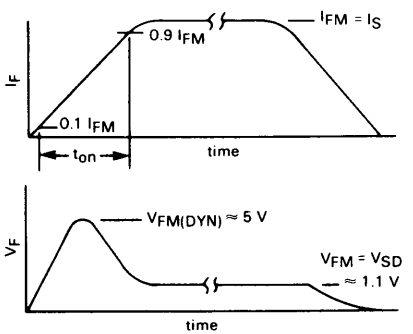


FIGURE 19 — REVERSE RECOVERY CHARACTERISTIC

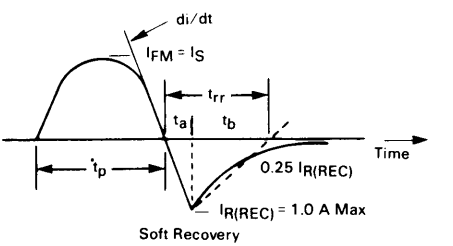
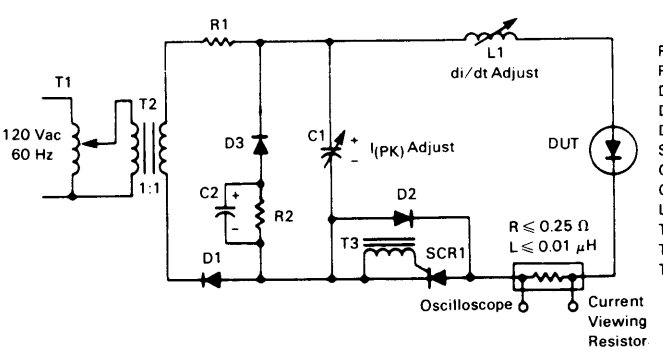


FIGURE 20 — JEDEC REVERSE RECOVERY CIRCUIT



R1 = 50 Ohms
R2 = 250 Ohms
D1 = 1N4723
D2 = 1N4001
D3 = 1N4933
SCR1 = MCR729-10
C1 = 0.5 to 50 μF
C2 = 4000 μF
L1 = 1.0-27 μH
T1 = Variac Adjusts $I_{(PK)}$ and di/dt
T2 = 1:1
T3 = 1:1 (to trigger circuit)