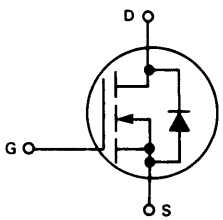
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)}$ = 4.5 Volts (max)

TMOS™

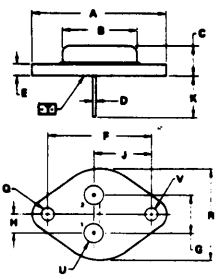


6 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 1.5 OHMS
550 and 600 VOLTS

MTM6N55
MTM6N60



STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-3 TYPE

MAXIMUM RATINGS

Rating	Symbol	MTM6N55	MTM6N60	Unit
Drain — Source Voltage	V_{DSS}	550	600	Vdc
Drain — Gate Voltage (R_{GS} = 1.0 mΩ)	V_{DGR}	550	600	Vdc
Gate — Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 6.0 30		Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	0.83	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves—representing boundaries on device characteristics—are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM6N55 MTM6N60	$V_{(BR)DSS}$	 550 600	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 BV_{DSS}, V_{GS} = 0) T_J = 100°C		I_{DSS}	 — —	 0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS}) T_J = 100°C		$V_{GS(th)}$	 2.0 1.5	 4.5 4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 3.0 Adc) (I_D = 6.0 Adc) (I_D = 3.0 Adc, T_J = 100°C)		$V_{DS(on)}$	 — — —	 4.5 10 9.0	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3.0 Adc)		$r_{DS(on)}$	—	1.5	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 3.0 A)		g_{fs}	2.0	—	mhos
SAFE OPERATING AREAS					
Forward Biased Safe Operating Area		FBSOA	See Figure 9		
Switching Safe Operating Area		SSOA	See Figure 10		
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1800	pF
Output Capacitance		C_{oss}	—	350	pF
Reverse Transfer Capacitance		C_{rss}	—	150	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 125 V, I_D = 3.0 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	150	ns
Turn-Off Delay Time		$t_{d(off)}$	—	200	ns
Fall Time		t_f	—	120	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 6.0 A	V_{SD}	1.0	Vdc
Forward Turn-On Time	V_{GS} = 0, di/dt = 25 A/μs	t_{on}	175	ns
Reverse Recovery Time	See Figures 14 and 15	t_{rr}	600	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

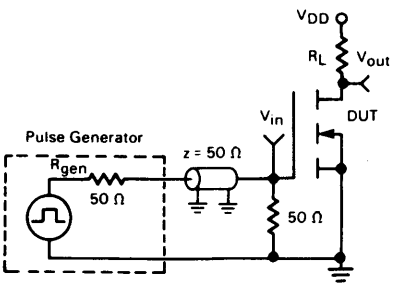
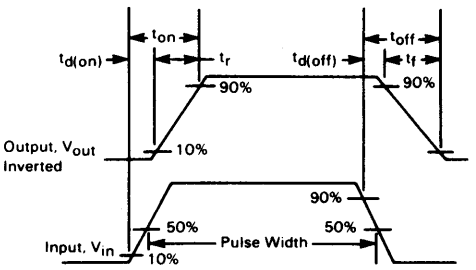


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

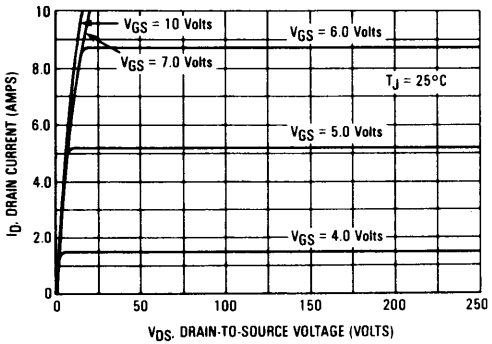


FIGURE 4 — ON-REGION CHARACTERISITCS

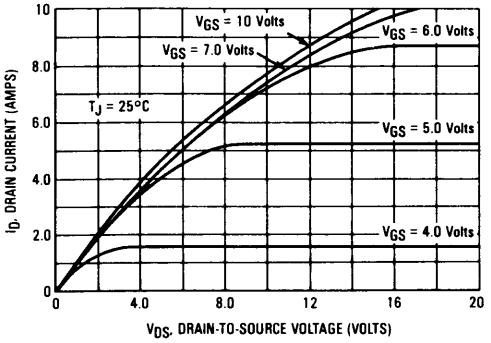


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE (NORMALIZED)

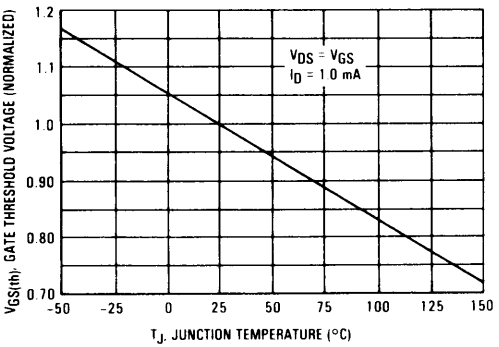


FIGURE 6 — TRANSFER CHARACTERISTICS

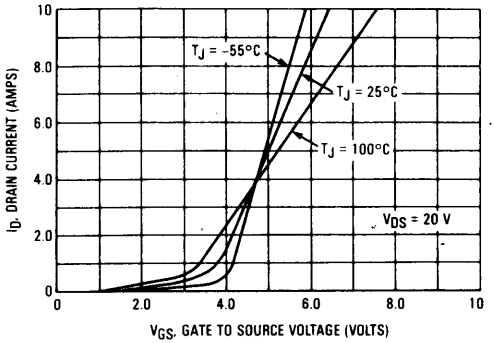


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

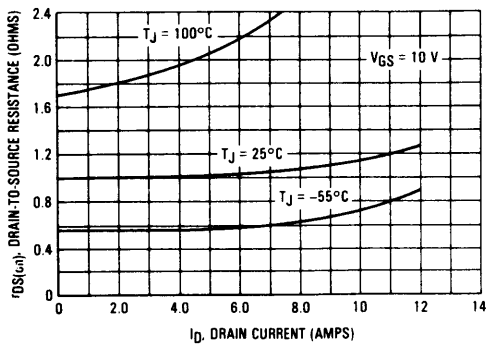
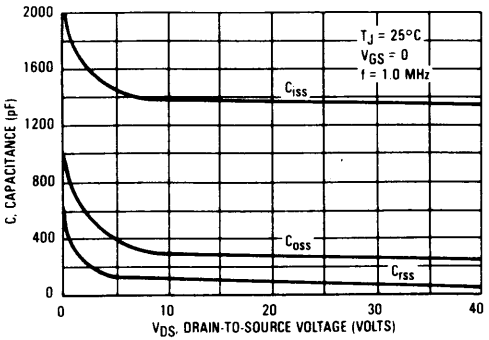


FIGURE 8 — CAPACITANCE VARIATION



SAFE OPERATING AREA INFORMATION

FIGURE 9 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

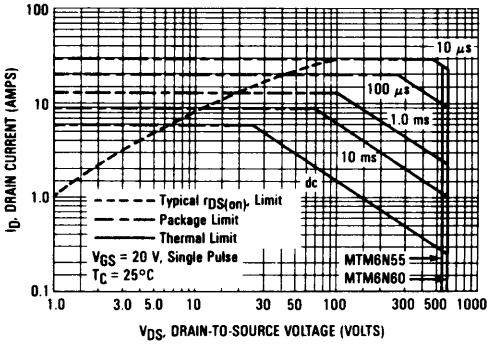
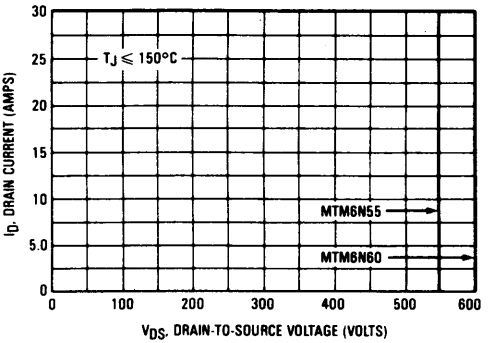


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



FORWARD BIASED

The data of Figure 9 is based on $T_C = 25°C$; $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 9 may be calculated for any case temperature with the aid of the following equation:

$$I_{D(T_C)} = I_{D(25°C)} \left[1 - \frac{T_C - 25°C}{P_D R_{\theta JC}} \right]$$

where

$I_{D(T_C)}$ = the maximum allowable current at a case temperature, T_C.

$I_{D(25°C)}$ = the maximum allowable current at a given voltage from Figure 9.

P_D = the rated power dissipation at $T_C = 25°C$.

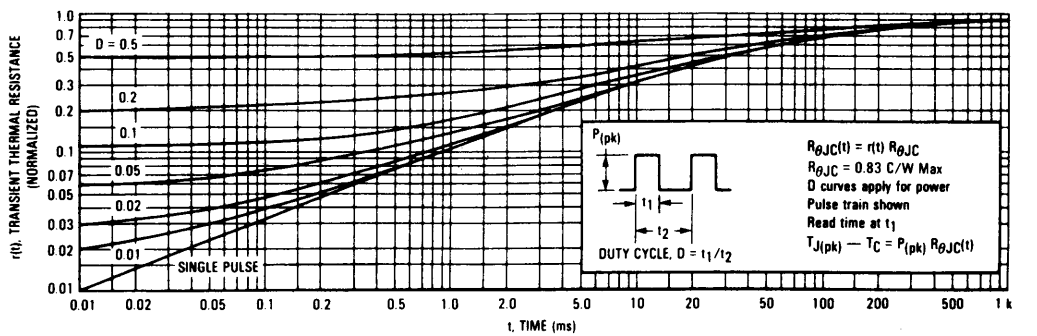
$R_{\theta JC}$ = the rated steady state thermal resistance

For various pulse widths and duty cycles, substitute $R_{\theta JC(t)}$ determined from Figure 11 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

FIGURE 11 — MTM6N55/MTM6N60



TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 11. Reversal of the drain voltage will cause current flow in the reverse direction. This diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 12 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

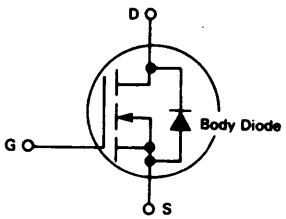


FIGURE 13 — DIODE TURN-ON TEST CIRCUIT

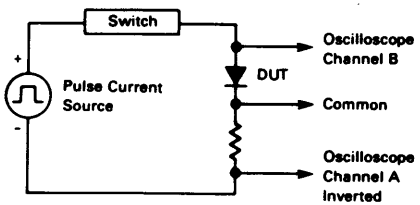


FIGURE 14 — DIODE TURN-ON WAVEFORMS

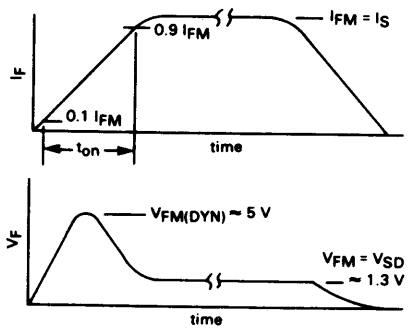


FIGURE 15 — REVERSE RECOVERY CHARACTERISTIC

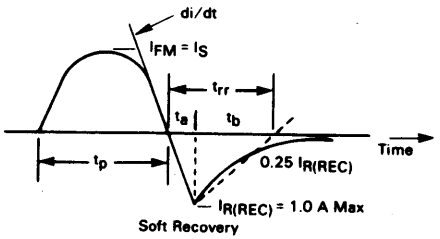
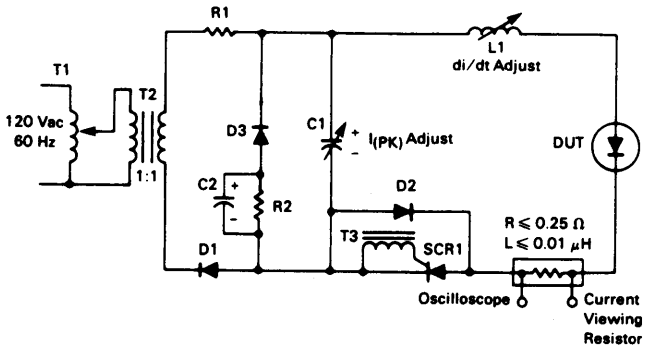


FIGURE 16 — JEDEC REVERSE RECOVERY CIRCUIT



R1 = 50 Ohms
R2 = 250 Ohms
D1 = 1N4723
D2 = 1N4001
D3 = 1N4933
SCR1 = MCR729-10
C1 = 0.5 to 50 μF
C2 = 4000 μF
L1 = 1.0–27 μH
T1 = Variac Adjusts $I_{(PK)}$ and di/dt
T2 = 1:1
T3 = 1:1 (to trigger circuit)

TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 500 mA. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

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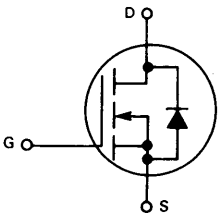
- Designer's Data — I_{DSS}, $V_{DS(on)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement, $V_{G(th)}$ = 4.5 Volts (max)

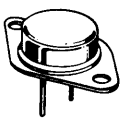
TMOS™



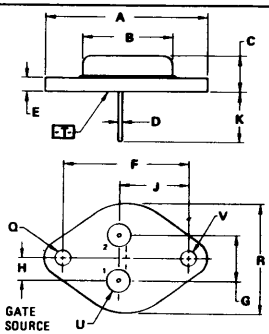
7 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 0.8 OHM
450 and 500 VOLTS



CASE 1-05
TO-3 TYPE



STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | 0.13 (0.005) M | T | V M
   FOR LEADS:
   ⌖ | 0.13 (0.005) M T | V M | Q M
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.46	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
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J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

MAXIMUM RATINGS

Rating	Symbol	MTM7N45	MTM7N50	Unit
Drain — Source Voltage	V_{DSS}	450	500	Vdc
Drain — Gate Voltage (R_{GS} = 1.0 mΩ)	V_{DGR}	450	500	Vdc
Gate — Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 7.0 35		Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	0.83	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

DS3420R1

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM7N45 MTM7N50	$V_{(BR)DSS}$	 450 500	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0) T_J = 100°C		I_{DSS}	 — —	 0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS}) T_J = 100°C		$V_{GS(th)}$	 2.0 1.5	 4.5 4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 3.5 Adc) (I_D = 7.0 Adc) (I_D = 3.5 Adc, T_J = 100°C)		$V_{DS(on)}$	 — — —	 4.2 10 8.4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3.5 A)		$r_{DS(on)}$	—	0.8	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 3.5 A)		g_{fs}	2.0	—	mhos
SAFE OPERATING AREAS					
Forward Biased Safe Operating Area		FBSOA	See Figure 9		
Switching Safe Operating Area		SSOA	See Figure 10		
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1800	pF
Output Capacitance		C_{oss}	—	350	pF
Reverse Transfer Capacitance		C_{rss}	—	150	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 125 V, I_D = 3.5 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	150	ns
Turn-Off Delay Time		$t_{d(off)}$	—	250	ns
Fall Time		t_f	—	120	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 7.0 A	V_{SD}	1.1	Vdc
Forward Turn-On Time	V_{GS} = 0, di/dt = 25 A/μs	t_{on}	175	ns
Reverse Recovery Time	See Figures 14 and 15	t_{rr}	600	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

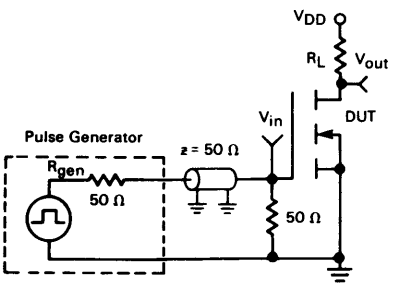
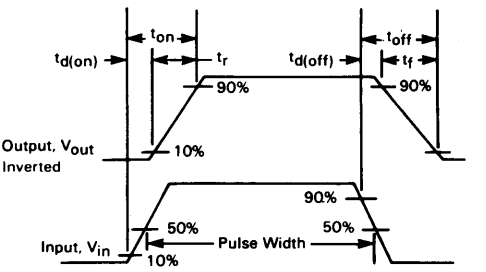


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

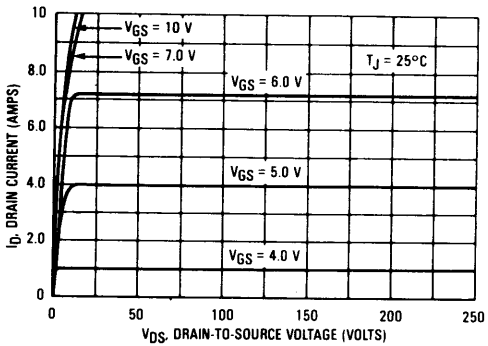


FIGURE 4 — ON-REGION CHARACTERISITCS

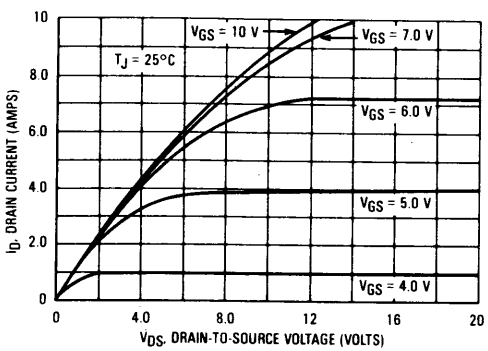


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

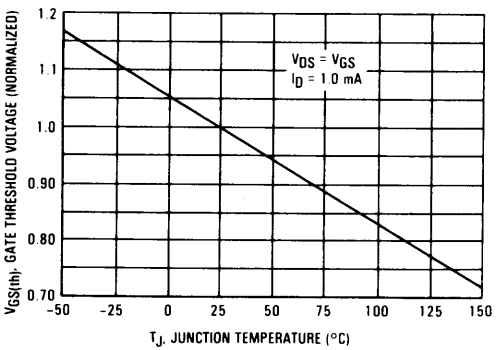


FIGURE 6 — TRANSFER CHARACTERISTICS

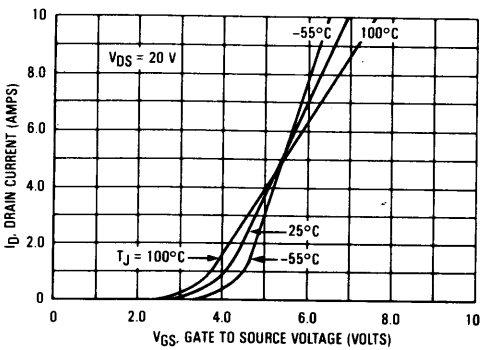


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

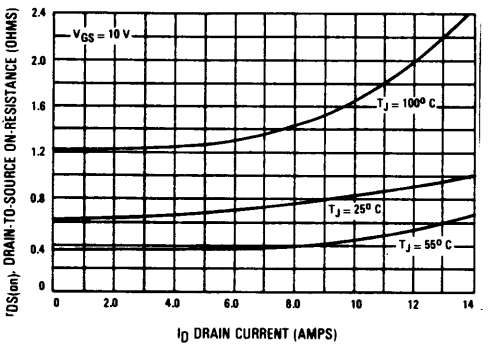
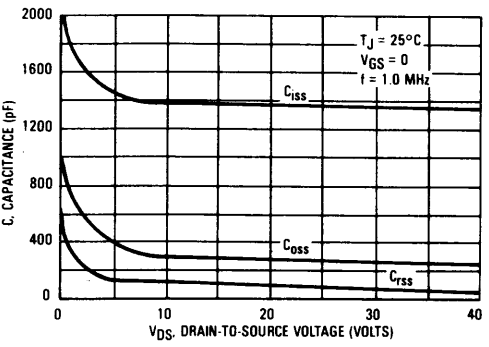


FIGURE 8 — CAPACITANCE VARIATION



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TYPICAL CHARACTERISTICS

FIGURE 9 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

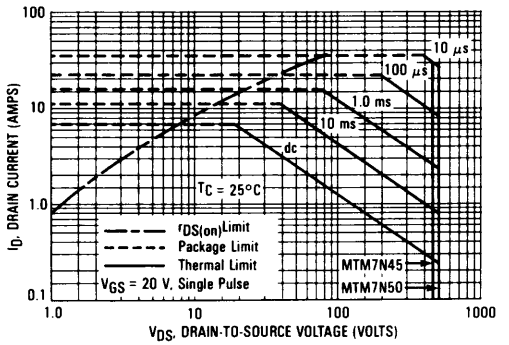
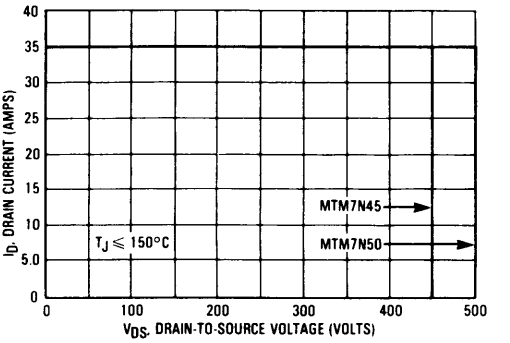


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIASED

The data of Figure 9 is based on $T_C = 25°C$; $T_{J(pk)}$ is a variable depending on the power level. The allowable current at the voltages shown in Figure 9 may be calculated for any case temperature with the aid of the following equation:

$$I_{D(T_C)} = I_{D(25°C)} \left[1 - \frac{T_C - 25°C}{P_D R_{\theta JC}} \right]$$

where

$I_{D(T_C)}$ = the maximum allowable current at a case temperature, T_C.

$I_{D(25°C)}$ = the maximum allowable current at a given voltage from Figure 9.

P_D = the rated power dissipation at $T_C = 25°C$.

$R_{\theta JC}$ = the rated steady state thermal resistance

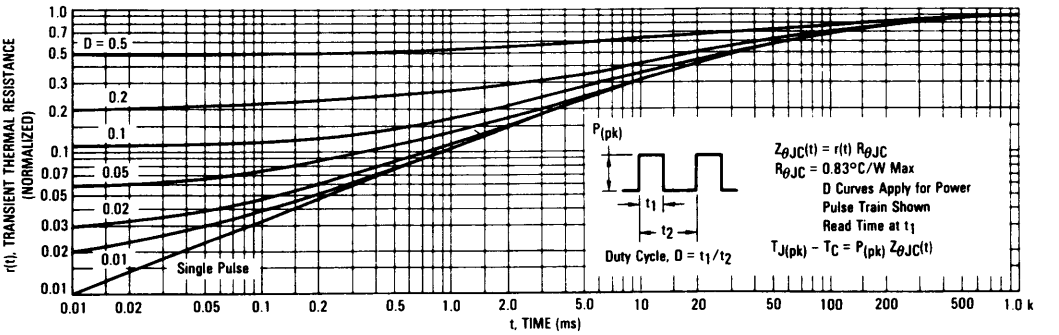
For various pulse widths and duty cycles, substitute $R_{\theta JC}(t)$ determined from Figure 11 for $R_{\theta JC}$.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 10, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 10 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

THERMAL RESPONSE

FIGURE 11 — THERMAL RESPONSE



TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 500 mA. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

TMOS SOURCE TO DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 12. Reversal of the drain voltage will cause current flow in the reverse direction. This diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

FIGURE 12 — TMOS FET WITH SOURCE-TO-DRAIN DIODE

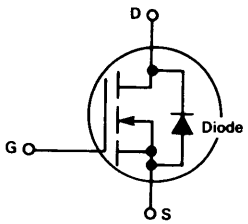


FIGURE 13 — DIODE TURN-ON TEST CIRCUIT

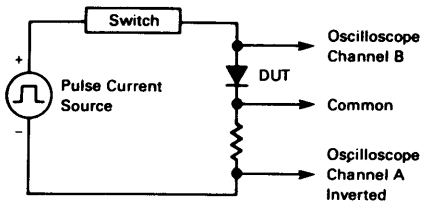


FIGURE 14 — DIODE TURN-ON WAVEFORMS

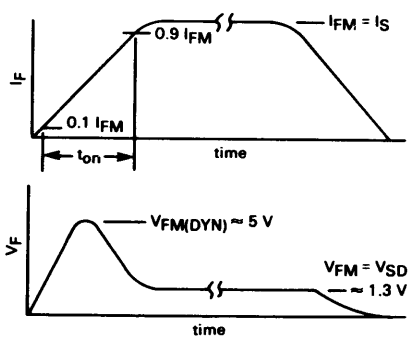


FIGURE 15 — REVERSE RECOVERY CHARACTERISTIC

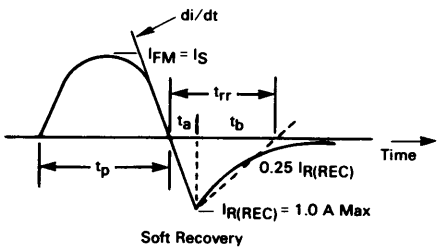


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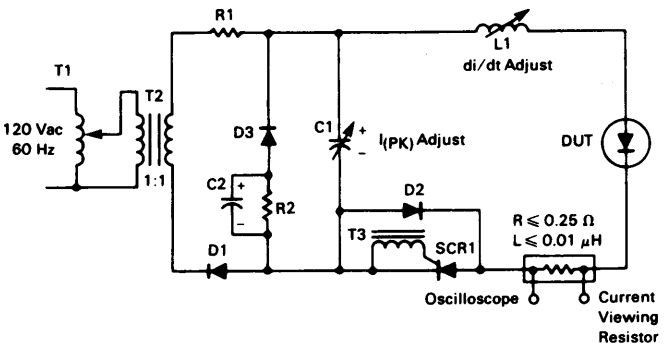
FIGURE 16 — JEDEC REVERSE RECOVERY CIRCUIT



R1 = 50 Ohms
R2 = 250 Ohms
D1 = 1N4723
D2 = 1N4001
D3 = 1N4933
SCR1 = MCR729-10
C1 = 0.5 to 50 μF
C2 = 4000 μF
L1 = 1.0–27 μH
T1 = Variac Adjusts $I_{(PK)}$ and di/dt
T2 = 1:1
T3 = 1:1 (to trigger circuit)

3