MT101B SINGLE MOST
MT102B MATCHED MOST PAIR

The MT 101B is a single p-channel enhancement mode MOS transistor with ultra-high input impedance, this characteristic making it suitable for many electrometer applications. It has no offset source-drain potential. The device is available in a T0-18 encapsulation.

The MT102B is a matched pair of devices similar to MT101B in a T0-5 encapsulation.

To achieve the ultra high input impedance, no gate protection diodes are incorporated in these devices. Special care must therefore be taken when handling the device, to keep the gate voltage within its absolute maximum rating of ±40V. (See Operating Notes).

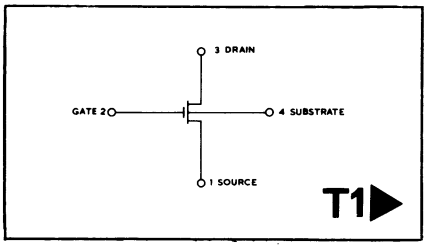

Fig. 1 MT 101B circuit diagram

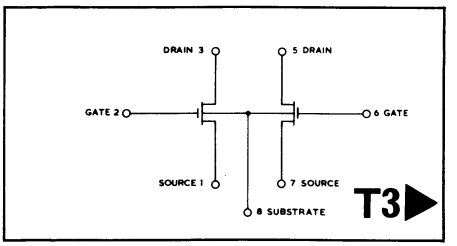

Fig. 2 MT 102B circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions: Temperature= +20°C ±2°C
V_{SSUB}=0V (except where otherwise stated)

Characteristic	Symbol	Circuit	Value			Units	Test conditions
			Min.	Typ.	Max.		
*Threshold voltage	TV_{GS}	MT101B MT102B	3·8	5·1	6·5	V (neg.)	$V_{GS}=V_{DS}$ I_D=10μA
D.C. drain resistance	r_{DS}	,,					$V_{DS}\leqslant$100mV
with V_{GS}= −10V				470	850	Ω	
with V_{GS}= −20V				200	350	Ω	
A.C. drain resistance	r_{ds}	,,	30	55		kΩ	V_{DS}= −10V V_{GS}= −7V $I_D\simeq$1mA
Gate source resistance	r_{GS}	,,		10^{14}		Ω	V_{GS}= −24V V_{DS}=0V
A.C. mutual conductance	g_m	,,	0·65	0·85		mA/V	$V_{GS}=V_{DS}$ I_D=1mA
Drain-source leakage	I_{DS}	,,		1·0	20	nA	V_{DS}= −20V V_{GS}=0V
Drain-substrate leakage	I_{DSUB}	,,		2·0	20	nA	V_{DSUB}= −20V V_{GS}=0V
Source-substrate leakage	I_{SSUB}	,,		2·0	20	nA	V_{SSUB}= −20V V_{GS}=0V

Characteristic	Symbol	Circuit	Value			Units	Test conditions
			Min.	Typ.	Max.		
Gate-source capacitance	C_{gs}	,,		4·6	6·9	pF	$V_{GS}=V_{DS}$ $I_D=1mA$ f=1MHz
Gate-drain capacitance	C_{gd}	,,		2·6	3·9	pF	$V_{GS}=V_{DS}$ $I_D=1mA$ f=1MHz
Drain-source capacitance	C_{ds}	,,		2·6	3·9	pF	$V_{GS}=V_{DS}$ $I_D=1mA$ f=1MHz
Drain-substrate capacitance	C_{dsub}	,,		3·4	5·1	pF	$V_{DSUB}=0V$ Source and gate open circuit f=1MHz
Source-substrate capacitance	C_{ssub}	,,		4·4	6·6	pF	$V_{SSUB}=0V$ Gate and drain open circuit f=1MHz
Temperature coefficient of drain resistance	—	MT101B MT102B		0·4		%/°C	$V_{GS}=-20V$ $V_{DS}=100mV$
Temperature coefficient of threshold voltage	—	,,		−3·6		mV/°C	$V_{GS}=V_{DS}$ $I_D=10\mu A$
Matching threshold voltage	ΔTV_{GS}	MT102B		50	200	mV	$V_{GS}=V_{DS}$ $I_D=10\mu A$
Matching d.c. drain resistance	Δr_{DS}	MT102B		20	40	Ω	$V_{GS}=-20V$ $V_{DS} \leqslant 100mV$
Matching a.c. mutual conductance	Δg_m	MT102B		35		µA/V	$V_{GS}=V_{DS}$ $I_D=1mA$

* To avoid confusion, maximum & minimum values of negative quantities are taken as referring to the magnitude of a parameter and sign is indicated in the units column.

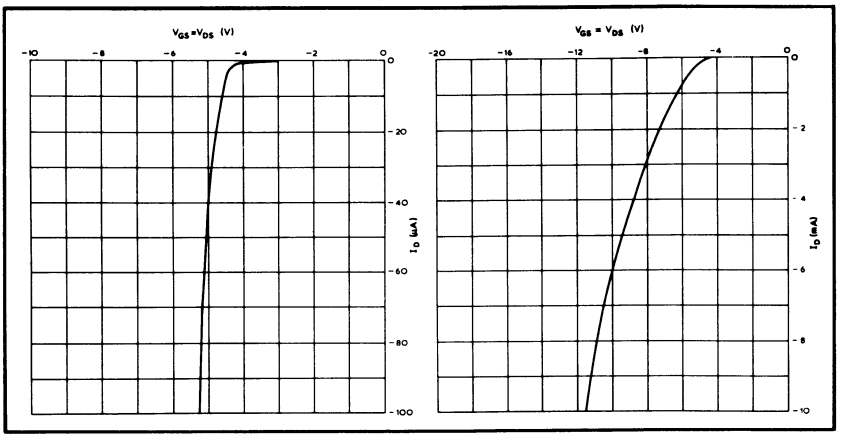

Fig. 3 Turn on characteristics at +25°C

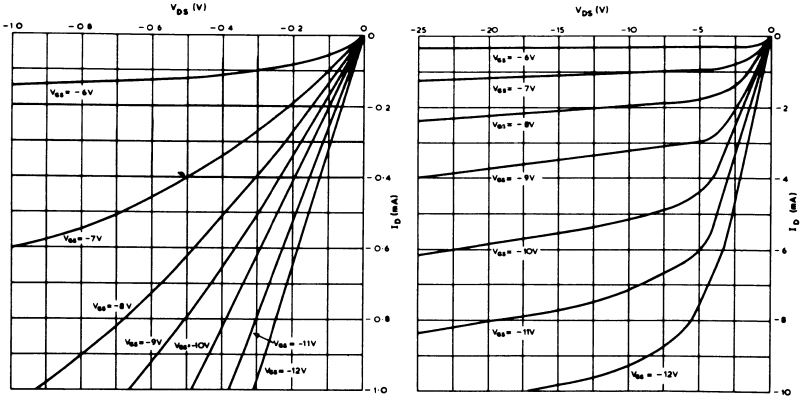

Fig. 4 Drain characteristics at +25°C

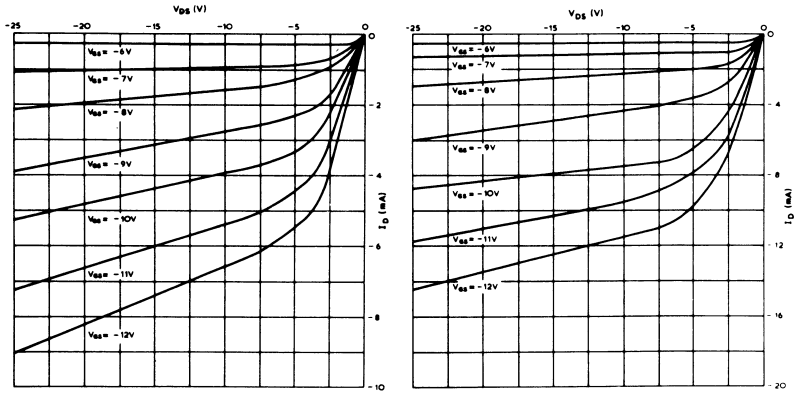

Fig. 5 Drain characteristics at +125°C

Fig. 6 Drain characteristics at − 55°C

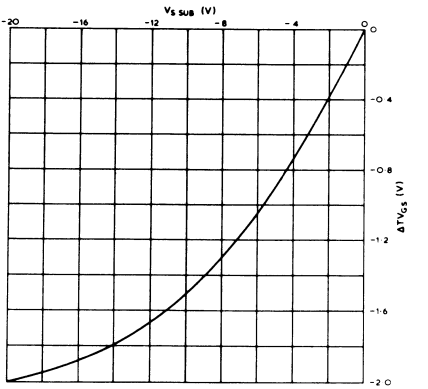

Fig. 7 Change of threshold voltage as a function of source - substrate bias at + 25°C

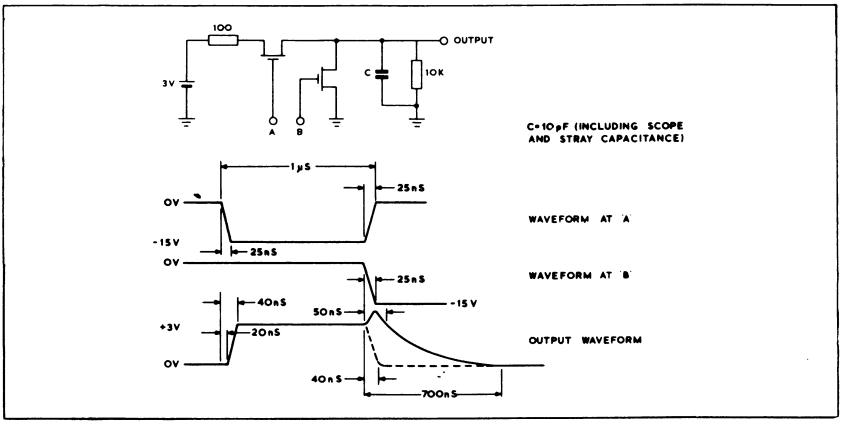

Fig. 8 Switching circuit typical waveforms

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting absolute values above which operating life may be shortened or satisfactory performance may be impaired.

Storage temperature	−55°C to +125°C
Chip temperature	+125°C
Chip-to-ambient thermal resistance	
MT101B	486°C/W
MT102B	250°C/W
Chip-to-case thermal resistance	
MT101B	146°C/W
MT102B	80°C/W
Gate breakdown voltage	±40V
Drain-source breakdown voltage	±40V
Drain (or source) -substrate breakdown voltage	-40V
Drain (or source) -substrate positive voltage	0.3V
Drain current	20mA

OPERATING NOTES

The identification of the source and drain of this type of MOS transistor is purely arbitrary because of the symmetrical nature of its construction. In multiple

Cascaded amplifier stages using these MOS transistors may be directly coupled.

CAUTION

These devices have very low input capacitance and extremely high input resistance. A very small charge can therefore cause the gate voltage to exceed its absolute maximum rating and cause permanent damage to the device. When handling the device, the leads should at all times be shorted together until actually incorporated in the circuit in which the device is being used. Care should be taken to avoid static charges occurring in the circuit before completion and soldering should be carried out with an earthed bit.

To ensure no damage occurs during transit, the devices are supplied with a shorting device round the leads.