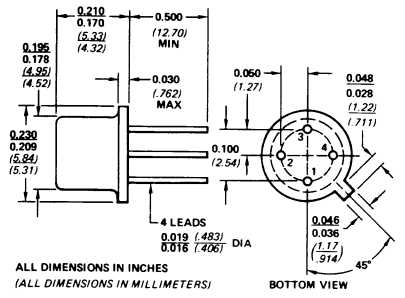
Performance Curves MBL
See Page 4-6

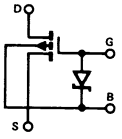
P-CHANNEL ENHANCEMENT-TYPE SILICON MOS FIELD-EFFECT TRANSISTOR

NORMALLY-OFF MOS FET FOR ANALOG AND DIGITAL SWITCHING APPLICATIONS

- Integrated Zener Clamp Protects the Gate
- Low $V_{GS(th)}$
- Very Low $I_{D(off)}$ and $I_{S(off)}$



TO-72



PIN	OUT
1	D
2	G
3	B,C
4	S

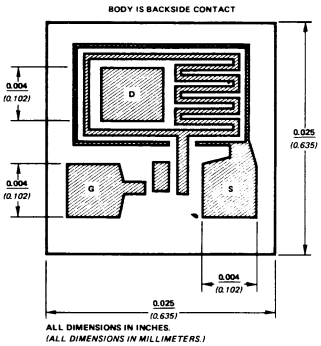
ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Source Voltage	-30 V
Gate-to-Source Voltage	-30 V
Gate-to-Drain Voltage	-30 V
Drain Current	-50 mA
Gate Current (Forward Direction for Zener Clamp)	±0.1 mA
Storage Temperature	-65 to 150°C
Operating Junction Temperature	-55 to 125°C
Total Device Dissipation (Derate 2.25 mW/°C to 125°C)	225 mW

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	-30		V	I_D = -1 μA, V_{GS} = V_{BS} = 0	
2		BV_{SDS}	Source-Drain Breakdown Voltage	-30			I_S = -1 μA, V_{GD} = V_{BD} = 0	
3		BV_{GBS}	Gate-Body Breakdown Voltage	-30	-90		I_G = -10 μA, V_{SB} = V_{DB} = 0	
4		I_{GSS}	Gate-Body Leakage		-0.1	nA	V_{GS} = -20 V, V_{DS} = V_{BS} = 0	
5		$I_{D(off)}$	Drain Cutoff Current		-0.2		V_{DS} = -20 V, V_{GS} = V_{BS} = 0	
6		$I_{S(off)}$	Source Cutoff Current		-0.2		V_{SD} = -20 V, V_{GD} = V_{BD} = 0	
7		$V_{GS(th)}$	Gate Threshold Voltage	-1	-3	V	V_{GS} = V_{DS}, I_D = -10 μA, V_{BS} = 0	
8		$r_{DS(on)}$	Drain Source ON Resistance		400	Ω	V_{GS} = -5 V, I_D = -100 μA, V_{BS} = 0	
9					200		V_{GS} = -10 V, I_D = -100 μA, V_{BS} = 0	
10	DYN	C_{gs} or C_{gd}	Gate-Source or Gate-Drain Capacitance		4	pF	V_{GB} = V_{DB} = V_{SB} = 0 Body Guarded	f = 1 MHz
11		C_{sb} or C_{db}	Source-Body or Drain-Body Capacitance		5		V_{GB} = 0, V_{DB} = V_{SB} = -5 V	
12		C_{ds}	Drain-Source Capacitance		0.3		V_{GB} = 0, V_{DB} = V_{SB} = -5 V Body Guarded	

MBL



P-CHANNEL ENHANCEMENT-TYPE SILICON MOS FIELD-EFFECT TRANSISTOR

APPLICATIONS

- Analog and Switching Circuits
- Audio Amplifiers

PRINCIPAL DEVICE

M113

PACKAGE TYPE

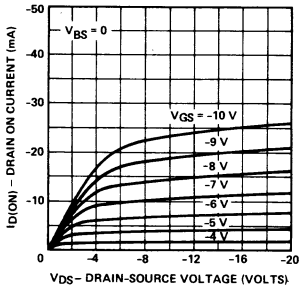
TO-72

FEATURES

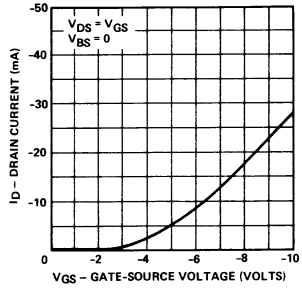
- Integrated Zener Clamp Protects the Gate
- Low $V_{GS(th)}$
- Normally OFF

PERFORMANCE CURVES (25°C unless otherwise noted)

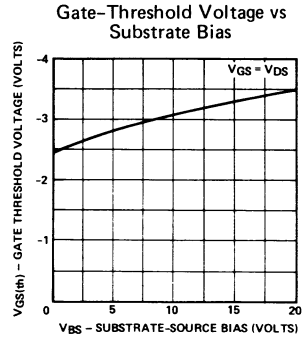
Output Characteristics



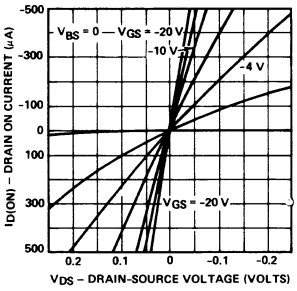
Transfer Characteristic



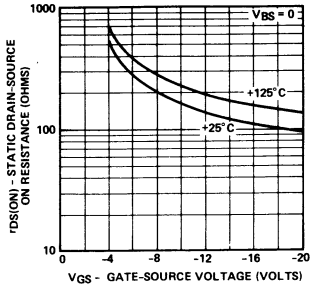
Gate-Threshold Voltage vs Substrate Bias



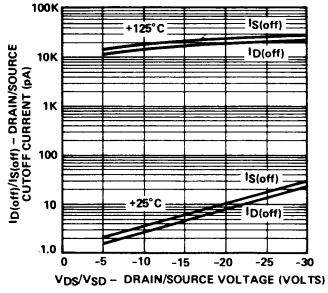
Low Voltage Output Characteristics



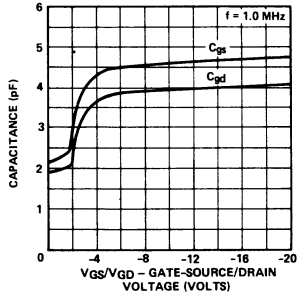
Drain-Source ON-State Resistance vs Gate-Source Bias



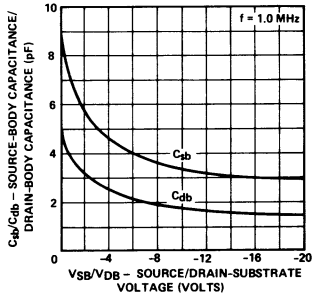
Leakage Currents vs Voltage



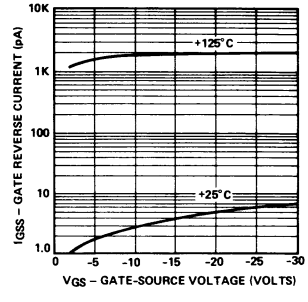
Gate Capacitance vs Voltage



Substrate Capacitance vs Voltage



Gate Leakage Current vs Gate-Source Bias

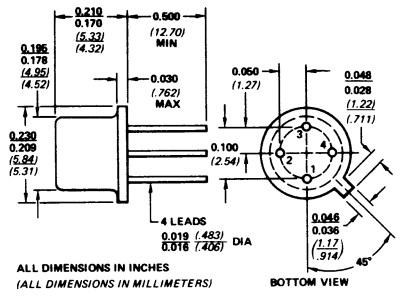


Performance Curves MBH
See Page 4-4

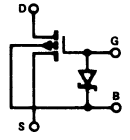
P-CHANNEL ENHANCEMENT-TYPE SILICON MOS FIELD-EFFECT TRANSISTOR

NORMALLY-OFF, INSULATED-GATE FET FOR ANALOG-GATE, GENERAL-PURPOSE AMPLIFIER AND DIGITAL SWITCHING APPLICATIONS

- Integrated Zener Clamp Protects the Gate
- Low I_{DSS} and I_{SDS}
- High BV_{DSS}, BV_{SDS} and BV_{GSS}



TO-72



PIN	OUT
1	D
2	G
3	B, C
4	S

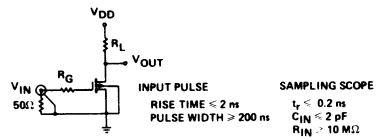
ABSOLUTE MAXIMUM RATINGS (25°C)

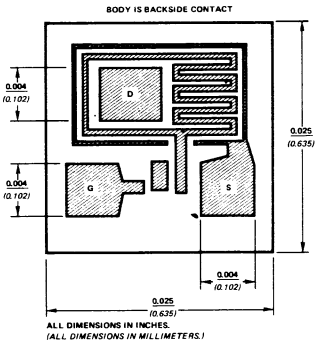
Drain-to-Source Voltage	-40 V
Gate-to-Source Voltage	-40 V
Gate-to-Drain Voltage	-40 V
Drain Current	-50 mA
Gate Zener Current	±0.1 mA
Storage Temperature	-65 to +150°C
Operating Junction Temperature	-55 to +125°C
Total Dissipation at 25°C Ambient Temperature (Derate 2.25 mW/°C)	225 mW

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	-40			V	I_D = -1 μA, V_{GS} = 0, V_{BS} = 0	
2		BV_{SDS}	Source-Drain Breakdown Voltage	-40				I_S = -1 μA, V_{GD} = 0, V_{BD} = 0	
3		BV_{GBS}	Gate-Body Breakdown Voltage	-40		-110		I_G = -1 μA, V_{SB} = 0, V_{DB} = 0	
4		I_{GSS}	Gate-Body Leakage		-6	-100	pA	V_{GS} = -20 V, V_{DS} = 0, V_{BS} = 0	
5		$I_{D(off)}$	Drain Cutoff Current		-15	-200		V_{DS} = -20 V, V_{GS} = 0, V_{BS} = 0	
6		$I_{S(off)}$	Source Cutoff Current		-16	-200		V_{SD} = -20 V, V_{GD} = 0, V_{BD} = 0	
7		$V_{GS(th)}$	Gate Threshold Voltage	-1.5	-2.9	-4.5	V	V_{GS} = V_{DS}, I_D = -10 μA, V_{BS} = 0	
8		$I_{D(on)}$	Drain Current	-8	-20	-35	mA	V_{DS} = -10 V, V_{GS} = -10 V, V_{BS} = 0	
9		$r_{DS(on)}$	Drain-Source ON Resistance		70	240	Ω	V_{GS} = -40 V, I_{DS} = -0.1 mA, V_{BS} = 0	
10					100	275		V_{GS} = -25 V, I_{DS} = -0.1 mA, V_{BS} = 15 V	
11					320	500		V_{GS} = -10 V, I_{DS} = -0.1 mA, V_{BS} = 30 V	
12		$V_{DS(on)}$	Drain- Source ON Voltage			900	mV	V_{GS} = -10 V, I_D = -2 mA, V_{BS} = 0	
13	DYNAMIC	9_{fs}	Common-Source Forward Transconductance	2,000	4,000		μmho	V_{DS} = -10 V, V_{GS} = -10 V, V_{BS} = 0	f = 1 kHz
14		C_{gs} or C_{gd}	Gate-Source or Gate-Drain Capacitance		2	4	pF	V_{GB} = 0, V_{DB} = 0, V_{SB} = 0 Body Guarded	f = 1 MHz
15		C_{sb}	Source-Body Capacitance		2.5	5		V_{GB} = 0, V_{DB} = -5 V, V_{SB} = -5 V	
16		C_{db}	Drain-Body Capacitance			4		V_{GB} = 0, V_{DB} = -5 V, V_{SB} = -5 V	
17		C_{ds}	Drain-Source Capacitance			0.3		V_{CB} = 0, V_{DB} = -5V, V_{SB} = -5V, Body Guarded	
18	SW	t_d	Turn-ON Delay Time			12	ns	V_{DD} = -15 V $I_{D(on)}$ = -10 mA R_G = R_L = 1.4 kΩ	See Below Circuit
19		t_r	Rise Time			24			
20		t_{off}	Turn-OFF Time			50			

MBH





P-CHANNEL ENHANCEMENT-TYPE SILICON MOS FIELD-EFFECT TRANSISTOR

APPLICATIONS

- Analog and Digital Switching

FEATURES

- Integrated Zener Clamp Protects the Gate
- Low $I_{D(off)}/I_{S(off)}$
- High Breakdown Voltage
- Low Leakage
- Normally OFF

PRINCIPAL DEVICE

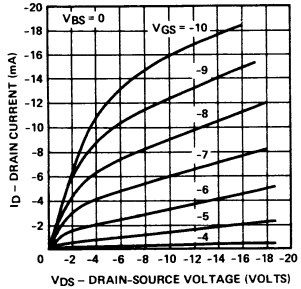
M114

PACKAGE TYPE

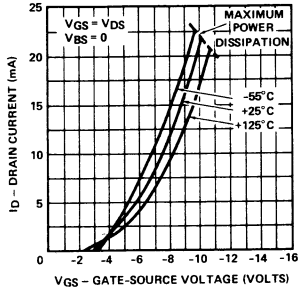
TO-72

PERFORMANCE CURVES (25°C unless otherwise noted)

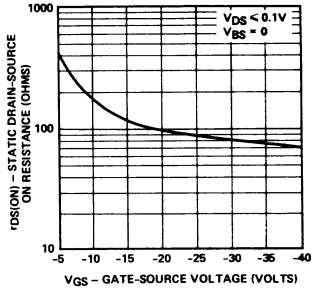
Output Characteristic



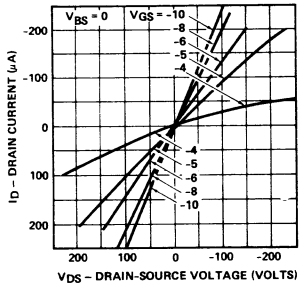
Transfer Characteristics



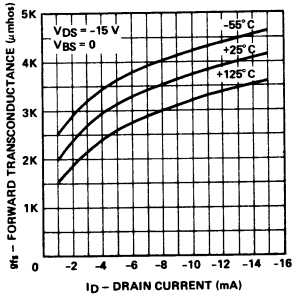
Drain-Source ON State Resistance vs Gate-Source Bias



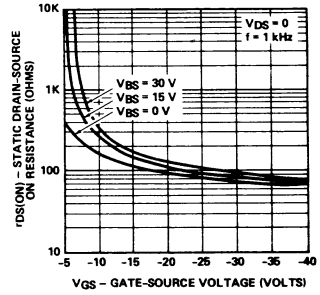
Low Voltage Output Characteristics



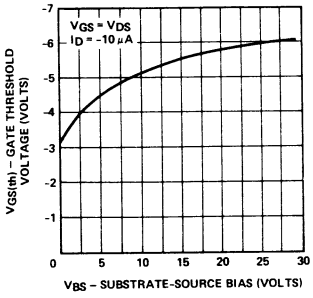
Forward Transconductance vs Drain Current



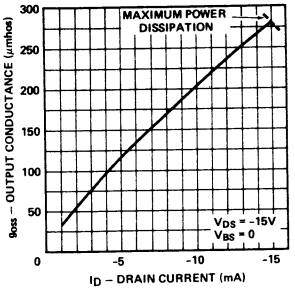
Drain-Source ON State Resistance vs Gate-Source Bias



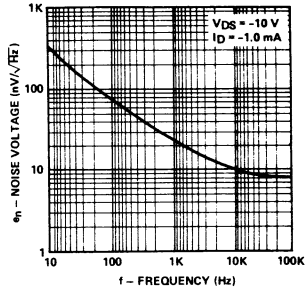
Gate-Threshold Voltage vs Substrate Bias



Output Conductance vs Drain Current

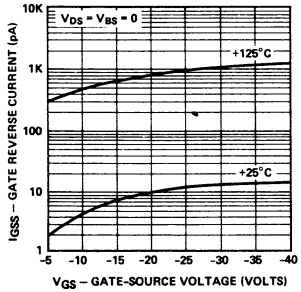


Short Circuit Equivalent Input Noise Voltage vs Frequency

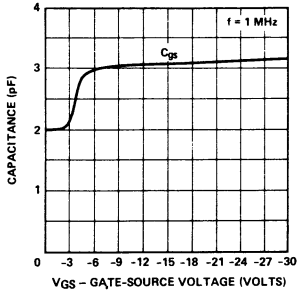


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

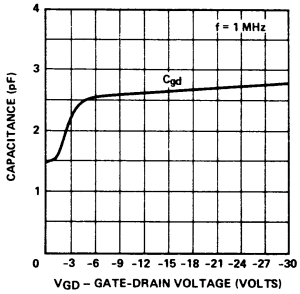
Gate Leakage Current vs Gate-Source Bias



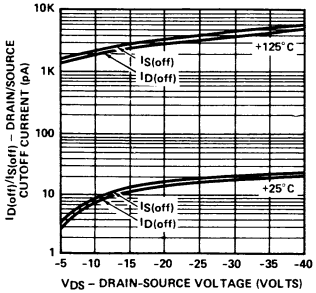
Gate-Source Capacitance vs Gate-Source Bias



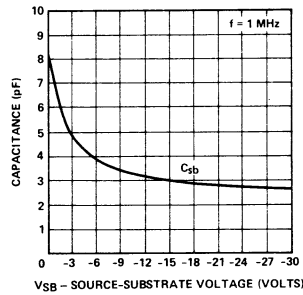
Gate-Drain Capacitance vs Voltage



Source-Drain Leakage Currents vs Voltage



Substrate Capacitance vs Voltage



Substrate Capacitance vs Voltage