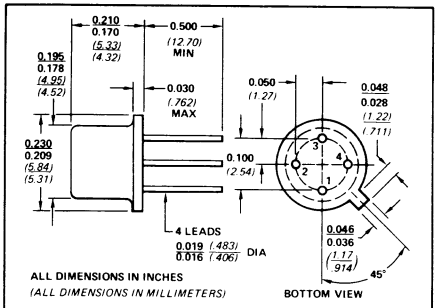
Performance Curves MBN MBNA

See Pages 4-7, 9

N-CHANNEL ENHANCEMENT-TYPE SILICON MOS FIELD-EFFECT TRANSISTOR

NORMALLY-OFF MOS FETS FOR AMPLIFIERS ANALOG AND DIGITAL SWITCHING APPLICATIONS

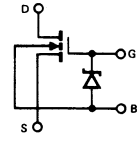
- Low I_{GSS}
- Integrated Zener Clamp Protects the M116 Gate



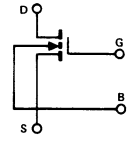
TO-72

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Source Voltage	30 V
Gate-to-Source Voltage M116	30 V
Gate-to-Source Voltage M117	±50 V
Gate-to-Drain Voltage M116	30 V
Gate-to-Drain Voltage M117	±50 V
Drain Current	50 mA
Gate Zener Current ... M116	±0.1 mA
Storage Temperature	-65 to 150°C
Operating Junction Temperature	−55 to +125°C
Total Device Dissipation (Derate 2.25 mW/°C to 125°C)	225 mW



M116	
PIN	OUT
1	D
2	G
3	B,C
4	S

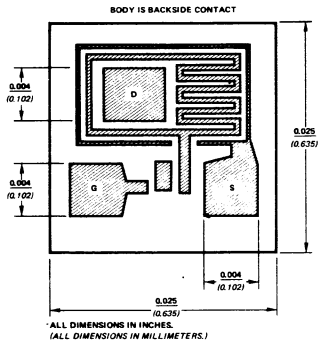


M117	
PIN	OUT
1	S
2	G
3	D
4	B,C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		M116 Min	M116 Max	M117 Min	M117 Max	Unit	Test Condition	
1	STATIC	I_{GSS}	Gate-Body Leakage		100		1.0	pA	V_{GS} = 20 V, V_{DS} = V_{BS} = 0	
2	STATIC	$V_{GS(th)}$	Gate Threshold Voltage	1	5	1	5	V	V_{GS} = V_{DS}, I_D = 10 μA, V_{BS} = 0	
3	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	30		30		V	I_D = 1 μA, V_{GS} = V_{BS} = 0	
4	STATIC	BV_{SDS}	Source-Drain Breakdown Voltage	30		30		V	I_S = 1 μA, V_{GD} = V_{BD} = 0	
5	STATIC	BV_{GBS}	Gate-Body Breakdown Voltage	30	60	±100[1]		V	I_G = 10 μA, V_{SB} = V_{DB} = 0	
6	STATIC	$I_{D(off)}$	Drain Cutoff Current		10		10	nA	V_{DS} = 20 V, V_{GS} = V_{BS} = 0	
7	STATIC	$I_{S(off)}$	Source Cutoff Current		10		10	nA	V_{SD} = 20 V, V_{GD} = V_{BD} = 0	
8	STATIC	$I_{D(on)}$	ON Drain Current	2	20	2	20	mA	V_{GS} = V_{DS} = -10 V, V_{BS} = 0	
9	STATIC	$r_{DS(on)}$	Drain Source ON Resistance		100		100	Ω	V_{GS} = 20 V, I_D = 100 μA, V_{BS} = 0	
10	STATIC	$r_{DS(on)}$	Drain Source ON Resistance		200		200	Ω	V_{GS} = 10 V, I_D = 100 μA, V_{BS} = 0	
11	DYN	C_{iss}	Input Capacitance		10		8	pF	V_{GB} = 0, V_{DB} = 10 V, V_{BS} = 0	f = 1 MHz
12	DYN	C_{gs} or C_{gd}	Gate-Source or Gate-Drain Capacitance		2.5		2.5	pF	V_{GB} = V_{DB} = V_{SB} = 0 Body Guarded	f = 1 MHz
13	DYN	C_{db}	Drain-Body Capacitance		7		7	pF	V_{GB} = 0, V_{DB} = 10 V	f = 1 MHz
				MBN		MBNA				

Note:
1 Gate -oxide breakdown voltage.



N-CHANNEL ENHANCEMENT-TYPE SILICON MOS FIELD-EFFECT TRANSISTOR

APPLICATIONS

- Audio Amplifiers
- Analog Circuits
- Digital Switching Circuits
- Commutating Circuits

PRINCIPAL DEVICE

M116

PACKAGE TYPE

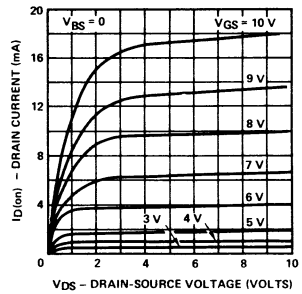
TO-72

FEATURES

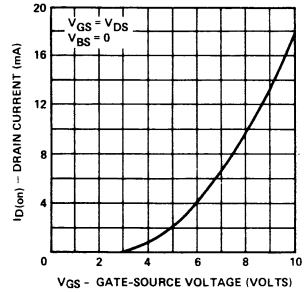
- Integrated Zener Clamp Protects the Gate
- Normally OFF

PERFORMANCE CURVES (25°C unless otherwise noted)

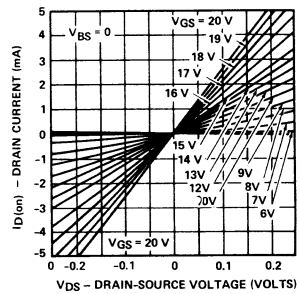
Output Characteristics



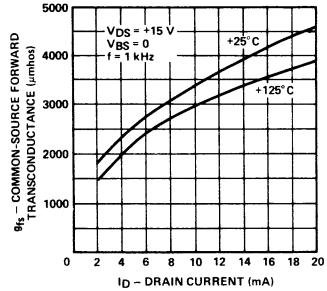
Transfer Characteristic



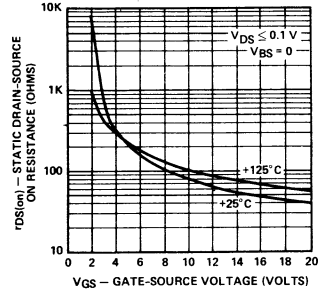
Low Voltage Output Characteristics



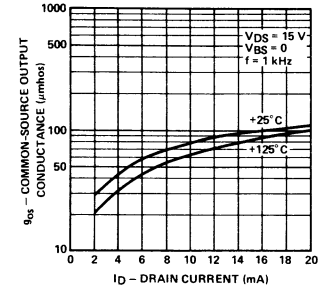
Forward Transconductance vs Drain Current



Drain-Source ON State Resistance vs Gate-Source Bias

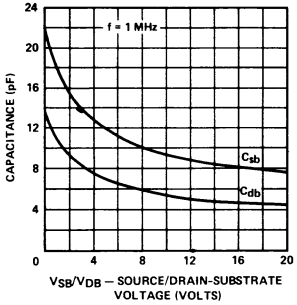


Output Conductance vs Drain Current

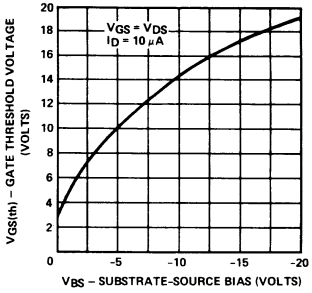


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

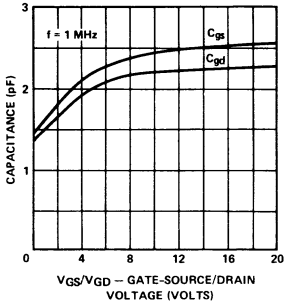
Substrate Capacitance vs Voltage



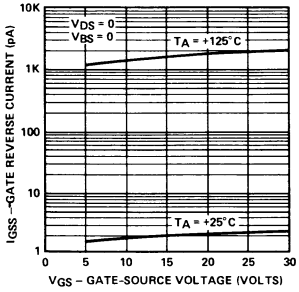
Gate Threshold Voltage vs Substrate Bias



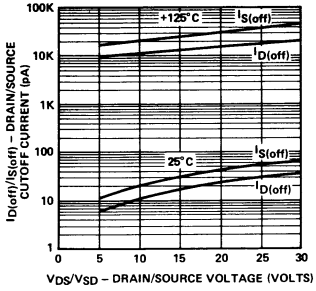
Gate Capacitance vs Voltage

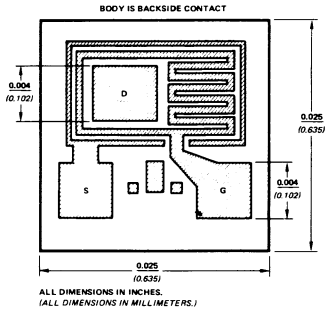


Gate Leakage Current vs Gate-Source Bias



Source-Drain Leakage Currents vs Voltage





N-CHANNEL ENHANCEMENT-TYPE SILICON MOS FIELD-EFFECT TRANSISTOR

APPLICATIONS

- Audio Amplifiers
- Analog Circuits
- Digital Switching Circuits
- Commutating Circuits

PRINCIPAL DEVICE

M117

PACKAGE TYPE

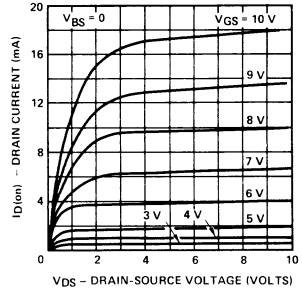
TO-72

FEATURES

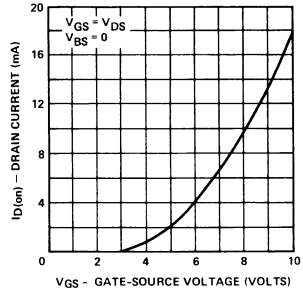
- Ultra-Low Gate Leakage
- Normally OFF

PERFORMANCE CURVES (25°C unless otherwise noted)

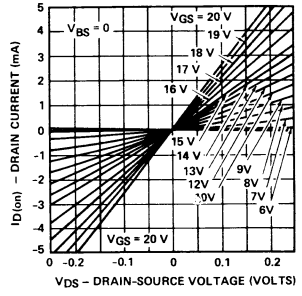
Output Characteristics



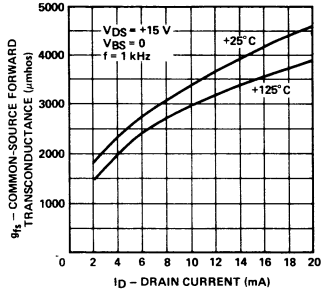
Transfer Characteristic



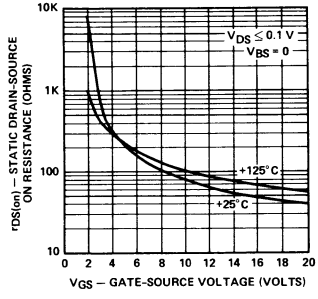
Low Voltage Output Characteristics



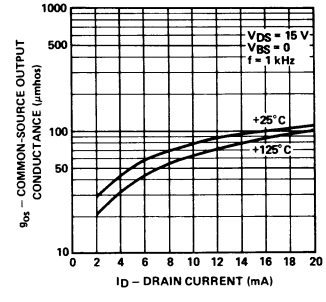
Forward Transconductance vs Drain Current



Drain-Source ON State Resistance vs Gate-Source Bias

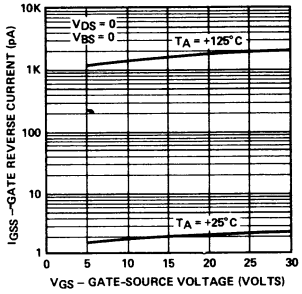


Output Conductance vs Drain Current

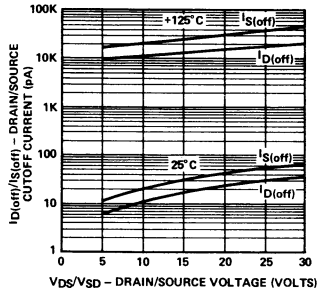


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

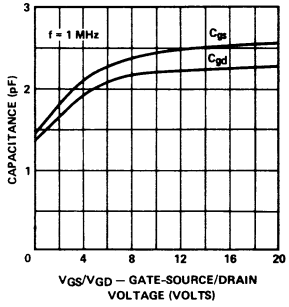
Gate Leakage Current vs Gate-Source Bias



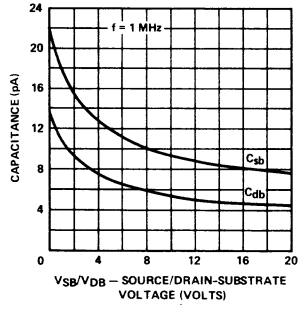
Source-Drain Leakage Currents vs Voltage



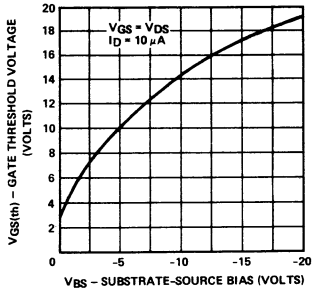
Gate Capacitance vs Voltage



Substrate Capacitance vs Voltage



Gate Threshold Voltage vs Substrate Bias

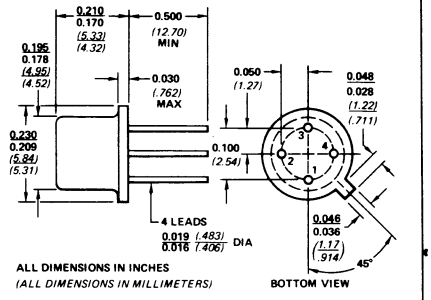


Performance Curves ME
See Page 4-13

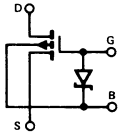
P-CHANNEL ENHANCEMENT-TYPE SILICON MOS FIELD-EFFECT TRANSISTOR

HIGH VOLTAGE MOSFET TRANSISTOR FOR ANALOG AND DIGITAL SWITCHING APPLICATIONS

- Zener Clamp Protects the Gate
- Low Drain-Source ON Resistance
- Very Low $I_{D(off)}$ and $I_{S(off)}$



TO-72



PIN	OUT
1	D
2	G
3	B,C
4	S

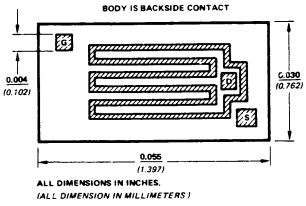
ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Source Voltage	±75 V
Gate-to-Source Voltage	-80 V
Gate-to-Drain Voltage	-80 V
Drain Current	-50 mA
Gate Zener Current	±0.1 mA
Storage Temperature	-65 to +150°C
Operating Junction Temperature	-55 to +125°C
Total Device Dissipation (Derate 2.25 mW/°C to 125°C)	225 mW

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	-75		V	I_D = -1 μA, V_{GS} = V_{BS} = 0	
2		BV_{SDS}	Source-Drain Breakdown Voltage	-75			I_S = -1 μA, V_{DG} = V_{BD} = 0	
3		BV_{GBS}	Gate-Body Breakdown Voltage	-80			I_G = -10 μA, V_{SB} = V_{DB} = 0	
4		I_{GSS}	Gate-Body Leakage		-250	pA	V_{GS} = -50 V, V_{DS} = V_{BS} = 0	
5		$I_{D(off)}$	Drain Cutoff Current		-0.8	nA	V_{DS} = -50 V, V_{GS} = V_{BS} = 0	
6		$I_{S(off)}$	Source Cutoff Current		-0.8		V_{SB} = -50 V, V_{GD} = V_{BD} = 0	
7		$V_{GS(th)}$	Gate Threshold Voltage	-2	-6	V	V_{GS} = V_{DS}, I_D = -10 μA, V_{BS} = 0	
8		$r_{DS(on)}$	Drain-Source ON Resistance		90	Ω	V_{GS} = -80 V, I_D = -100 μA, V_{BS} = 0 V	
9					125		V_{GS} = -60 V, I_D = -100 μA, V_{BS} = 20 V	
10					230		V_{GS} = -40 V, I_D = -100 μA, V_{BS} = 40 V	
11	DYNAMIC	C_{gs} or C_{gd}	Gate-Source or Gate-Drain Capacitance		8	pF	V_{GS} = 0, V_{DS} = 0, V_{BS} = 0 Body Guarded	f = 1 MHz
12		C_{sb}	Source-Body Capacitance		15		V_{GB} = 0, V_{DS} = 0, V_{SB} = -5 V	
13		C_{db}	Drain-Body Capacitance		10			
14		C_{ds}	Drain-Source Capacitance		0.3		V_{GB} = 0, V_{DB} = -5 V, V_{SB} = -5 V Body Guarded	

ME



P-CHANNEL ENHANCEMENT-TYPE SILICON MOS FIELD-EFFECT TRANSISTOR

APPLICATIONS

- Analog and Digital Switching
- Multiplexers

PRINCIPAL DEVICE

M119

PACKAGE TYPE

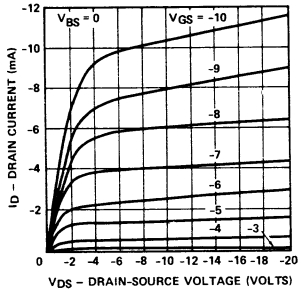
TO-72

FEATURES

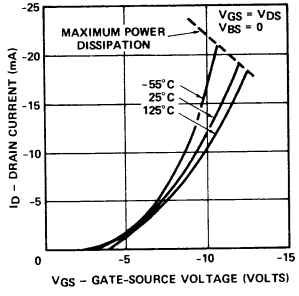
- Integrated Zener Clamp Protects the Gate
- High Voltage Breakdown
- Low $I_{D(off)}$ and $I_{S(off)}$

PERFORMANCE CURVES (25°C unless otherwise noted)

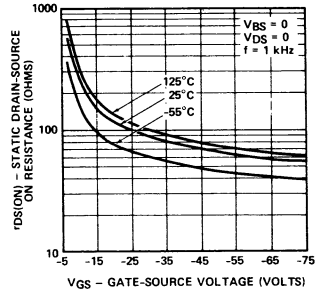
Output Characteristic



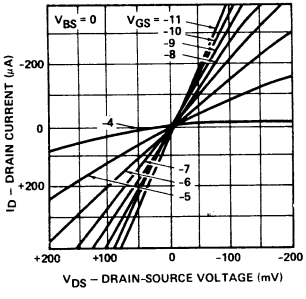
Transfer Characteristics



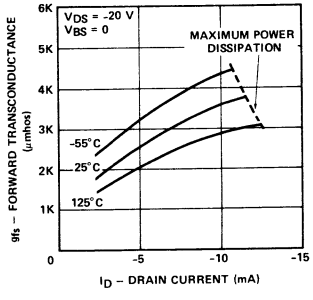
Drain Source ON Resistance vs Gate-Source Bias



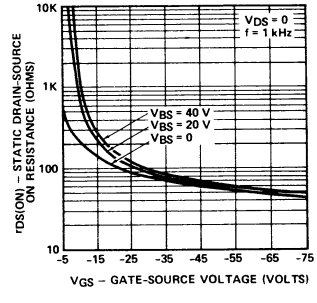
Low Voltage Output Characteristics



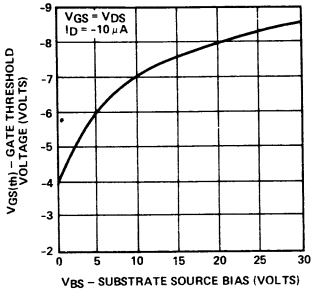
Forward Transconductance vs Drain Current



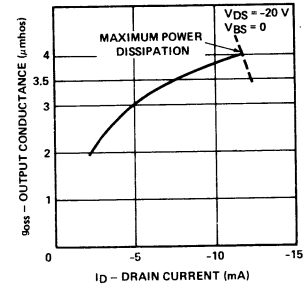
Drain-Source ON Resistance vs Gate-Source Bias



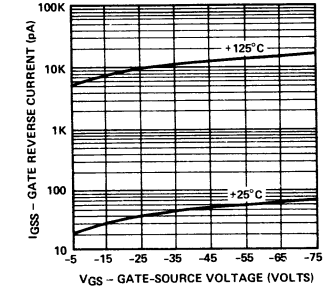
Gate Threshold Voltage vs Substrate Bias



Output Conductance vs Drain Current

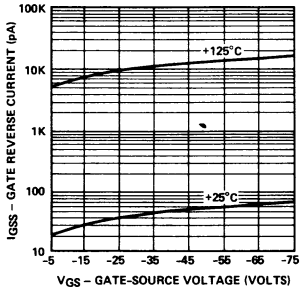


Gate Leakage Current vs Gate-Source Bias

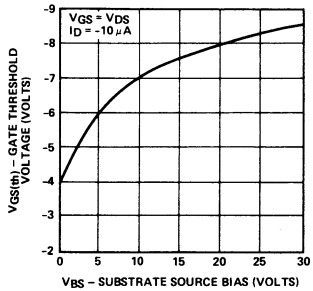


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

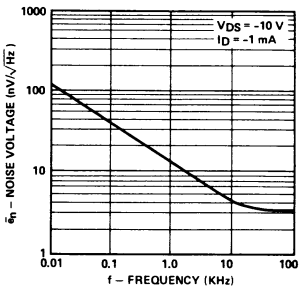
Gate Leakage Current vs Gate-Source Bias



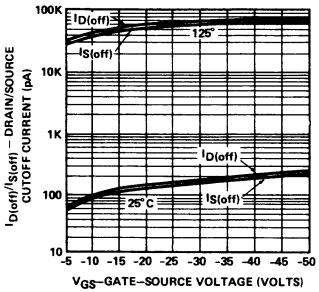
Gate Threshold Voltage vs Substrate Bias



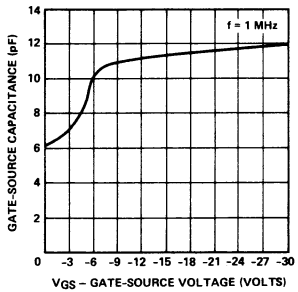
Short Circuit Equivalent Input Noise Voltage vs Frequency



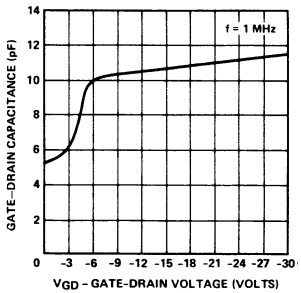
Drain/Source Leakage Currents vs Voltage



Gate-Source Capacitance vs Voltage



Gate-Drain Capacitance vs Voltage

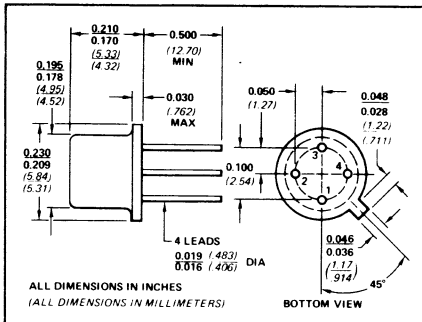


Performance Curves MKA
See Page 4-15

P-CHANNEL ENHANCEMENT-TYPE SILICON MOS FIELD-EFFECT TRANSISTOR

FOR AUDIO & RF AMPLIFIERS, CHOPPER, MULTIPLEX AND COMMUTATING APPLICATIONS

- **Integrated Zener Clamp Protects the Gate**
- **Normally OFF with Zero Gate Voltage**



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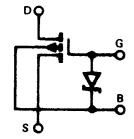


PIN	OUT
1	D
2	G
3	B, C
4	S

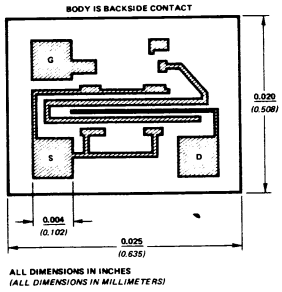
ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Source Voltage	-30 V
Gate-to-Source Voltage	-30 V
Gate-to-Drain Voltage	-30 V
Drain Current	-50 mA
Gate Current (Forward Direction for Zener Clamp)	±0.1 mA
Storage Temperature	-65 to 150°C
Operating Junction Temperature	-55 to 125°C
Total Dissipation at 25°C Ambient Temperature (Derate 2.25 mW/°C)	225 mW

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Leakage Current			-1	nA	V_{GS} = -15 V, V_{DS} = V_{BS} = 0	
2	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	-30			V	I_D = -10 μA, V_{GS} = V_{BS} = 0	
3	STATIC	$V_{GS(th)}$	Gate Threshold Voltage	-3		-6	V	V_{GS} = V_{DS}, I_D = -10 μA, V_{BS} = 0	
4	STATIC	I_{DSS}	Drain Leakage Current		-0.5	-10	nA	V_{DS} = -20 V, V_{GS} = V_{BS} = 0	
5	STATIC	$I_{D(on)}$	Drain Current	-3	-6		mA	V_{GS} = V_{DS} = -10 V, V_{BS} = 0	
6	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance			300	Ω	V_{GS} = -15 V, I_D = -0.1 mA, V_{BS} = 0	
7	DYN	g_{fs}	Common Source Forward Transconductance	1,000			μmho	V_{GS} = V_{DS} = -10 V, V_{BS} = 0	f = 1 kHz
8	DYN	g_{fs}	Common Source Forward Transconductance	1,000			μmho	V_{GS} = V_{DS} = -10 V, V_{BS} = 0	f = 10 MHz
9	DYN	C_{gs}	Gate-Source Capacitance			3	pF	V_{GS} = V_{DS} = -10 V, V_{BS} = 0	f = 1 MHz
10	DYN	C_{gd}	Gate-Drain Capacitance			2.5	pF	V_{GS} = V_{DS} = -10 V, V_{BS} = 0	f = 1 MHz
11	DYN	C_{ds}	Drain-Source Capacitance		0.15		pF	V_{GS} = V_{DS} = -10 V, V_{BS} = 0	f = 1 MHz

MKA



P-CHANNEL ENHANCEMENT-TYPE SILICON MOS FIELD-EFFECT TRANSISTOR

APPLICATIONS

- Audio and RF Amplifiers
- Analog Switches
- Logic Circuits
- Multiplexers

PRINCIPAL DEVICE

MEM511

PACKAGE TYPE

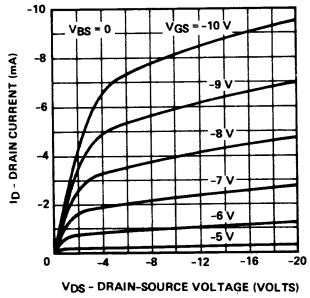
TO-72

FEATURES

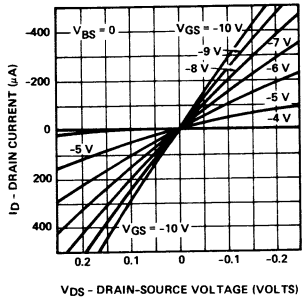
- $10^{10}\ \Omega$ Input Resistance
- Integrated Zener Clamp Protects the Gate
- Square Low Transfer Characteristics
- Normally OFF

PERFORMANCE CURVES (25°C unless otherwise noted)

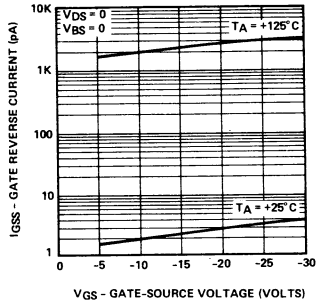
Output Characteristics



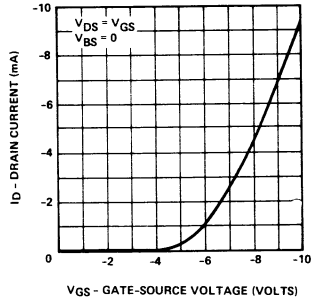
Low Voltage Output Characteristics



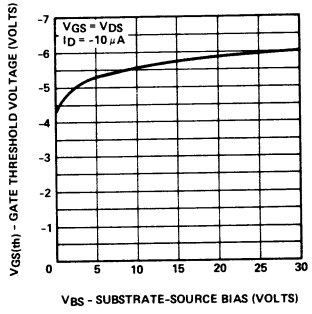
Gate Leakage Current vs Gate-Source Bias



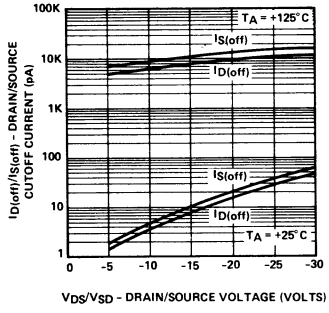
Transfer Characteristic



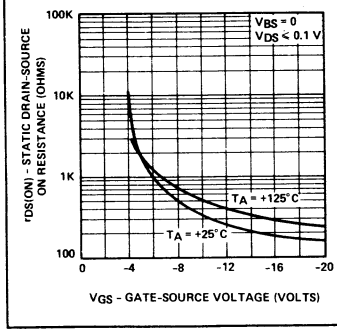
Gate Threshold Voltage vs Substrate Bias



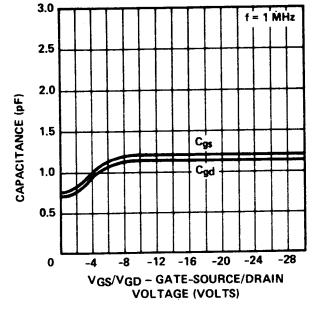
Source-Drain Leakage Currents vs Voltage



Drain-Source ON State Resistance vs Gate-Source Bias



Gate Capacitance vs Voltage



Substrate Capacitance vs Voltage