

N-CHANNEL ENHANCEMENT-MODE HIGH-VOLTAGE D-MOS POWER FETS

ABSOLUTE MAXIMUM RATINGS

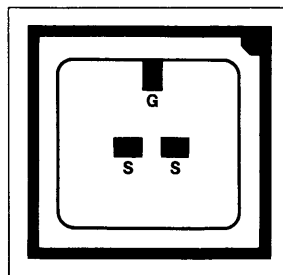
($T_A = +25^\circ\text{C}$ unless otherwise noted)

Drain-Source Voltage	
SD1100	450V
SD1101	400V
Drain-Gate Voltage ($V_{GS} = 0$)	
SD1100	450V
SD1101	400V
Gate-Source Voltage	$\pm 30\text{V}$
Continuous Drain Current	
SD1100DD, SD1101DD	80mA
SD1100HD, SD1101HD	140mA
Peak Drain Current	
SD1100DD, SD1101DD	250mA
SD1100HD, SD1101HD	300mA
Continuous Device Dissipation	
SD1100DD, SD1101DD	360mW
SD1100HD, SD1101HD	800mW
Linear Derating Factor	
SD1100DD, SD1101DD	2.9mW/ $^\circ\text{C}$
SD1100HD, SD1101HD	6.4mW/ $^\circ\text{C}$
Operating Junction Temperature	
Range	-55 to $+150^\circ\text{C}$
Storage Temperature Range	-55 to $+150^\circ\text{C}$
Lead Temperature (1/16" from mounting surface for 30 Sec)	$+260^\circ\text{C}$

ORDERING INFORMATION

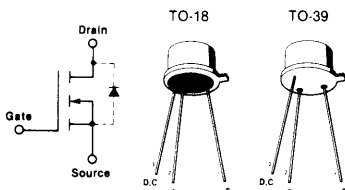
Sorted Chips in Carriers	SD1100CHP	SD1101CHP
TO-18 Package	SD1100DD	SD1101DD
TO-39 Package	SD1100HD	SD1101HD
Description	450V, 35 ohm	400V, 25 ohm

CHIP CONFIGURATION



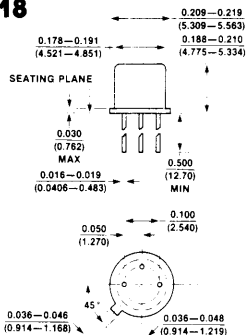
Dimensions: .054 x .056 x .013 inches
Drain is backside contact.

SCHEMATIC DIAGRAM/ PACKAGES



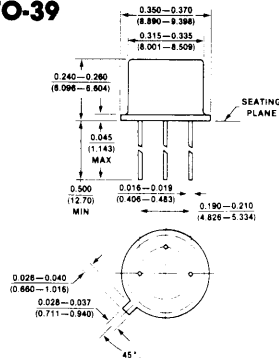
Body Internally connected to Source.
Drain common to Case.

PACKAGE DIMENSIONS TO-18



All dimensions in inches and (millimeters)

PACKAGE DIMENSIONS TO-39



All dimensions in inches and (millimeters)

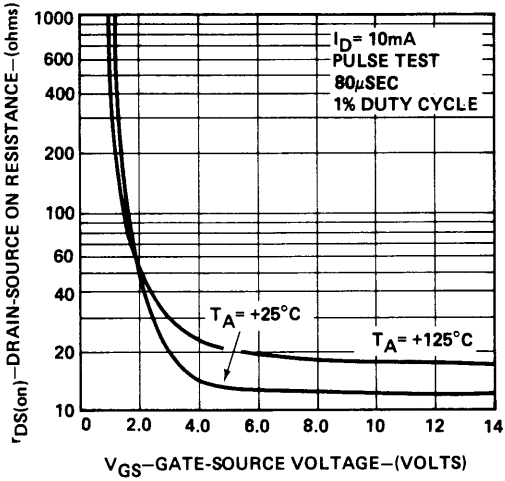
ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

#	CHARACTERISTIC	SD1100			SD1101			UNIT	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
1	BV_{DSS} Drain-Source Breakdown Voltage	450	475		400	425		V	$I_D = 10 \mu\text{A}, V_{GS} = 0$
2	$V_{GS(th)}$ Gate-Source Threshold Voltage	1.0	3.0	5.0	1.0	3.0	5.0	V	$I_D = 10 \mu\text{A}, V_{DS} = V_{GS}$
3	I_{GBS} Gate-Body Leakage Current		.03	1.0		.03	1.0	nA	$V_{GS} = 20\text{V}, V_{DS} = 0$
4	I_{DSS} Drain-Source OFF Leakage Current		2.0	200				nA	$V_{DS} = 360\text{V}, V_{GS} = 0$
5	I_{DSS} Drain-Source OFF Leakage Current					2.0	200	nA	$V_{DS} = 320\text{V}, V_{GS} = 0$
6	$I_{D(on)}$ ON Drain Current	250	400		250	400		mA	$V_{DS} = 25\text{V}, V_{GS} = 15\text{V}$ (Note 1)
7	$r_{DS(on)}$ Drain-Source ON Resistance		25	35		20	25	ohms	$I_D = 10\text{mA}, V_{GS} = 15\text{V}$
8	g_{fs} Common-Source Forward Transconductance		210			210		mmhos	$V_{DS} = 25\text{V}, I_D = 250\text{mA}$ $f = 1\text{KHz}$ (Note 1)
9	C_{iss} Common-Source Input Capacitance		80			80		pF	$V_{DS} = 25\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$
10	C_{rss} Common-Source Reverse Transfer Capacitance		1.3			1.3			
11	C_{oss} Common-Source Output Capacitance		10.5			10.5			

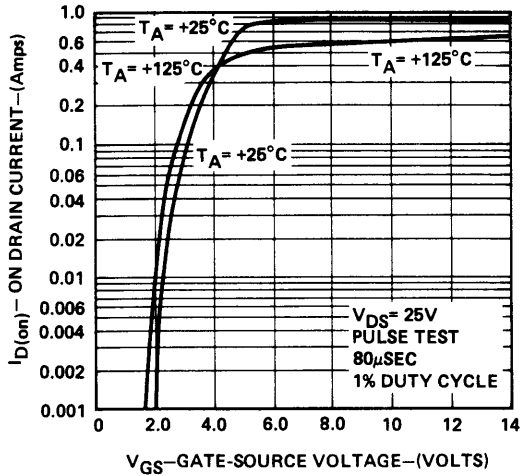
Note 1: Pulse Test 80 μ Sec, 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

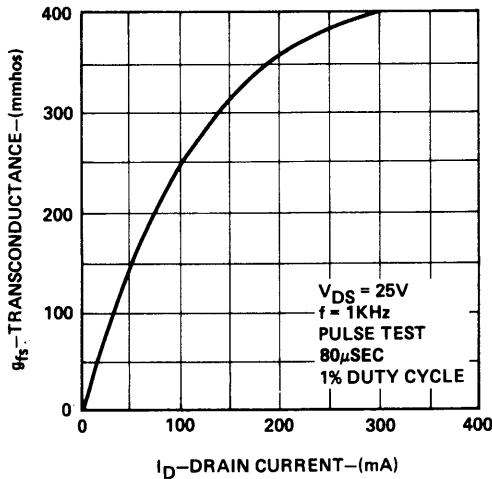
DRAIN-SOURCE ON RESISTANCE
—vs—
GATE-SOURCE VOLTAGE



ON DRAIN CURRENT
—vs—
GATE-SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE
—vs—
ON DRAIN CURRENT



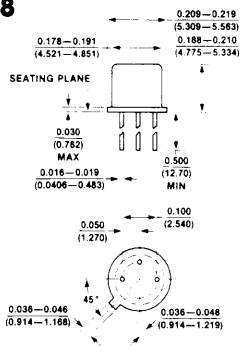
N-CHANNEL ENHANCEMENT-MODE HIGH-VOLTAGE D-MOS POWER FETs

ORDERING INFORMATION

Sorted Chips in Carriers	SD1102CHP	SD1112CHP	SD1113CHP
TO-18 Package	SD1102DD	SD1112DD	SD1113DD
TO-39 Package	SD1102HD	SD1112HD	SD1113HD
TO-92 Package	SD1102BD	SD1112BD	SD1113BD
Description	250V, 10 ohms	200V, 7.0 ohms	200V, 10 ohms

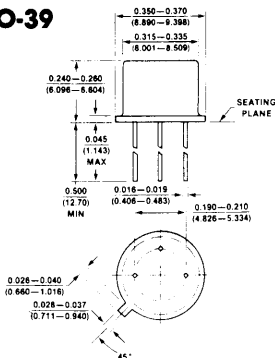
PACKAGE DIMENSIONS

TO-18



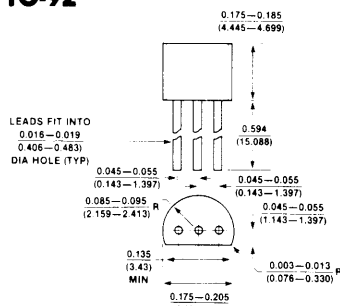
All dimensions in inches and (millimeters)

TO-39



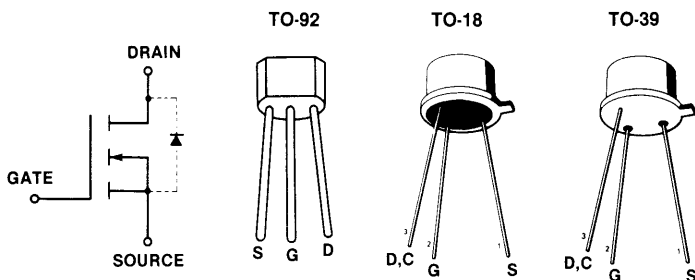
All dimensions in inches and (millimeters)

TO-92

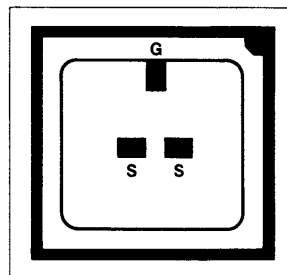


All dimensions in inches and (millimeters)

SCHEMATIC DIAGRAM/PACKAGES



CHIP CONFIGURATION



Dimensions: .054 x .056 x .013 inches
Drain is backside contact.

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Drain-Source Voltage		
SD1102.....	250V	
SD1112, SD1113.....	200V	
Drain-Gate Voltage ($V_{GS} = 0$)		
SD1102.....	250V	
SD1112, SD1113.....	200V	
Gate-Source Voltage.....		$\pm 30\text{V}$
Continuous Drain Current		
	$T_A = 25^\circ\text{C}$	$T_C = 25^\circ\text{C}$
SD1102BD, SD1113BD ..	.13	.23A
SD1112BD ..	.15	.27A
SD1102DD, SD1113DD ..	.14	.31A
SD1112DD ..	.16	.37A
SD1102HD, SD1113HD ..	.23	.57A
SD1112HD ..	.27	.69A
Peak Pulsed Drain Current.....		0.5A

Continuous Device Dissipation

	$T_A = +25^\circ\text{C}$	$T_C = +25^\circ\text{C}$	
SD1102/1112/1113BD ..	0.30	1.0	W
SD1102/1112/1113DD ..	0.36	1.8	W
SD1102/1112/1113HD ..	1.0	6.25	W
Linear Derating Factor			
	$T_A = +25^\circ\text{C}$	$T_C = +25^\circ\text{C}$	
SD1102/1112/1113BD ..	2.4	8.0	mW/°C
SD1102/1112/1113DD ..	2.9	14.4	mW/°C
SD1102/1112/1113HD ..	8.0	50	mW/°C
Operating Junction			
Temperature Range..... -55 to $+150^\circ\text{C}$			
Storage Temperature Range..... -55 to $+150^\circ\text{C}$			
Lead Temperature (1/16" from mounting surface for 30 Sec)..... $+260^\circ\text{C}$			

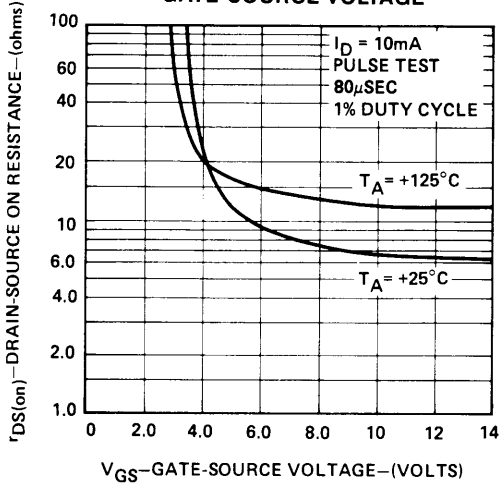
ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

#	CHARACTERISTIC		SD1102			SD1112, SD1113			UNIT	TEST CONDITION	
			MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV _{DSS} Drain-Source Breakdown Voltage	250	270		200	250		V	$I_D = 10\mu\text{A}, V_{GS} = 0$	
2		V _{GS(th)} Gate-Source Threshold Voltage	1.0	3.0	5.0	1.0	3.0	5.0	V	$V_{DS} = V_{GS}, I_D = 10\mu\text{A}$	
3		I _{GBS} Gate-Body Leakage Current		.03	1.0		.03	1.0	nA	$V_{GS} = 20\text{V}, V_{DS} = 0$	
4		I _{DSS} Drain-Source OFF Leakage Current		0.1	1.0				μA	$V_{DS} = 200\text{V}$	
5							0.1	1.0		$V_{DS} = 160\text{V}$	
6		I _{D(on)} ON Drain Current	0.5			0.5			A	$V_{DS} = 25\text{V}, V_{GS} = 15\text{V}$ (Note 1)	
7		r _{DS(on)} Static Drain-Source ON Resistance	SD1102		8.0	10			ohms	$I_D = 10\text{mA}, V_{GS} = 15\text{V}$ (Note 1)	
8			SD1112				6.0	7.0			
9			SD1113					7.0			10
10		DYNAMIC	g _{fs} Common-Source Forward Transcond.		300			300		mmhos	$V_{DS} = 25\text{V}, I_D = 0.5\text{A}$ $f = 1\text{KHz}$ (Note 1)
11			c _{iss} Common-Source Input Capacitance		80			80		pF	$V_{DS} = 25\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$
12			C _{rSS} Common-Source Reverse Transfer Capacitance		1.3			1.3			
13			c _{oss} Common-Source Output Capacitance		10.5			10.5			

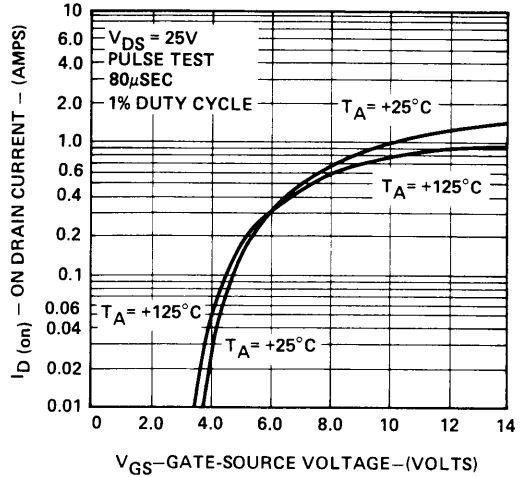
Note 1: Pulse Test 80 μSec , 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

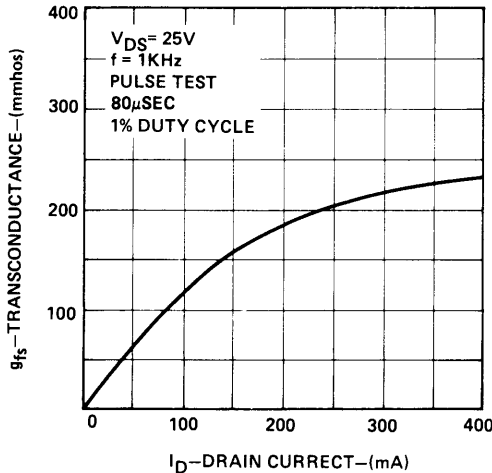
DRAIN-SOURCE ON RESISTANCE
—vs—
GATE-SOURCE VOLTAGE



ON DRAIN CURRENT
—vs—
GATE-SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE
—vs—
ON DRAIN CURRENT



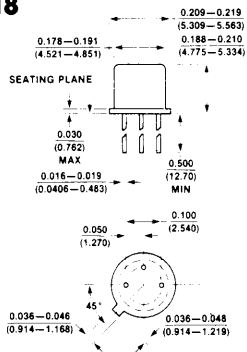
N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION

Sorted Chips in Carriers	SD1104CHP	SD1105CHP	SD1114CHP	SD1115CHP
TO-18 Package	SD1104DD	SD1105DD	SD1114DD	SD1115DD
TO-39 Package	SD1104HD	SD1105HD	SD1114HD	SD1115HD
TO-92 Package	SD1104BD	SD1105BD	SD1114BD	SD1115BD
Description	100V, 3.0 ohms	100V, 4.0 ohms	80V, 3.0 ohms	80V, 4.0 ohms

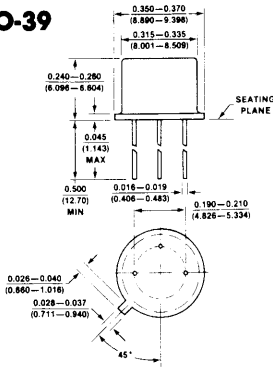
PACKAGE DIMENSIONS

TO-18



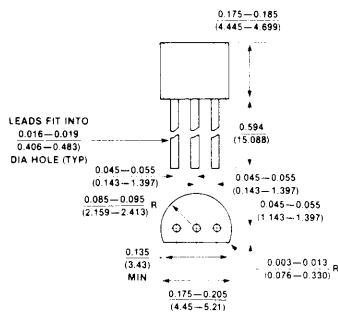
All dimensions in inches and (millimeters)

TO-39



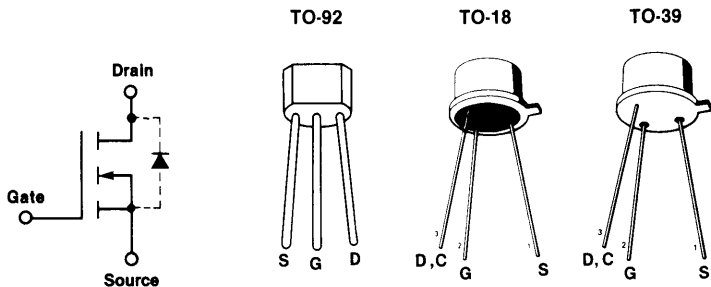
All dimensions in inches and (millimeters)

TO-92

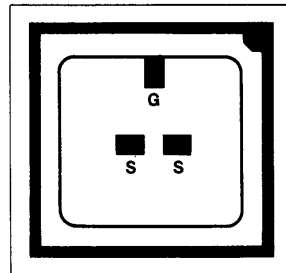


All dimensions in inches and (millimeters)

SCHEMATIC DIAGRAM/PACKAGES



CHIP CONFIGURATION



Dimensions: .054 x .056 x .013 inches
Drain is backside contact.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Drain-Source Voltage	SD1104, SD1105..... 100V	SD1114, SD1115..... 80V	Peak Pulsed Drain Current..... 2.0A
Drain-Gate Voltage (V _{GS} = 0)	SD1104, SD1105..... 100V	SD1114, SD1115..... 80V	Continuous Device Dissipation
Gate-Source Voltage..... ±30V			T _A = +25°C T _C = +25°C
Continuous Drain Current			SD1104/1105/1114/1115BD 0.30 1.0 W
	T _A = 25°C T _C = 25°C		SD1104/1105/1114/1115DD 0.36 1.8 W
SD1104BD, SD1114BD .23 .42A			SD1104/1105/1114/1115HD 1.0 6.25 W
SD1105BD, SD1115BD .20 .36A			Linear Derating Factor
SD1104DD, SD1114DD .25 .56A			T _A = +25°C T _C = +25°C
SD1105DD, SD1115DD .22 .49A			SD1104/1105/1114/1115BD 2.4 8.0 mW/°C
SD1104HD, SD1114HD .42 1.05A			SD1104/1105/1114/1115DD 2.0 14.4 mW/°C
SD1105HD, SD1115HD .36 .91A			SD1104/1105/1114/1115HD 8.0 50 mW/°C
			Operating Junction
			Temperature Range..... -55 to +150°C
			Storage Temperature Range..... -55 to +150°C
			Lead Temperature (1/16" from mounting surface for 30 Sec)..... +260°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#	CHARACTERISTIC		SD1104, SD1105			SD1114, SD1115			UNIT	TEST CONDITION
			MIN	TYP	MAX	MIN	TYP	MAX		
1	STATIC	BV _{DSS} Drain-Source Breakdown Voltage	100			80			V	I _D = 100μA, V _{GS} = 0
2		V _{GS(th)} Gate-Source Threshold Voltage	1.0	2.4	5.0	1.0	2.4	5.0	V	V _{DS} = V _{GS} , I _D = 1mA
3		I _{GBS} Gate-Body Leakage Current		.03	1.0		.03	1.0	nA	V _{GS} = 20V, V _{DS} = 0
4		I _{DSS} Drain-Source OFF Leakage Current		0.1	10				μA	V _{DS} = 80V
5		I _{DSS} Drain-Source OFF Leakage Current					0.1	10		V _{DS} = 64V
6		I _{D(on)} ON Drain Current		2.0			2.0		A	V _{DS} = 25V, V _{GS} = 15V (Note 1)
7		r _{DS(on)} Static Drain-Source ON Resistance	SD1104			3.0			ohms	I _D = 100mA, V _{GS} = 15V (Note 1)
8			SD1105			4.0				
9			SD1114					3.0		
10			SD1115					4.0		
11	DYNAMIC	g _{fs} Common-Source Forward Transcond.		500			500	mmhos	V _{DS} = 25V, I _D = 1.0A f = 1KHz (Note 1)	
12		c _{iss} Common-Source Input Capacitance		80			80	pF	V _{DS} = 25V, V _{GS} = 0 f = 1MHz	
13		c _{rss} Common-Source Reverse Transfer Capacitance		1.3			1.3			
14		c _{oss} Common-Source Output Capacitance		10.5			10.5			
15		t _{on} Turn-On Time		4.0			4.0	nSec	V _{DD} = 25V R _L = 20 ohms R _G = 50 ohms V _{GS} = 10V	
16		t _{off} Turn-off Time		4.0			4.0			

Note 1: Pulse Test 80μSec, 1% Duty Cycle

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

FEATURES

- Inherent Current Sharing Capability when Paralleled
- Simple Straight-Forward DC Biasing
- Extended Safe Operating Area
- Inherently Temperature Stable—
Output Current Decreases as Temperature Increases

APPLICATIONS

- High-Speed Pulse Amplifiers
- Logic Buffers
- Line Drivers
- Solid-State Relays

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Drain-Source Voltage	60V
Drain-Gate Voltage (V _{GS} = 0)	60V
Gate-Source Voltage	±30V
Continuous Drain Current (Note 1, Note 2) .	0.5A
Peak Drain Current (Note 1, Note 2)	2.0A
Continuous Device Dissipation (Note 1, Note 2)	1.8W
Linear Derating Factor (Note 1, Note 2)	14.4mW/°C
Operating Junction Temperature Range	-55 to +150°C
Storage Temperature Range	-55 to +150°C
Lead Temperature (1/16" from mounting surface for 30 Sec)	+260°C

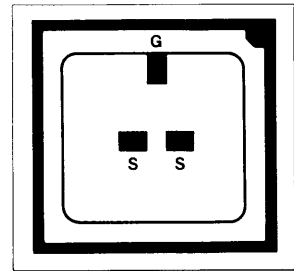
Note 1: T_{Case} = +25°C

Note 2: Not applicable to chips. Final value depends upon mounting substrate.

ORDERING INFORMATION

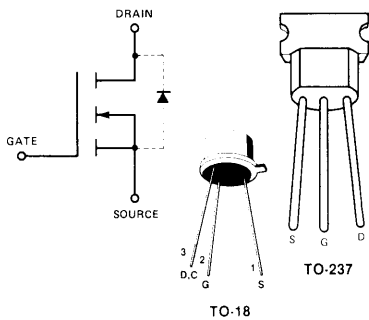
Sorted Chips in Carriers	SD1106CHP
TO-18 Package	SD1106DD
TO-237 Package	SD1106AD

CHIP CONFIGURATION



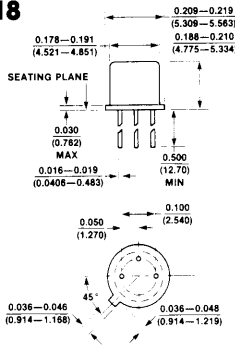
Dimensions: .054 x .056 x .013 inches
Drain is backside contact.

SCHEMATIC DIAGRAM



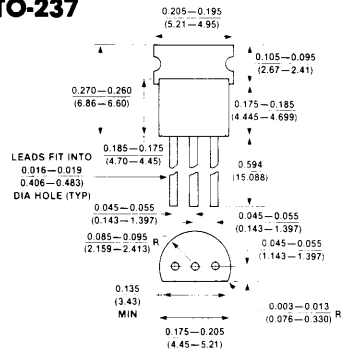
Drain common to Case or Tab.

PACKAGE DIMENSIONS TO-18



All dimensions in inches and (millimeters)

PACKAGE DIMENSIONS TO-237



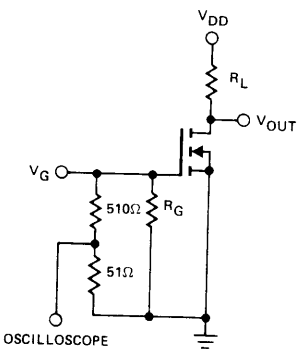
All dimensions in inches and (millimeters)

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

#	CHARACTERISTIC	SD1106			UNIT	TEST CONDITION
		MIN	TYP	MAX		
1	BV _{DSS} Drain-Source Breakdown Voltage	60			V	$I_D = 100\mu\text{A}, V_{GS} = 0$
2	V _{GS(th)} Gate-Source Threshold Voltage	0.8	2.5		V	$V_{DS} = V_{GS}, I_D = 1\text{mA}$
3	I _{GBS} Gate-Body Leakage Current		.03	10	nA	$V_{GS} = 20\text{V}, V_{DS} = 0$
4	I _{DSS} Drain-Source OFF Leakage Current		.01	10	μA	$V_{DS} = 40\text{V}, V_{GS} = 0$
5	I _{D(on)} ON Drain Current	0.25			A	$V_{DS} = 25\text{V}$ Note 1
6		0.50				
7	V _{DS(on)} Drain-Source ON Voltage		1.8	2.5	V	$V_{GS} = 10\text{V}, I_D = 0.5\text{A}$ Note 1
8	g _{fs} Common-Source Forward Transcond.	100	270		mmhos	$V_{DS} = 15\text{V}, I_D = 0.5\text{A}$ $f = 1\text{KHz}$ Note 1
9	C _{iss} Common-Source Input Capacitance		80		pF	$V_{DS} = 25\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$
10	C _{rss} Common-Source Reverse Transfer Capacitance		1.3			
11	C _{oss} Common-Source Output Capacitance		10.5			
12	t _{on} Turn-On Time		4.0	6.0		
13	t _{off} Turn-Off Time		4.0	6.0	nSec	$V_{DD} = 25\text{V}$ $R_L = 25\text{ ohms}$ $R_G = 51\text{ ohms}$ $V_{G(on)} = 10\text{V}$

Note 1: Pulse Test 80 μSec , 1% Duty Cycle

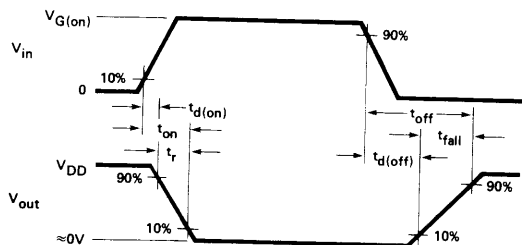
SWITCHING TIMES TEST CIRCUIT



INPUT PULSE
 $t_r \leq 0.5\text{ nSEC}$
 PULSE WIDTH - 100 nSEC

SAMPLING OSCILLOSCOPE
 $t_r < 0.36\text{ nSEC}$
 $R_{in} > 1\text{M}\Omega$
 $C_{in} < 2.0\text{ pF}$

TEST WAVEFORMS



N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

FEATURES

- Inherent Current Sharing Capability when Paralleled
- Simple Straight-Forward DC Biasing
- Extended Safe Operating Area
- Inherently Temperature Stable — Output Current Decreases as Temperature Increases

APPLICATIONS

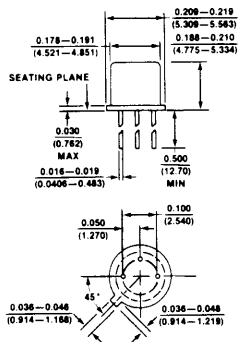
- High-Speed Pulse Amplifiers
- CMOS Logic to High-Current Interfaces
- High-Speed Switching
- Line Drivers

ORDERING INFORMATION

Sorted Chips in Carriers	SD1107CHP	SD1117CHP
TO-18 Package	SD1107DD	SD1117DD
TO-39 Package	SD1107HD	SD1117HD
TO-92 Package	SD1107BD	SD1117BD
Description	100V, 4.0 ohm	60V, 2.5 ohm

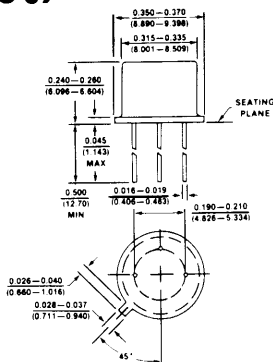
PACKAGE DIMENSIONS

TO-18



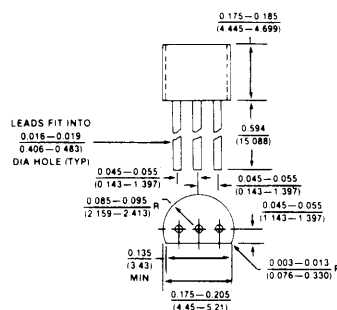
All dimensions in inches and (millimeters)

TO-39



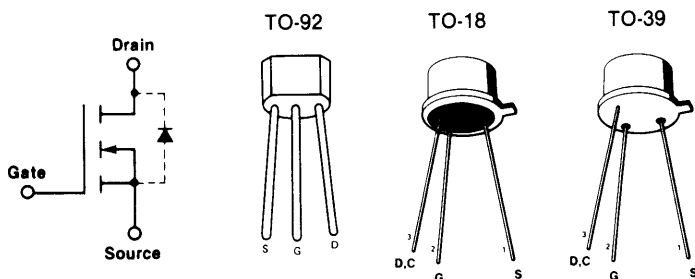
All dimensions in inches and (millimeters)

TO-92

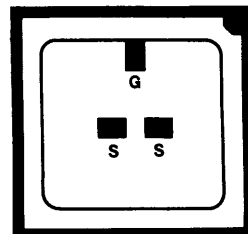


All dimensions in inches and (millimeters)

SCHEMATIC DIAGRAM/PACKAGES



CHIP CONFIGURATION



Dimensions: .054 x .058 x .013 inches
Drain is backside contact.

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Drain-Source Voltage			Continuous Device Dissipation		
SD1107	100V		$T_A = +25^\circ\text{C}$		$T_C = +25^\circ\text{C}$
SD1117	60V		SD1107BD, SD1117BD	0.30	1.0 W
Drain-Gate Voltage ($V_{GS} = 0$)			SD1107DD, SD1117DD	0.36	1.8 W
SD1107	100V		SD1107HD, SD1117HD	1.0	6.25 W
SD1117	60V		Linear Derating Factor		
Gate-Source Voltage	$\pm 30\text{V}$		$T_A = +25^\circ\text{C}$		$T_C = +25^\circ\text{C}$
Continuous Drain Current	$T_A = 25^\circ\text{C}$ $T_C = 25^\circ\text{C}$		SD1107BD, SD1117BD	2.4	8.0 mW/ $^\circ\text{C}$
			SD1107DD, SD1117DD	2.9	14.4 mW/ $^\circ\text{C}$
			SD1107HD, SD1117HD	8.0	50 mW/ $^\circ\text{C}$
SD1107BD	.20	.36 A	Operating Junction		
SD1107DD	.22	.49 A	Temperature Range		
SD1107HD	.36	.91 A	Storage Temperature Range		
SD1117BD	.25	.46 A	Lead Temperature (1/16" from mounting		
SD1117DD	.28	.62 A	surface for 30 Sec)		
SD1117HD	.46	1.15 A	+260 $^\circ\text{C}$		
Peak Pulsed Drain Current	2.0A				

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

#	CHARACTERISTIC	SD1107			SD1117			UNIT	TEST CONDITION	
		MIN	TYP	MAX	MIN	TYP	MAX			
1	BV _{DSS} Drain-Source Breakdown Voltage	100	140		60	90		V	$I_D = 10\mu\text{A}, V_{GS} = 0$	
2	V _{GS(th)} Gate-Source Threshold Voltage	0.8		2.0	0.8		2.0	V	$V_{DS} = V_{GS}, I_D = 1\text{mA}$	
3	I _{GBS} Gate-Body Leakage Current		.03	1.0		.03	1.0	nA	$V_{GS} = 20\text{V}, V_{DS} = 0$	
4				10			10		$T_A = +125^\circ\text{C}$	
5		I _{DSS} Drain-Source OFF Leakage Current		0.1	1.0				μA	$V_{DS} = 80\text{V}, V_{GS} = 0$
6					50					$T_A = +125^\circ\text{C}$
7						0.1	1.0		$V_{DS} = 48\text{V}, V_{GS} = 0$	
8						50			$T_A = +125^\circ\text{C}$	
9	I _{D(on)} ON Drain Current	2.0	3.0		2.0	3.5		A	$V_{DS} = 25\text{V}, V_{GS} = 10\text{V}$ (Note 1)	
10	r _{DS(on)} Drain-Source ON Resistance		3.2	5.0		2.3	4.5	ohms	$V_{GS} = 5\text{V}, I_D = 0.3\text{A}$ (Note 1)	
11				2.9	4.0		2.0	2.5		$V_{GS} = 10\text{V}, I_D = 1.0\text{A}$ (Note 1)
12	g _{fs} Common-Source Forward Transcond.		500			500		mmhos	$V_{DS} = 25\text{V}, I_D = 1.0\text{A}$ $f = 1\text{KHz}$ (Note 1)	
13	c _{iss} Common-Source Input Capacitance		80			80		pF	$V_{DS} = 25\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$	
14	c _{rss} Common-Source Reverse Transfer Capacitance		1.3			1.3				
15	c _{oss} Common-Source Output Capacitance		10.5			10.5				
16	t _{on} Turn-On Time		4.0	6.0		4.0	6.0	nSec	$V_{DD} = 25\text{V}$ $R_L = 25\text{ohms}$ $R_G = 51\text{ohms}$ $V_{G(on)} = 10\text{V}$	
17	t _{off} Turn-Off Time		4.0	6.0		4.0	6.0			

Note 1: Pulse Test 80 μSec , 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

