TOPAZ SEMICONDUCTOR

SD1122

N-CHANNEL ENHANCEMENT-MODE HIGH-VOLTAGE D-MOS POWER FETS

FEATURES

- Inherent Current Sharing Capability when Paralleled
- Simple Straight-Forward DC Biasing
- Extended Safe Operating Area
- Inherently Temperature Stable — Output Current Decreases as Temperature Increases

APPLICATIONS

- High-Speed Pulse Amplifiers
- Logic Buffers
- Line Drivers
- Line Interrupters
- Outpulser Switches
- Display Drivers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Drain-Source Voltage	200V
Drain-Gate Voltage (V_{GS} = 0)	200V
Gate-Source Voltage	±30V
Continuous Device Dissipation (Note 2)	0.3W
Linear Derating Factor (Note 2)	2.4mW/°C
Continuous Drain Current (Note 2)	0.12A
Peak Drain Current (Note 1, Note 2)	0.5A
Continuous Device Dissipation (Note 1, Note 2)	1.0W
Linear Derating Factor (Note 1, Note 2)	8.0mW/°C
Thermal Resistance, Junction to case	125°C/W
Operating Junction Temperature Range	−55 to +150°C
Storage Temperature Range	−55 to +150°C
Lead Temperature (1/16″ from mounting surface for 30 Sec)	+260°C

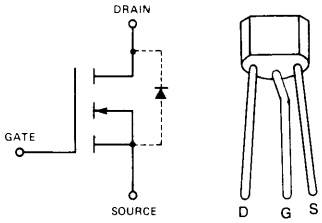
Note 1: T_{CASE} = +25°C

Note 2: Not applicable to chips. Final value depends upon mounting substrate.

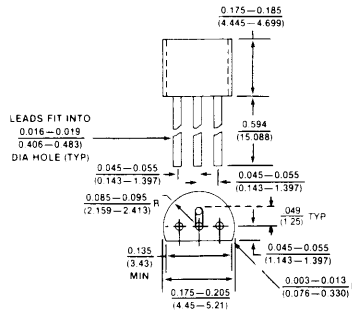
ORDERING INFORMATION

Sorted Chips in Carriers	SD1122CHP
TO-92 Pkg-Lead Formed	SD1122BD
Description	200V, 10 ohms

SCHEMATIC DIAGRAM



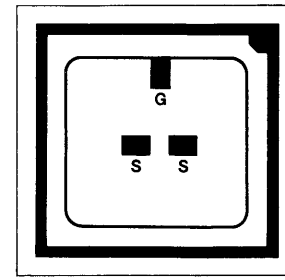
PACKAGE DIMENSIONS TO-92, LEAD FORMED



Lead-formed to TO-18 pin circle.

All dimensions in inches and (millimeters)

CHIP CONFIGURATION



Dimensions: .054 x .056 x .013 inches

Drain is backside contact.

Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

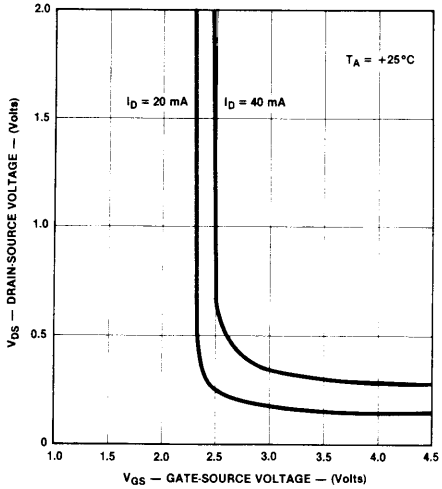
ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		CHARACTERISTIC		SD1122 MIN	SD1122 TYP	SD1122 MAX	UNITS	TEST CONDITIONS
1	STATIC	B_{VDSS}	Drain Source Breakdown Voltage	200	270		V	I_D = 10μA, V_{GS} = 0
2	STATIC	$V_{GS(th)}$	Gate Source Threshold Voltage	0.8	1.9	2.4	V	V_{DS} = V_{GS}, I_D = 1mA
3	STATIC	I_{GBS}	Gate-Body Leakage Current		.03	1.0	nA	V_{GS} = 20V, V_{DS} = 0
4	STATIC	I_{DSX}	Drain-Source OFF Leakage Current		0.1	1.0	μA	V_{DS} = 70V, V_{GS} = 0.2V
5	STATIC	I_{DSS}				30	nA	V_{DS} = 130V, V_{GS} = 0
6	STATIC	$I_{D(on)}$	ON Drain Current	0.5			A	V_{DS} = 25V, V_{GS} = 15V (Note 1)
7	STATIC	$r_{DS(on)}$	Static Drain-Source ON Resistance		7.5	10	ohms	I_D = 120mA (Note 1), V_{GS} = 5.0V
8	STATIC	$r_{DS(on)}$			11	28	ohms	I_D = 20mA, V_{GS} = 2.6V
9	DYNAMIC	g_{fs}	Common-Source Forward Transcond.		300		mmhos	V_{DS} = 25V, I_D = 0.5A f = 1KHz (Note 1)
10	DYNAMIC	C_{iss}	Common-Source Input Capacitance		80		pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz
11	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		1.3		pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz
12	DYNAMIC	C_{oss}	Common-Source Output Capacitance		10.5		pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz

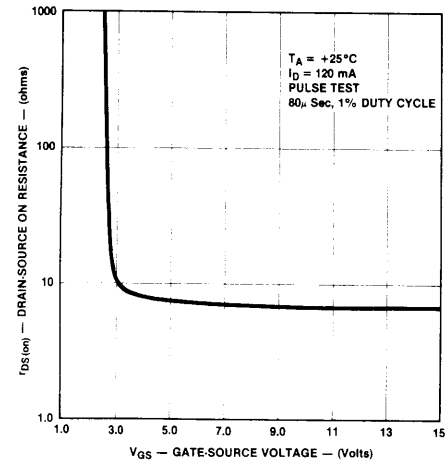
Note 1: Pulse Test 80μSec, 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS

DRAIN-SOURCE ON VOLTAGE — VS — GATE-SOURCE VOLTAGE



DRAIN-SOURCE ON RESISTANCE — VS — GATE-SOURCE VOLTAGE



TOPAZ SEMICONDUCTOR

SD1124

N-CHANNEL ENHANCEMENT-MODE HIGH-VOLTAGE D-MOS POWER FETs

FEATURES

- Inherent Current Sharing Capability when Paralleled
- Simple Straight-Forward DC Biasing
- Extended Safe Operating Area
- Inherently Temperature Stable — Output Current Decreases as Temperature Increases

APPLICATIONS

- High-Speed Pulse Amplifiers
- Logic Buffers
- Line Drivers
- Analog Switches
- Motor Controls
- Power Supplies

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Drain-Source Voltage	60V
Drain-Gate Voltage (V_{GS} = 0)	60V
Gate-Source Voltage	±30V
Continuous Device Dissipation (Note 2)	0.3W
Linear Derating Factor (Note 2)	2.4mW/°C
Continuous Drain Current (Note 2)	0.2A
Peak Drain Current (Note 1, Note 2)	1.0A
Continuous Device Dissipation (Note 1, Note 2)	1.0W
Linear Derating Factor (Note 1, Note 2)	8.0mW/°C
Thermal Resistance, Junction to case	125°C/W
Operating Junction Temperature Range	−55 to +150°C
Storage Temperature Range	−55 to +150°C
Lead Temperature (1/6″ from mounting surface for 30 Sec)	+260°C

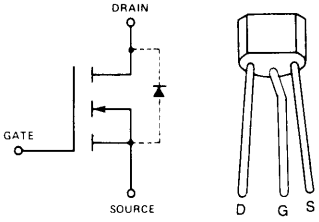
Note 1: T_{CASE} = +25°C

Note 2: Not applicable to chips. Final value depends upon mounting substrate.

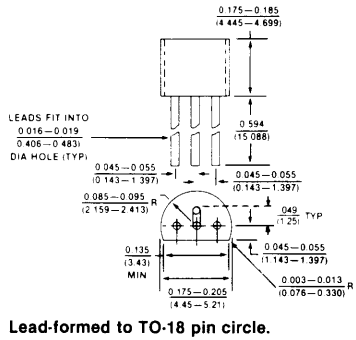
ORDERING INFORMATION

Sorted Chips in Carriers	SD1124CHP
TO-92 Pkg-Lead Formed	SD1124BD
Description	60V, 5 ohms

SCHEMATIC DIAGRAM

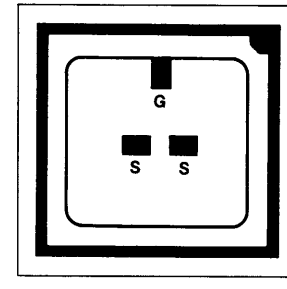


PACKAGE DIMENSIONS TO-92, LEAD FORMED



Lead-formed to TO-18 pin circle.
All dimensions in inches and (millimeters)

CHIP CONFIGURATION



Dimensions: .054 x .056 x .013 inches
Drain is backside contact.

Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

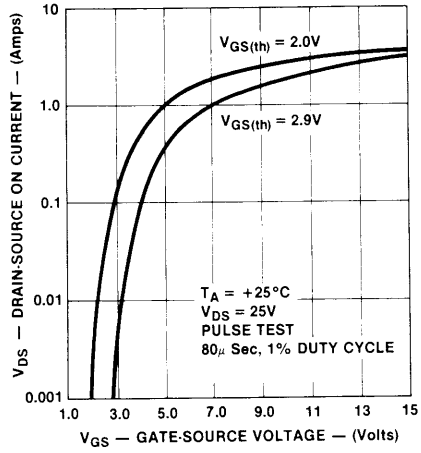
ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		CHARACTERISTIC		SD1124 MIN	SD1124 TYP	SD1124 MAX	UNITS	TEST CONDITIONS
1	STATIC	BV_{DSS}	Drain Source Breakdown Voltage	60	100		V	I_D = 10μA, V_{GS} = 0
2	STATIC	$V_{GS(th)}$	Gate Source Threshold Voltage	0.8	2.1	3.0	V	V_{DS} = V_{GS}, I_D = 1mA
3	STATIC	I_{GBS}	Gate-Body Leakage Current		.03	1.0	nA	V_{GS} = 20V, V_{DS} = 0
4	STATIC	I_{DS}	Drain-Source OFF Leakage Current		0.1	1.0	μA	V_{DS} = 48V, V_{GS} = 0
5	STATIC	I_{DSS}				0.5	μA	V_{DS} = 25V, V_{GS} = 0
6	STATIC	$I_{D(on)}$	ON Drain Current	1.0			A	V_{DS} = 25V, V_{GS} = 15V (Note 1)
7	STATIC	$r_{DS(on)}$	Static Drain-Source ON Resistance		2.8	5.0	ohms	I_D = 200mA, V_{GS} = 10V (Note 1)
8	DYNAMIC	g_{fs}	Common-Source Forward Transcond.		300		mmhos	V_{DS} = 25V, I_D = 0.2A f = 1KHz (Note 1)
9	DYNAMIC	c_{iss}	Common-Source Input Capacitance		80		pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz
10	DYNAMIC	c_{rss}	Common-Source Reverse Transfer Capacitance		1.3		pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz
11	DYNAMIC	c_{oss}	Common-Source Output Capacitance		10.5		pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz
12	DYNAMIC	t_{on}	Turn ON Time		2.0	5.0	nSec	V_{DD} = 25V, $I_{D(on)}$ = 0.2A R_L = 23Ω, R_G = 51Ω
13	DYNAMIC	t_{off}	Turn OFF Time		2.0	5.0	nSec	V_{DD} = 25V, $I_{D(on)}$ = 0.2A R_L = 23Ω, R_G = 51Ω

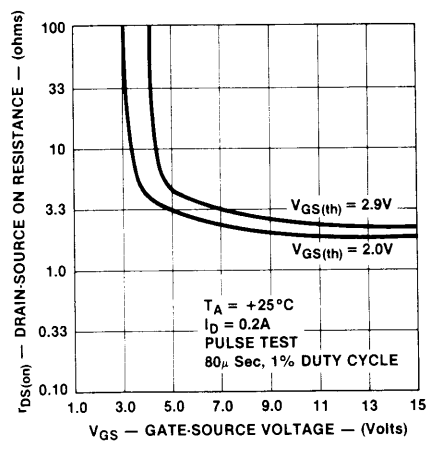
Note 1: Pulse Test 80μSec, 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS

DRAIN-SOURCE ON CURRENT — VS — GATE-SOURCE VOLTAGE



DRAIN-SOURCE ON RESISTANCE — VS — GATE-SOURCE VOLTAGE



TOPAZ SEMICONDUCTOR

SD1127

N-CHANNEL ENHANCEMENT-MODE VERTICAL D-MOS FET ULTRA LOW-LEAKAGE

FEATURES

- Drain-Source Leakage (I_{DSS}), 1.0nA max
- Low Output and Transfer Capacitances
- Extended Safe Operating Area

APPLICATIONS

- High-Speed Switches
- Low-Leakage Solid State Relays
- High-Speed Pulse Amplifiers
- Logic Interfaces
- Line Drivers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Drain-Source Voltage ..... +60V
Drain-Gate Voltage (V_{GS} = 0) ..... +60V
Gate-Source Voltage ..... ±30V
Continuous Drain Current

	T_A = +25°C	T_C = +25°C
SD1127BD	.20A	.36A

Peak Pulsed Drain Current 2.0A

Continuous Device Dissipation

	T_A = +25°C	T_C = +25°C
SD1127BD	0.30W	1.0W

Linear Derating Factor

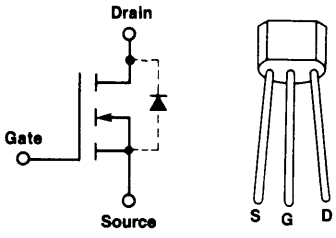
	T_A = +25°C	T_C = +25°C
SD1127BD	3.0mW/°C	10mW/°C

Operating Junction and Storage Temperature Range
-55°C to +150°C
Lead Temperature (1/16" from mounting surface for 30 sec.) ..... +260°C

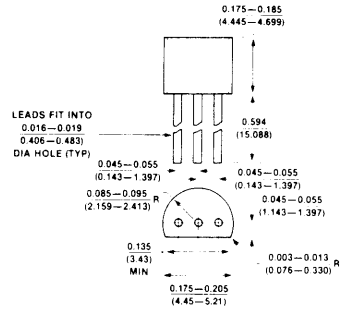
ORDERING INFORMATION

TO-92 Plastic Package	SD1127BD
Sorted Chips in Waffle Pack	SD1127CHP
Description	60 Volt, 4.0 ohm

PIN CONFIGURATION

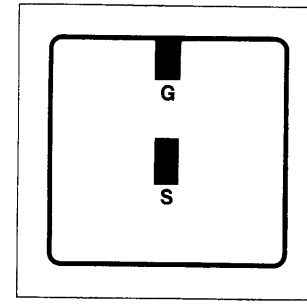


PACKAGE DIMENSIONS TO-92



All dimensions in inches and (millimeters)

CHIP CONFIGURATION



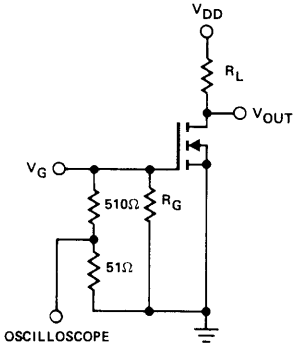
Dimensions: .0445 x .0460 x .013 inches
Drain is backside contact.

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		CHARACTERISTIC		SD1127 MIN	SD1127 TYP	SD1127 MAX	UNIT	TEST CONDITION
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	60	90		V	I_D = 10μA, V_{GS} = 0
2	STATIC	$V_{GS(th)}$	Gate-Source Threshold Voltage	0.8		2.4	V	V_{DS} = V_{GS}, I_D = 1mA
3	STATIC	I_{GBS}	Gate-Body Leakage Current		.03	1.0	nA	V_{GS} = 20V, V_{DS} = 0
4	STATIC					10		T_A = +125°C
5	STATIC	I_{DSS}	Drain-Source OFF Leakage Current			1.0	nA	V_{DS} = 30V, V_{GS} = 0
6	STATIC					100		T_A = +125°C
7	STATIC	$I_{D(on)}$	ON Drain Current	2.0	3.5		A	V_{DS} = 25V, V_{GS} = 10V (Note 1)
8	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance		3.2	5.0	ohms	V_{GS} = 5V, I_D = 0.3A (Note 1)
9	STATIC				2.9	4.0		V_{GS} = 10V, I_D = 1.0A (Note 1)
10	DYNAMIC	g_{fs}	Common-Source Forward Transcond.	250	500		mmhos	V_{DS} = 25V, I_D = 1.0A f = 1KHz (Note 1)
11	DYNAMIC	C_{iss}	Common-Source Input Capacitance		80		pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz
12	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz
13	DYNAMIC	C_{oss}	Common-Source Output Capacitance		15		pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz
14	DYNAMIC	t_{on}	Turn-On Time		4.0	6.0	nSec	V_{DD} = 25V, R_L = 25 ohms, R_G = 51 ohms, $V_{G(on)}$ = 10V
15	DYNAMIC	t_{off}	Turn-Off Time		4.0	6.0	nSec	V_{DD} = 25V, R_L = 25 ohms, R_G = 51 ohms, $V_{G(on)}$ = 10V

Note 1: Pulse Test 80μSec, 1% Duty Cycle

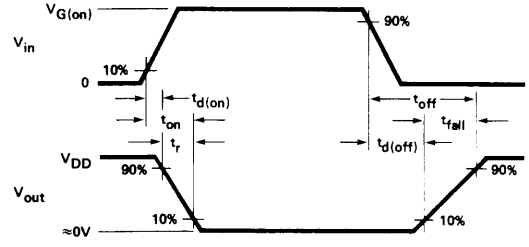
SWITCHING TIMES TEST CIRCUIT



INPUT PULSE
$t_r \leq 0.5$ nSEC
PULSE WIDTH – 100 nSEC

SAMPLING OSCILLOSCOPE
$t_r < 0.36$ nSEC
$R_{in} > 1M\Omega$
$C_{in} < 2.0$ pF

TEST WAVEFORMS



TOPAZ SEMICONDUCTOR

SD1137, TN0106 TN0110

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION

TO-92 Plastic Package	SD1137BD	TN0106N3	TN0110N3
Sorted Chips in Carriers	SD1137CHP	TN0106ND	TN0110ND
Description	60V, 2.5 ohm	60V, 3.0 ohm	100V, 3.0 ohm

FEATURES

- Low Threshold,, $V_{GS(th)}$1.5V max
- Low Output and Transfer Capacitance
- Extended Safe Operating Area
- Complementary P-Channel Drivers Available

APPLICATIONS

- Complementary Voltage and Current Drivers
- Line Drivers
- Pulse Amplifiers
- Solid-State Relays

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise specified)

Drain-Source Voltage
SD1137, TN0106 ..... +60V
TN0110 ..... +100V
SD1137, TN0106 ..... +60V
TN0110 ..... +100V
Gate-Source Voltage ..... ±30V
Continuous Drain Current

	T_A = +25°C	T_C = +25°C
SD1137BD	.25A	.46A
TN0106N3 } TN0110N3 }	.23A	.42A

Peak Pulsed Drain Current ..... +2.0A
Continuous Device Dissipation

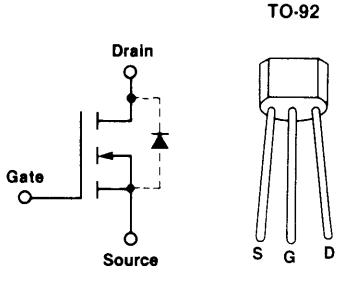
	T_A = +25°C	T_C = +25°C
TO-92 (N3 & BD) pkg	0.30W	1.0W

Linear Derating Factor

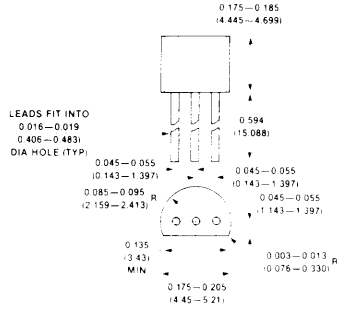
	T_A = +25°C	T_C = +25°C
TO-92 (N3 & BD) pkg	3.0mW/°C	10mW/°C

Operating Junction and Storage Temperature Range -55°C to +150°C
Lead Temperature (1/16" from mounting surface for 30 sec) ..... +250°C

PIN CONFIGURATION

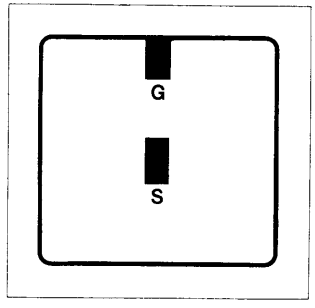


PACKAGE DIMENSIONS TO-92



All dimensions in inches and (millimeters)

CHIP CONFIGURATION



Dimensions: .0445 x .0460 x .013 inches
Drain is backside contact.

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise specified)

#	PARAMETER	SD1137 MIN	SD1137 TYP	SD1137 MAX	TN0106 MIN	TN0106 TYP	TN0106 MAX	TN0110 MIN	TN0110 TYP	TN0110 MAX	UNIT	CONDITIONS		
1	BV_{DSS} Drain-Source Breakdown Voltage	60	90		60	90		100	115		V	I_D = 1.0mA, V_{GS} = 0		
2				100								V_{DS} = 48V	T_A = +125°C	
3							500					V_{DS} = 48V	V_{GS} = 0	
4	Drain-Source									500		V_{DS} = 80V		
5	I_{DSS} Off Leakage		.01	1.0								V_{DS} = 60V		
6	Current					.01	10				μA	V_{DS} = 60V	V_{GS} = 0	
7									.01	10		V_{DS} = 100V		
8	Gate-Body			± 1.0			± 1.0			± 1.0	μA	V_{GB} = ± 30V	V_{DS} = 0	
9	I_{GBS} Leakage Current			1.0			10			10	nA	V_{GB} = ± 20V		
10	$V_{GS(th)}$ Gate-Source Threshold Voltage	0.5		1.5	0.5		1.5	0.5		1.5	V	V_{DS} = V_{GS}, I_D = 1.0mA		
11	$r_{DS(on)}$ Drain-Source			4.5			4.5			4.5	ohms	V_{GS} = 5V, I_D = .25A		
12	On Resistance			2.5								V_{GS} = 10V	I_D = 1.0A	
13							3.0			3.0			I_D = 0.5A	
14	$I_{D(on)}$ On Drain Current				.75			.75			A	V_{GS} = 5V	V_{DS} = 25V	
15		2.0			2.0			2.0				V_{GS} = 10V		(Note 1)
16	g_{fs} Common-Source	300	500								mmhos	V_{DS} = 25V	I_D = 0.5A	
17	Forward Transcond.				225	500		225	500			V_{DS} = 20V	f = 1KHz	
18	V_{SD} Source-Drain			1.5							V	I_{SD} = 0.8A	V_{GS} = 0	
19	Forward Voltage						1.5			1.5		I_{SD} = 0.5A		
20	c_{iss} Common-Source Input Capacitance			60			60			60	pF	V_{DS} = 25V V_{GS} = 0 f = 1MHz		
21	c_{oss} Common-Source Output Capacitance		11	35		11	35		11	35				
22	c_{rss} Common-Source Reverse Transfer Capacitance		1.5	8.0		1.5	8.0		1.5	8.0				
23	t_{on} Turn ON Time		8.0	10		8.0	10		8.0	10	nS	V_{DD} = 25V, $V_{G(on)}$ = 10V		
24	t_{off} Turn OFF Time		8.0	12		8.0	12		8.0	12		R_G = 51Ω, R_L = 25Ω		

NOTE 1: Pulse Test, 80μSec. 1% Duty Cycle

TOPAZ SEMICONDUCTOR

SD1200, SD1201

N-CHANNEL ENHANCEMENT-MODE HIGH-VOLTAGE D-MOS FETs

FEATURES

- Extended Safe Operating Area
- Simple, Straight-Forward, DC Biasing
- Low Capacitance, C_{oss} 1.5 pF (typ.)

APPLICATIONS

- Display Drivers
- Reed Relays
- Low-Power, High-Voltage Drivers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Drain-Source Voltage
SD1200 ..... 450V
SD1201 ..... 400V

Drain-Gate Voltage (V_{GS} = 0)
SD1200 ..... 450V
SD1201 ..... 400V

Gate-Source Voltage ..... ±30V

Continuous Drain Current
SD1200DD, SD1201DD 20mA

Peak Drain Current
SD1200DD, SD1201DD 40mA

Continuous Device Dissipation
SD1200DD, SD1201DD 300mW

Linear Derating Factor
SD1200DD, SD1201DD ..... 2.4mW/°C

Operating Junction Temperature Range ..... −55 to +150°C

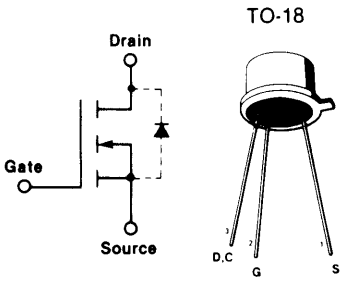
Storage Temperature Range ..... −55 to +150°C

Lead Temperature (1/16″ from mounting surface for 30 Sec) ..... +260°C

ORDERING INFORMATION

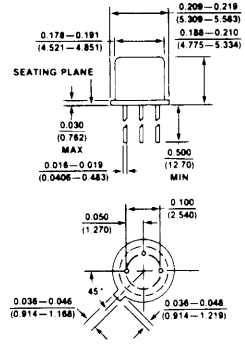
Sorted Chips in Carriers	SD1200CHP	SD1201CHP
TO-18 Package	SD1200DD	SD1201DD
Description	450V, 700 ohm	400V, 500 ohm

SCHEMATIC DIAGRAM



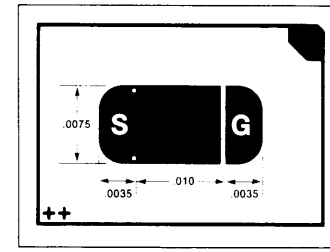
Drain common to case.

PACKAGE DIMENSIONS TO-18



All dimensions in inches and (millimeters)

CHIP CONFIGURATION



Drain is backside contact.
Dimensions: .025 x .034 x .013 inches

Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

ELECTRICAL CHARACTERISTICS (T_A = +25°C)

#		CHARACTERISTIC	SD1200 MIN	SD1200 TYP	SD1200 MAX	SD1201 MIN	SD1201 TYP	SD1201 MAX	UNIT	TEST CONDITIONS
1	STATIC	BV_{DSS} Drain-Source Breakdown Voltage	450	500		400	450		V	I_D = 10μA, V_{GS} = 0
2		$V_{GS(th)}$ Gate-Source Threshold Voltage	1.0	4.0	5.0	1.0	4.0	5.0	V	I_D = 10μA, V_{DS} = V_{GS}
3		I_{GBS} Gate-Body Leakage Current		.02	1.0		.02	1.0	nA	V_{GS} = 20V, V_{DS} = 0
4		I_{DSS} Drain-Source OFF Leakage Current		1.0	100				nA	V_{DS} = 360V, V_{GS} = 0
5							1.0	100		V_{DS} = 320V, V_{GS} = 0
6		$I_{D(on)}$ ON Drain Current	40			40			mA	V_{DS} = 25V, V_{GS} = 15V
7		$r_{DS(on)}$ Drain-Source ON Resistance		400	700		300	500	ohms	I_D = 1mA, V_{GS} = 15V
8	DYNAMIC	g_{fs} Common-Source Forward Transconductance		10			10		mmhos	V_{DS} = 20V, I_D = 20mA f = 1KHz
9		c_{iss} Common-Source Input Capacitance		8.0			8.0		pF	V_{DS} = 20V, V_{GS} = 0 f = 1MHz
10		c_{rss} Common-Source Reverse Transfer Capacitance		0.8			0.8			
11		c_{oss} Common-Source Output Capacitance		1.5			1.5			

TOPAZ SEMICONDUCTOR

SD1202

N-CHANNEL ENHANCEMENT-MODE HIGH-VOLTAGE D-MOS FETs

FEATURES

- Extended Safe Operating Area
- Simple, Straight-Forward, DC Biasing
- Low Capacitance (C_{oss} 1.5 pF typ.)
- Low Leakage (I_{DSS} 1.0 nA typ. @ 180V)
- High Gate Breakdown (±100V min.)

APPLICATIONS

- Display Drivers
- AC-DC Relays
- Reed Relays
- Low-Power, High-Voltage Drivers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

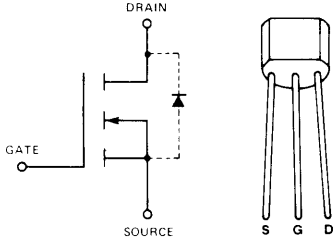
Drain-Source Voltage	200V
Drain-Gate Voltage (V_{GS} = 0)	200V
Gate-Source Voltage	±100V
Continuous Drain Current (Note 1)	20mA
Peak Drain Current (Note 1)	40mA
Continuous Device Dissipation (Note 1)	300mW
Linear Derating Factor (Note 1)	2.4mW/°C
Operating Junction Temperature Range	−55 to +150°C
Storage Temperature Range	−55 to +150°C
Lead Temperature (1/6″ from mounting surface for 30 Sec)	+260°C

Note 1: Not applicable to chips. Final value depends upon mounting substrate.

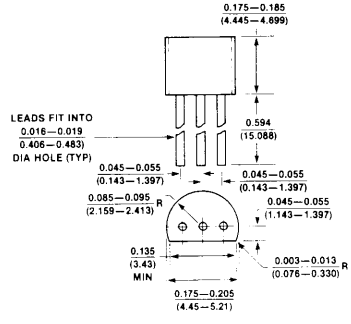
ORDERING INFORMATION

Sorted Chips in Carriers	SD1202CHP
TO-92 Package	SD1202BD
Description	200V, 250 ohm

SCHEMATIC DIAGRAM

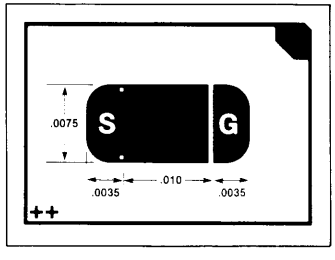


PACKAGE DIMENSIONS TO-92



All dimensions in inches and (millimeters)

CHIP CONFIGURATION



Drain is backside contact.
Dimensions: .025 x .034 x .013 inches