TOPAZ SEMICONDUCTOR

SD200, SD201 SD202, SD203

N-CHANNEL ENHANCEMENT-MODE LATERAL D-MOS FETs

FEATURES

- High Gain—8.0dB min. @ 1GHz
- Low Noise—5.0dB max. @ 1GHz SD202, SD203
- Low Interelectrode Capacitances

APPLICATIONS

- High-Gain VHF/UHF Amplifiers, Oscillators, and Mixers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

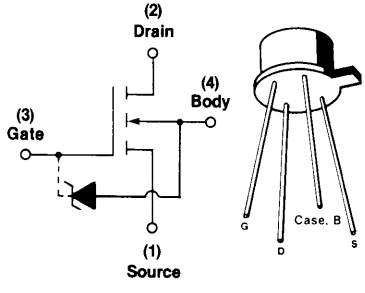
PARAMETER	SD200	SD201	SD202	SD203	UNIT
Breakdown Voltages					
V_{DS}	+25	+25	+20	+20	Vdc
V_{DB}	+25	+25	+20	+20	Vdc
V_{GS}	±40	−0.3	±40	−0.3	Vdc
		+20		+20	Vdc
V_{GB}	±40	−0.3	±40	−0.3	Vdc
		+20		+20	Vdc
V_{GD}	±40	−0.3	±40	+0.3	Vdc
		+20		+20	Vdc

I_D	Continuous Drain Current	50mA
P_T	Power Dissipation (at or below T_C = +25°C)	1.8W
	Linear Derating Factor	18 mW/°C
P_D	Power Dissipation (at or below T_A = +25°C)	360mW
	Linear Derating Factor	3.6 mW/°C
T_j	Operating Junction Temperature Range	−55 to +125°C
T_s	Storage Temperature Range	−65 to +175°C

ORDERING INFORMATION

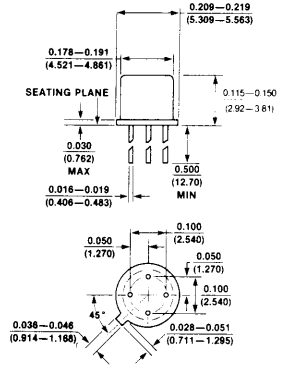
TO-52, 4 Lead Pkg.	SD200DC	SD201DC	SD202DC	SD203DC
Shorting Rings	SD200DC/R	SD201DC/R	SD202DC/R	SD203DC/R
Sorted Chips in Carriers	SD200CHP	SD201CHP	SD202CHP	SD203CHP

SCHEMATIC DIAGRAM

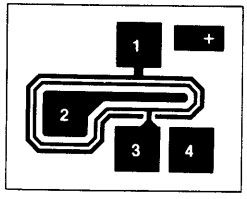


Body internally connected to Case.
Diode protection on SD201/SD203 only.

PACKAGE DIMENSIONS TO-52, 4-LEAD



CHIP CONFIGURATION



PAD
1—Source
2—Drain
3—Gate
4—Diode

For SD201·203CHP bond Gate and Diode to common point. Body is backside contact. Dimensions: .022 x .025 x .013 inches

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SECTION 2

In addition to standard products listed in this section, a wide variety of special electrical selections are available to the user. Specials are available in the same packages as the basic standard products, including chip form. All special electrical selections, including these in chip form, are 100% tested to the selection criteria.

PARAMETER SELECTOR GUIDE

Basic Chip	BV_{DS} min (V)	BV_{DSX} min (V)	BV_{SDX} min (V)	$I_{D(off)}$ max (nA)	$I_{S(off)}$ max (nA)	$V_{GS(th)}$ min (V)	$V_{GS(th)}$ max (V)	$r_{DS(on)}$ max @ 5V (ohms)	$r_{DS(on)}$ max @ 5V (ohms)
SD200-201	25-30	—	—	10-1000	—	0.1-1.0	1.2-2.0	45-70	—
SD202-203	20-25	—	—	10-1000		0.1-1.0	1.2-2.0	35-50	—
SD205	25	—	—	100-1000	—	0.5-1.0	1.2-2.0	7.0-8.0	5.0-6.0
SD210-211	30-35	10-25	10-15	1.0-10	2.0-10	0.5-1.2	1.2-2.0	50-70	40-45
SD214-215	—	20-25	20	1.0-10	2.0-10	0.1-1.2	1.2-2.0	50-70	40-45
SD217	25	15-20	15-20	10-100	20-100	0.1-1.0	1.2-2.0	7.0-8.0	5.0-6.0
SD219	25	15-20	20	10-100	20-100	0.1-1.0	1.2-2.0	7.0-8.0	5.0-6.0
SD303	20-25	—	—	10-1000	—	0.1-0.5	1.5	65-80	—
SD304	25-30	—	—	10-1000	—	0.1-0.5	1.5-2.0	90-130	—
SD306	20-25	—	—	10-1000	—	0.1-0.5	1.5	65-100	—
SD2215	25-35	—	—	50-1000	—	0.5-1.2	1.2-2.0	30-35	22-25
SD5000	—	20-25	20	1.0-10	2.0-10	0.5-1.2	1.2-2.0	50-70	—
SD5001	—	10-25	10	1.0-10	2.0-10	0.5-1.2	1.2-2.0	50-70	—
SD5002	—	15-25	15	1.0-10	2.0-10	0.5-1.2	1.2-2.0	50-70	—
SD5100	30-35	—	—	1.0-10	-	0.5-1.0	1.2-2.0	50-70	40-45
SD5101	15-25	—	—	1.0-10	-	0.5-1.0	1.2-2.0	50-70	40-45
SD5200	30-35	—	—	10-10000	-	0.5-1.2	1.2-2.0	50-80	—

Note: Parameters such as Switching Times (t_{on}, t_{off}), capacitances (eg: C_{iss}, C_{oss}, C_{rss}) Power Gain and Noise Figure are chip design or test circuit dependent and cannot be selected.

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		PARAMETER		SD200, SD201			SD202, SD203			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DS} Drain-Source Breakdown Voltage		25	30		20	25		V	I_D = 1.0μA, V_{GS} = V_{BS} = 0	
2		BV_{DB} Drain-Substrate Breakdown Voltage		25			20				I_D = 1.0μA, V_{GB} = 0 Source OPEN	
3		$I_{D(off)}$ Drain-Source OFF Current				1.0				μA	V_{DS} = 25V	V_{GS} = V_{BS} = 0
4									1.0		V_{DS} = 20V	
5		I_{GBS} Gate-Body Leakage Current	SD200			±0.1				nA	V_{GB} = ±40V	V_{DB} = V_{SB} = 0
6			SD202						±0.1			
7			SD201			1.0				μA	V_{GB} = 20V	
8			SD203						1.0			
9		$V_{GS(th)}$ Gate Threshold Voltage		0.1	1.0	2.0	0.1	1.0	2.0	V	V_{DS} = V_{GS}, I_D = 1μA, V_{SB} = 0	
10		$r_{DS(on)}$ Drain-Source ON Resistance			40	70		35	50	ohms	V_{GS} = 5V I_D = 1mA V_{SB} = 0	
11	DYNAMIC	g_{fs} Common-Source Forward Transcond.		13	14		17	20		mmhos	I_D = 20mA V_{DS} = 15V f = 1KHz, V_{SB} = 0	
12		c_{iss} Common-Source Input Capacitance			2.4	3.0		3.0	3.6	pF	I_D = 20mA	V_{DS} = 15V f = 1MHz V_{SB} = 0
13		c_{oss} Common-Source Output Capacitance			1.0	1.2		1.0	1.2		V_{GS} = 0	
14		c_{rss} Common-Source Reverse Transfer Capacitance			0.2	0.3		0.2	0.3			
15		G_{ps} Common-Source Power Gain		8.0	10		8.0	10		dB		V_{DS} = 15V f = 1GHz I_D = 20mA V_{SB} = 0
16		NF Noise Figure			4.5	6.0		4.0	5.0	dB		
17		P_i Interept Point			29			29		dBM	Δf = 2MHz	

TOPAZ SEMICONDUCTOR

SD217, SD219

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FET

ORDERING INFORMATION

TO-72 Package	SD217DE	SD219DE
Shorting Ring	SD217DE/R	SD219DE/R
Sorted Chips in Waffle Pack	SD217CHP	SD219CHP
Description	6.0 ohm, 25V V_{SB} = 15V min	6.0 ohm, 25V V_{SB} = 20V min

FEATURES

- CMOS Compatible Input
- Small Package, Standard Pin-Out
- TTL and CMOS Compatible Input
- Low Capacitance
- Peak Pulsed Current, 1 Amp min

APPLICATIONS

- ± 10V Analog Switch, SD219DE
- ± 7.5 Analog Switch, SD217DE
- High Speed, Medium Power, Switch Drivers
- Sample and Hold and Track and Hold
- A-to-D and D-to-A Converters

ABSOLUTE MAXIMUM RATINGS (T_A = + 25 °C unless otherwise specified)

V_{DS} Drain-Source Voltage ..... + 25V

V_{DB} Drain-Body Voltage
- SD217 ..... + 22.5V
- SD219 ..... + 25V

V_{SD} Source-Drain Voltage
- SD217 ..... + 15V
- SD219 ..... + 20V

V_{SB} Source-Body Voltage
- SD217 ..... + 22.5V
- SD219 ..... + 25V

V_{GB} Gate-Body Voltage ..... + 30V

V_{GS} Gate-Source Voltage ..... ± 22.5V

V_{GD} Gate-Drain Voltage ..... ± 22.5V

I_D Peak Pulsed Drain Current ..... + 1.0A

I_D Continuous Drain Current (Note 1) 160mA

P_D Continuous Power Dissipation (Note 1)
- T_A = + 25 °C (Free Air) 300mW
- T_C = + 25 °C (Infinite Heat Sink) 1.2W

Power Derating Factors (Note 1)
- Free Air ..... 3.0mW/ °C
- Infinite Heat Sink ..... 12mW/ °C

Thermal Resistance (Note 1)

O_{ja} Junction to Ambient ..... 333 °C/W

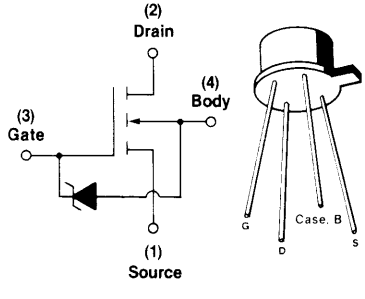
O_{jc} Junction to Case ..... 83 °C/W

T_{op} Operating Junction Temperature Range ..... -55 to + 125 °C

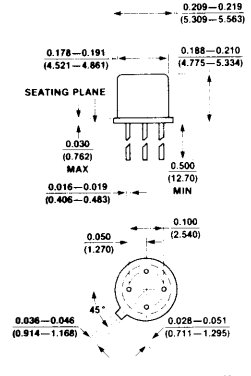
T_{stg} Storage Temperature Range ..... -55 to + 150 °C

Note 1: Not applicable to chips. Final value depends on mounting.

SCHEMATIC DIAGRAM

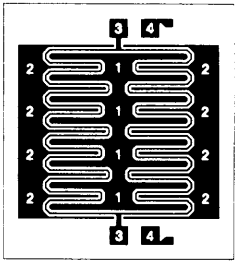


PACKAGE DIMENSIONS TO-72



All dimensions in inches and (millimeters)

CHIP CONFIGURATION



1—Drain 2—Source 3—Gate 4—Diode
Minimum bonding required. One Drain, One Source (left), One Source (right), One Gate. Bond Gate and Adjacent Diode to Common Point to Connect Protective Diode.

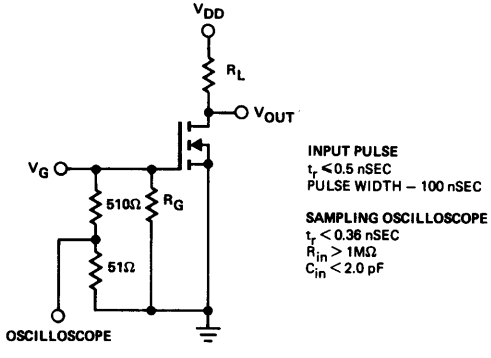
Size: .040 x .044 x .013 inch.
Body (Substrate) is backside contact.

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise specified)

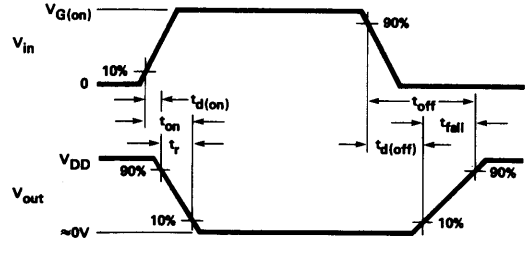
#		CHARACTERISTIC		MIN	TYP	MAX	UNITS	TEST CONDITIONS
1	STATIC	BV_{DS} Drain-Source Breakdown Voltage		25	30		V	I_D = 10μA, V_{GS} = V_{BS} = 0
2				15	20			I_D = 100nA, V_{GS} = V_{BS} = -5V
3		BV_{SD} Source-Drain Breakdown Voltage	SD217	15			V	I_S = 100nA, V_{GD} = V_{BD} = -5V
4			SD219	20				
5		BV_{DB} Drain-Body Breakdown Voltage	SD217	22.5			V	I_D = 100nA, V_{GB} = 0, Source Open
6			SD219	25				
7		BV_{SB} Source-Body Breakdown Voltage	SD217	22.5			V	I_S = 100nA, V_{GB} = 0, Drain Open
8			SD219	25				
9		$I_{D(off)}$ Drain-Source OFF Leakage Current				100	nA	V_{DS} = 15V, V_{GS} = V_{BS} = -5V
10		$I_{S(off)}$ Source-Drain OFF Leakage Current				100		V_{SD} = 15V, V_{GD} = V_{BD} = -5V
11		I_{GB} Gate-Body ON Leakage Current				10	μA	V_{GB} = 30V, V_{GS} = V_{GD} = 22.5V
12		$V_{GS(th)}$ Gate-Source Threshold Voltage		0.1		2.0	V	V_{DS} = V_{GS}, I_D = 10μA, V_{SB} = 0
13		$I_{D(on)}$ Drain-Source ON Current (Note 1)		1.0			A	V_{DS} = V_{GS} = 10V, V_{SB} = 0
14		$r_{DS(on)}$ Drain-Source ON Resistance (Note 1)				8.0	ohms	V_{GS} = 5.0V, I_D = 50mA, V_{SB} = 0
15						6.0		
16						6.0		V_{GS} = 10V, I_D = 500mA, V_{SB} = 0
17	DYNAMIC	g_{fs} Common-Source (Note 1) Forward Transconductance		100			mmhos	V_{DS} = 15V, I_D = 200mA, V_{SB} = 0, F = 1KHz
18		$C_{(gs+gd+gb)}$ Gate Node Capacitance				30	pF	V_{DS} = 10V, $V_{GS}V_{BS}$ = -15V, f = 1MHz
19		$C_{(gd+db)}$ Drain-Node Capacitance				15		
20		$C_{(gs+sb)}$ Source Node Capacitance				40		
21		$C_{(dg)}$ Reverse Transfer Capacitance				5.0		
22		t_{on} Turn ON Time			2.0	4.0	nS	V_{DD}= 10V, $V_{G(on)}$ = 10V, R_L= 133Ω, R_G= 51Ω
23		t_{off} Turn OFF Time			3.0	5.0		

Note 1: Pulse Test 80μSec, 1% Duty Cycle

SWITCHING TIMES TEST CIRCUIT

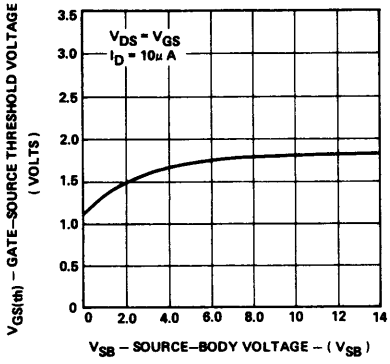


TEST WAVEFORMS

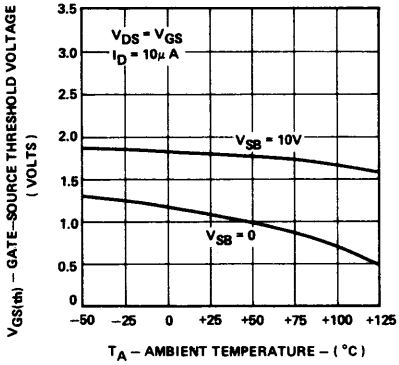


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise specified)

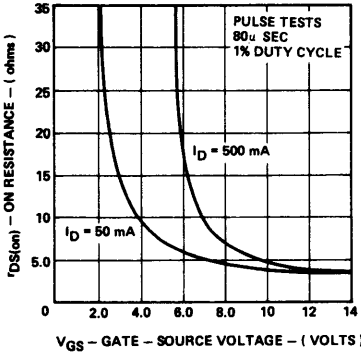
GATE-SOURCE THRESHOLD VOLTAGE —VS— SOURCE-BODY VOLTAGE



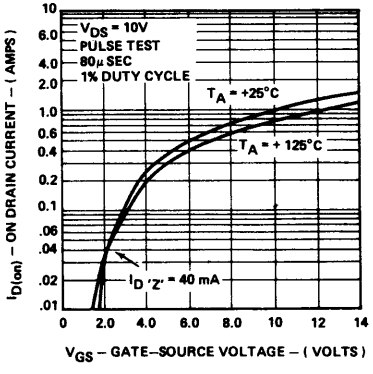
GATE-SOURCE THRESHOLD VOLTAGE —VS— TEMPERATURE



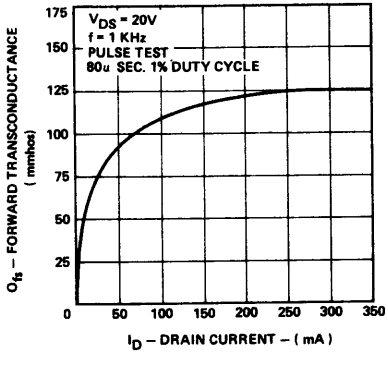
DRAIN-SOURCE ON RESISTANCE —VS— GATE-SOURCE VOLTAGE



ON DRAIN CURRENT —VS— GATE-SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE —VS— ON DRAIN CURRENT



TOPAZ SEMICONDUCTOR

SD303

N-CHANNEL ENHANCEMENT-MODE DUAL GATE D-MOS FET

FEATURES

- Normally Off-Enhancement-Mode Operation
- Dual Gate with Gate Protective Diodes
- Low Feedback Capacitance — c_{rss} .02pF (typ)
- Wide Dynamic Range-Remote AGC capability
- High Power Gain- 10dB min. @ 1GHz
- Low Noise-7.0dB max. @ 1GHz
- Low Cross-Modulation Distortion

APPLICATIONS

- Wide Band (Unneutralized) VHF/UHF Amplifiers
- VHF/UHF Linear Mixers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

V_{DS} Drain-Source Voltage ..... +20V
V_{G1B} Gate 1-Substrate Voltage ..... −0.3 to +10V
V_{G2B} Gate 2-Substrate Voltage ..... −0.3 to +15V
I_D Continuous Drain Current (Note 1) 50mA
P_D Continuous Power Dissipation (Note 1)
T_A = +25°C (Free Air) 360mW
T_C = +25°C (Infinite Heat Sink) 1.8W
Power Derating Factors (Note 1)
Free Air ..... 3.6mW/°C
Infinite Heat Sink ..... 18mW/°C

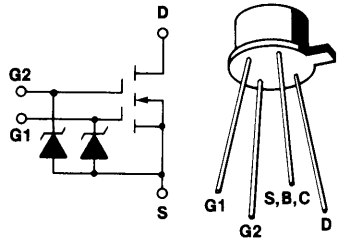
T_{op} Operating Junction Temperature Range ..... −55 to +125°C
T_{stg} Storage Temperature Range .. −65 to +175°C

Note 1: Not applicable to chips. Final value depends mounting substrate.

ORDERING INFORMATION

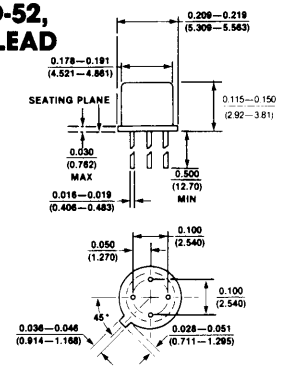
Sorted Chips in Carriers	SD303CHP
TO-52, 4 Lead Package	SD303DC
Shorting Rings	SD303DC/R

SCHEMATIC DIAGRAM



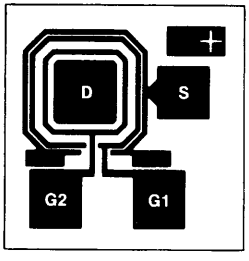
Pin 1-Drain, 2-Gate 2
Pin 3-Gate 1,
Pin 4-Source, Substrate, Case

PACKAGE DIMENSIONS TO-52, 4 LEAD



All dimensions in inches and (millimeters)

CHIP CONFIGURATION



Chip backside connected to source
Dimensions: .022 x .022 x .013 inches

Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

ELECTRICAL CHARACTERISTICS (TA = +25°C unless otherwise noted)

#		PARAMETER		SD303 MIN	SD303 TYP	SD303 MAX	UNIT	TEST CONDITIONS	
1	STATIC	BV_{DS}	Drain-Source Breakdown Voltage	20	25		V	$I_D = 5\mu A$ $V_{G1S} = V_{G2S} = 0$	
2	STATIC	I_{DSS}	Drain-Source OFF Leakage Current		.01	1.0	μA	$V_{DS} = 15V$ $V_{G1S} = V_{G2S} = 0$	
3	STATIC	I_{G1SS}	Gate 1 Leakage Current		1.0	100	nA	$V_{G1S} = 5V$ $V_{G2S} = V_{DS} = 0$	
4	STATIC	I_{G2SS}	Gate 2 Leakage Current		1.0	100	nA	$V_{G2S} = 10V$ $V_{G1S} = V_{DS} = 0$	
5	STATIC	V_{T1}	Gate 1-Source Threshold Voltage	0.1	0.5	1.5	V	$V_{DS} = V_{G1S}$ $V_{G2S} = 10V$, $I_D = 1\mu A$	
6	STATIC	V_{T2}	Gate 2-Source Threshold Voltage	0.1	0.5	1.5	V	$V_{G1S} = 4V$	$V_{DS} = V_{G2S}$ $I_D = 1\mu A$
7	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance		65	80	ohms	$I_D = 1mA$, $V_{G1S} = 5V$ $V_{G2S} = 10V$	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	13	15		mmhos	$V_{DS} = 15V$, $I_D = 18mA$ $V_{G2S} = 10V$, f = 1KHz	
9	DYNAMIC	c_{iss}	Common-Source Input Capacitance		3.0	3.5	pF	$V_{DS} = 15V$, $I_D = 18mA$ $V_{G2S} = 10V$, f = 1MHz	
10	DYNAMIC	c_{oss}	Common-Source Output Capacitance		0.6		pF	$V_{DS} = 15V$, $V_{G1S} = 0$ $V_{G2S} = 10V$, f = MHz	
11	DYNAMIC	c_{rss}	Common-Source Reverse Transfer Capacitance		.02		pF		
12	DYNAMIC	G_{ps}	Power Gain	10	14		dB	f = 1GHz	$V_{DS} = 15V$ $V_{G2S} = 10V$ $I_D = 18mA$
13	DYNAMIC	NF	Noise Figure		5.5	7.0	dB	f = 1GHz	
14	DYNAMIC	AGC (V_{G2S})	Range of Automatic Gain Control		40		dB	$V_{G1S} \cong 2.5V$ f = 500MHz	$V_{DS} = 15V$ $V_{G2S} = 10V$ to 0V
15	DYNAMIC	E_{INT}	Interfering Signal at Gate for 1% Cross-Modulation Distortion (Peak Voltage ref. to 300 ohm system)		150		mV	fo = 1.000GHz fi = 0.995GHz	$V_{DS} = 15V$ $V_{G2S} = 10V$ $I_D = 18mA$