High-Speed Analog N-Channel/Enhancement-Mode DMOS FETS

calogic CORPORATION

SD400 / SD402

FEATURES

- Fast switching ..... t_{on} <1ns
- Low capacitance ..... C_{rss} 0.3 pF (typ)
- Low threshold ..... <1.5V max
- CMOS and TTL Compatible Input

APPLICATIONS

- Switch Drivers
- Video Switches
- Active Pullups
- VHF/UHF Amplifiers

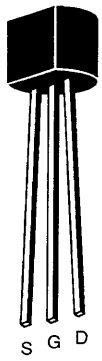
DESCRIPTION

The SD400 and SD402 are N-Channel Enhancement Mode devices processed utilizing Calogics proprietary high speed, low capacitance lateral DMOS technology. These devices are excellent switch drivers where low threshold offers the designer the advantage of CMOS and TTL compatibility with ultra high switching speeds.

ORDERING INFORMATION

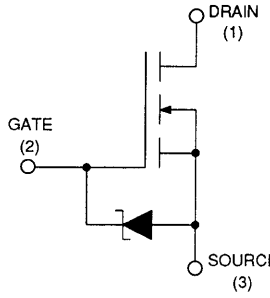
Part	Package	Temperature Range
SD400BD	Plastic TO-92	-40°C to +125°C
SD402BD	Plastic TO-92	-40°C to +125°C
XSD400	Sorted Chips in Carriers	-40°C to +125°C
XSD402	Sorted Chips in Carriers	-40°C to +125°C

PIN CONFIGURATION

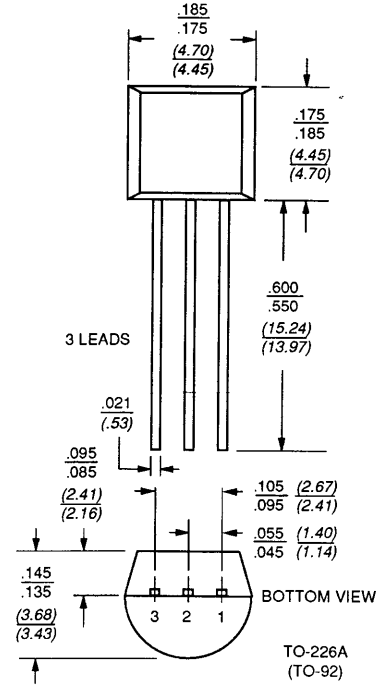


CD1

SCHEMATIC DIAGRAM



PACKAGE DIMENSIONS



ABSOLUTE MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

V_{DS} Drain-Source Voltage
SD400 ..... +30V
SD402 ..... +15V
V_{GS} Gate-Source Voltage ..... -0.3 V
+20 V
V_{DG} Gate-Drain Voltage ..... -0.3 V
+20 V

V_{SD} Source-Drain Voltage ..... -0.3 V
I_D Continuous Drain Current ..... 50 mA
Power Dissipation (at or below T_C = +25°C) .. 300mW
Linear Derating Factor ..... 3.0 mW/ °C
Operating Storage and
Junction Temperature Range ..... -40°C to +125°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

SYMBOL	CHARACTERISTICS	SD400			SD402			UNIT	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
STATIC									
BV_{DSS}	Drain-Source Breakdown Voltage	30	35		15	25		V	I_D = 1.0µA, V_{GS} = 0
$I_{D(OFF)}$	Drain-Source OFF Leakage Current			1.0			1.0	µA	V_{DS} = 15 V, V_{GS} = 0
I_{GSS}	Gate-Source Leakage Current			1.0			1.0	µA	V_{GS} = 20 V, V_{DS} = 0
$I_{D(ON)}$	Drain-Source ON Current	50	100		50	100		mA	V_{DS} = 10 V, V_{GS} = 10 V Pulse Test
$V_{GS(th)}$	Gate-Source Threshold Voltage	0.7		1.5	0.7		1.5	V	I_D = 1.0 µA, V_{DS} = V_{GS}
$V_{DS(ON)}$	Drain-Source ON Voltage		150	250		150	250	mV	I_D = 1 mA, V_{GS} = 2.4 V
$r_{DS(ON)}$	Drain-Source ON Resistance		150	250		150	250	ohms	
$V_{DS(ON)}$	Drain-Source ON Voltage		60	80		60	80	mV	I_D = 1 mA, V_{GS} = 4.5 V
$r_{DS(ON)}$	Drain-Source ON Resistance		60	80		60	80	ohms	
DYNAMIC									
g_{fs}	Common-Source Forward Transconductance	8.0	12		8.0	12		mS	I_D = 20 mA, V_{DS} = 10 V f = 1 KHz Pulse Test
C_{iss}	Common-Source Input Capacitance		4.0	5.0		4.0	5.0	pF	V_{DS} = 10 V, V_{GS} = 0 f = 1 MHz
C_{oss}	Common-Source Output Capacitance		1.8	2.5		1.8	2.5		
C_{rss}	Common-Source Reverse Transfer Capacitance		0.3	0.5		0.3	0.5		
$t_{d(ON)}$	Turn ON Delay Time		0.7	1.0		0.7	1.0	nS	V_{DD} = 10 V, R_L = 680 $V_{G(ON)}$ = 10 V, R_G = 51 C_L = 1.5 pF
t_r	Rise Time		0.8	1.0		0.8	1.0		
$t_{(OFF)}$	Turn OFF Time		12			12			

High Speed DMOS N-Channel Switch

calogic CORPORATION

SD403

FEATURES

- Ultra High Speed Switching ..... t_r < 1ns
- Very Low Capacitance ..... C_{rss} 0.4pf typical
- CMOS and TTL Compatible Input
- Low ON Resistance .....40 ohms typical

APPLICATIONS

- Switch Drivers
- Video Switches
- Samples and Hold
- Track and Hold
- VHF/UHF Amplifiers

DESCRIPTION

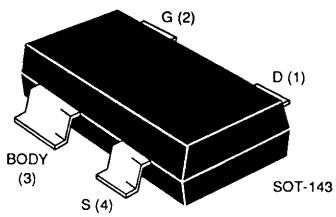
The Calogic SD403 is an N-Channel Enhancement-Mode Lateral DMOS FET. This product has very low capacitance, (C_{rss} < 0.4pf typical) allowing for high speed switching (t_r 1ns). The SD403 is a high gain device (19mmhos) and has good performance values for sample and hold circuits, video switches and switch drivers where lower capacitance and high speed switching are critical.

ORDERING INFORMATION

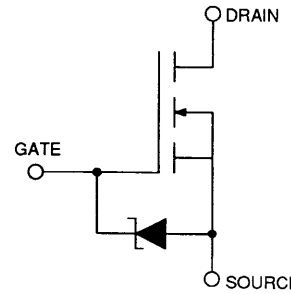
Part	Package	Temperature Range
SD403BD	Plastic TO-92	-55 to +125°C
SD403CY	SOT-143 Surface Mount	-55 to +125°C
XSD403	Sorted Chips in Carriers	-55 to +125°C

PIN CONFIGURATION

CD1



SCHEMATIC DIAGRAM



PACKAGE DIMENSIONS AT END OF THIS DATA SHEET.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Drain-Source Voltage ..... +15V
Gate-Source Voltage ..... -0.3V
+20V
Gate-Drain Voltage ..... -0.3V
+20V
Source-Drain Voltage ..... -0.3V

Continuous Drain Current 50mA
Power Dissipation (at or below T_A = +25°C) 300mW
Linear Derating Factor ..... 3.0mW/ °C
Operating Junction and Storage
Temperature Range ..... -55°C to +125°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise specified)

SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNIT	TEST CONDITIONS
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	15	25		V	I_D = 1.0μA, V_{GS} =0
$I_{D(OFF)}$	Drain-Source OFF Leakage Current			1.0	μA	V_{DS} = 15V, V_{GS} = 0
I_{GSS}	Gate-Source Leakage Current			1.0	μA	V_{GS} = 20V, V_{DS} = 0
$I_{D(ON)}$	Drain-Source ON Current	80	120		mA	V_{DS} = 10V, V_{GS} = 10 V Pulse Test
$V_{GS(th)}$	Gate-Source Threshold Voltage	0.5		1.5	V	I_D = 1.0μA, V_{DS} = V_{GS}
$V_{DS(ON)}$	Drain-Source ON Voltage		140	175	mV	I_D = 1mA, V_{GS} = 2.4V
$r_{DS(ON)}$	Drain-Source ON Resistance		140	175	ohms	
$V_{DS(ON)}$	Drain-Source ON Voltage		40	60	mV	I_D = 1mA, V_{GS} = 4.5V
$r_{DS(ON)}$	Drain-Source ON Resistance		40	60	ohms	
DYNAMIC						
gfs	Common-Source Forward Transconductance	15	19		mS	I_D = 20mA V_{DS} = 10V, f = 1KHz Pulse Test
C_{iss}	Common-Source Input Capacitance		4.5	6.0	pf	V_{DS} = 10V, V_{GS} = 0 f = 1MHz
C_{oss}	Common-Source Output Capacitance		2.0	3.0		
C_{rss}	Common-Source Reverse Transfer Capacitance		0.4	0.6		
td(on)	Turn ON Delay Time		0.8	1.2	nS	V_{DD} = 10V, R_L = 680Ω $V_{G(ON)}$ = 10V, R_G = 51Ω C_L = 1.5pF
t_r	Rise Time		0.9	1.2		
$t_{(OFF)}$	Turn OFF Time		1.4			

SD403

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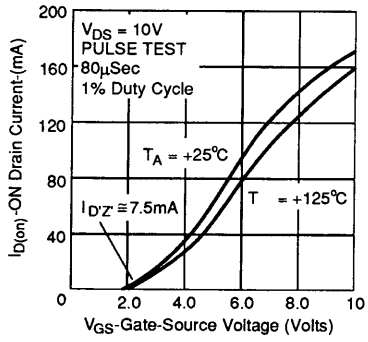
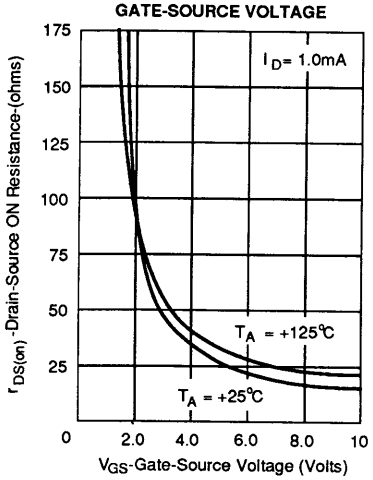
TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise noted)

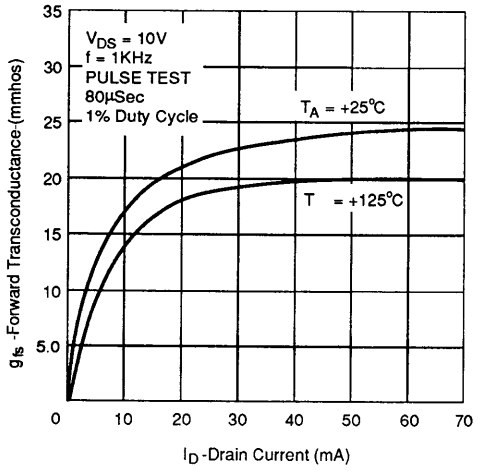
ON DRAIN CURRENT
-VS-
GATE-SOURCE VOLTAGE



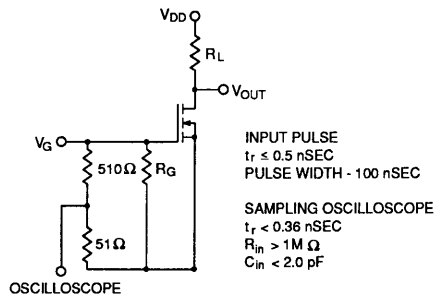
DRAIN-SOURCE ON RESISTANCE
-VS-
GATE-SOURCE VOLTAGE



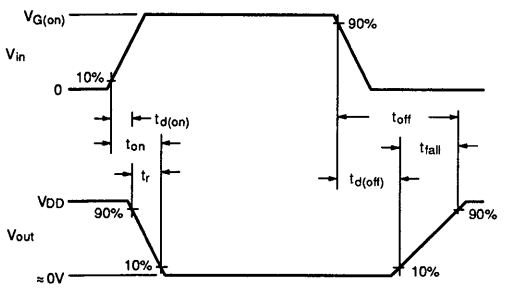
FORWARD TRANSCONDUCTANCE
-VS-
ON DRAIN CURRENT



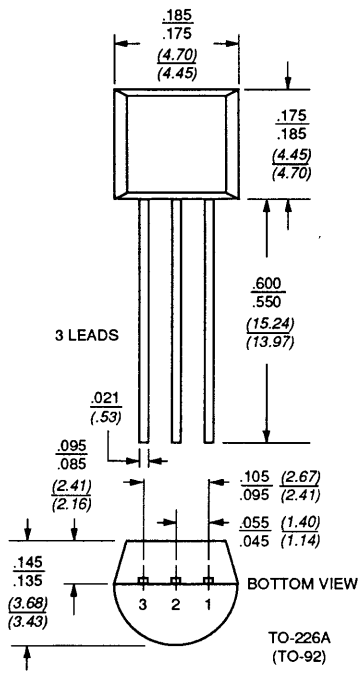
SWITCHING TIMES TEST CIRCUIT

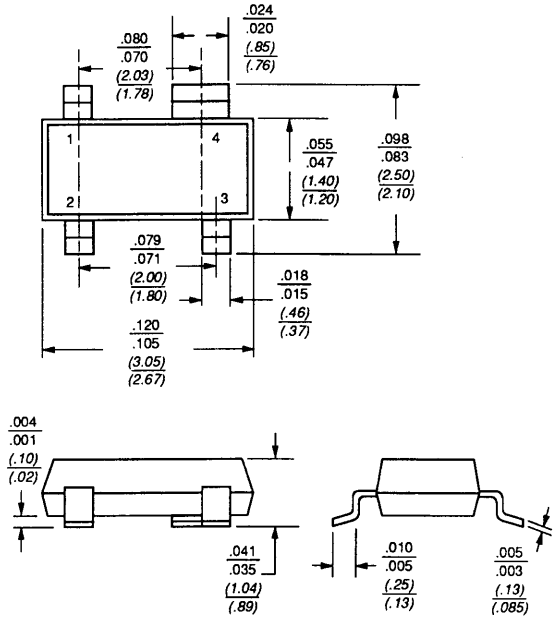


TEST WAVEFORMS



PACKAGE DIMENSIONS





High Speed DMOS N-Channel Switch

calogic CORPORATION

SD404

FEATURES

- High Speed Switching ..... t_r < 2ns
- Low Capacitance .....C_{rss} 1.2pF typical
- Very Low on Resistance .....8 ohm max
- Low Threshold ..... < 1.5V
- CMOS and TTL Compatible Input
- Available in Surface Mount Package

APPLICATIONS

- Switch Drivers
- Video Switches
- VHF/UHF Amplifiers

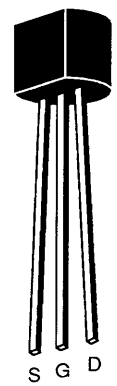
DESCRIPTION

The SD404 is an N-Channel Enhancement Mode device processed with Calogic's ultra high speed lateral DMOS technology. The SD404 is an excellent switch driver or analog switch. Its low threshold offers the designer an advantage in applying the benefits of low on resistance and high speed switching to low voltage circuits.

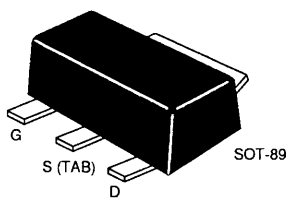
ORDERING INFORMATION

Part	Package	Temperature Range
SD404BD	Plastic TO-92 Package	-55°C to +125°C
XSD404	Sorted Chips in Carriers	-55°C to +125°C
SD404CY	SOT-89 Surface Mount	-55°C to +125°C

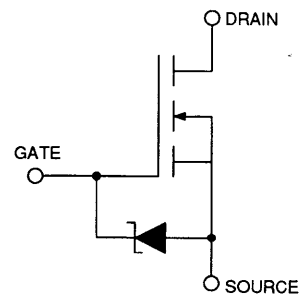
PIN CONFIGURATION



CD3



SCHEMATIC DIAGRAM



PACKAGE DIMENSIONS AT END OF THIS DATA SHEET.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Drain-Source Voltage ..... +20V
Gate-Source Voltage ..... -0.3V
+20V
Gate-Drain Voltage ..... -0.3V
+20V
Source-Drain Voltage ..... -0.3V

Peak Pulsed Drain Current ..... +0.8A
Continuous Drain Current 100mA
Power Dissipation (at or below T_A = +25°C) 300mW
Linear Derating Factor ..... 3.0mW/ °C
Operating Junction and Storage
Temperature Range ..... -40°C to +125°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise specified)

SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNIT	TEST CONDITIONS	
STATIC							
BV_{DSS}	Drain-Source Breakdown Voltage	20	25		V	I_D = 1.0μA, V_{GS} =0	
$I_{D(OFF)}$	Drain-Source OFF Leakage Current			1.0	μA	V_{DS} = 15V, V_{GS} = 0	
I_{GSS}	Gate-Source Leakage Current			10	μA	V_{GS} = 20V, V_{DS} = 0	
$I_{D(ON)}$	Drain-Source ON Current	0.8	1.2		A	V_{DS} = 10V, V_{GS} = 10 V (Note 1)	
$V_{GS(th)}$	Gate-Source Threshold Voltage	0.5	1.1	1.5	V	I_D = 1.0μA, V_{DS} = V_{GS}	
$V_{DS(ON)}$	Drain-Source ON Voltage			200	mV	I_D = 10mA V_{GS} = 2.4V	(Note 1)
$r_{DS(ON)}$	Drain-Source ON Resistance			20	ohms		
$V_{DS(ON)}$	Drain-Source ON Voltage			800	mV	I_D = 100mA V_{GS} = 4.5V	
$r_{DS(ON)}$	Drain-Source ON Resistance			8.0	ohms		
DYNAMIC							
gfs	Common-Source Forward Transconductance	100			mS	I_D = 0.3A V_{DS} = 20V f = 1KHz	(Note 1)
C_{iss}	Common-Source Input Capacitance		12	18	pf	V_{DS} = 20V, V_{GS} = 0 f = 1MHz	
C_{oss}	Common-Source Output Capacitance		6.0	8.0			
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2	2.0			
td(on)	Turn ON Delay Time		1.0	1.5	nS	V_{DD} = 10V, R_L = 390Ω $V_{G(ON)}$ = 10V, R_G = 51Ω C_L = 1.5pF	
t_r	Rise Time		1.0	2.0			
$t_{(OFF)}$	Turn OFF Time		1.0				

Note 1: Pulse Test, 80μSec, 1% Duty Cycle

DMOS

SD404

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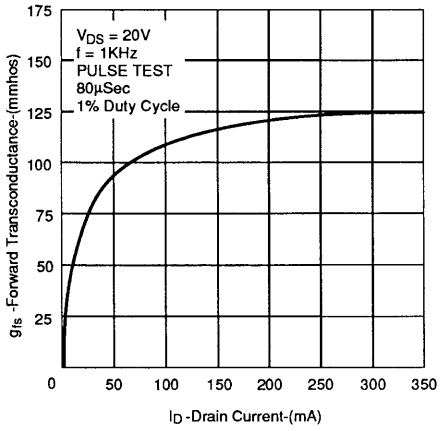
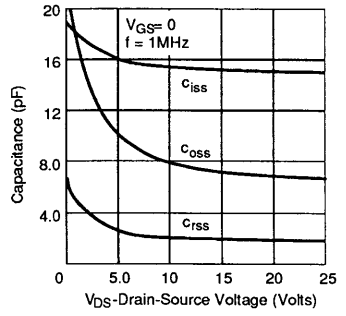
TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise noted)

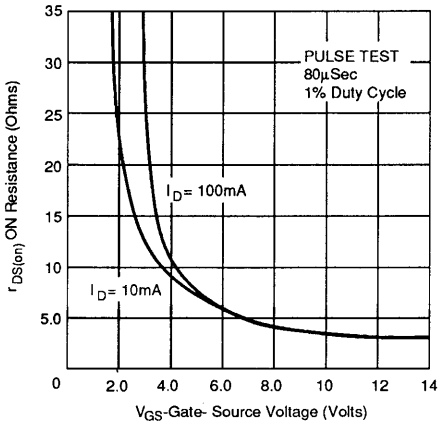
FORWARD TRANSCONDUCTANCE -VS- ON DRAIN CURRENT



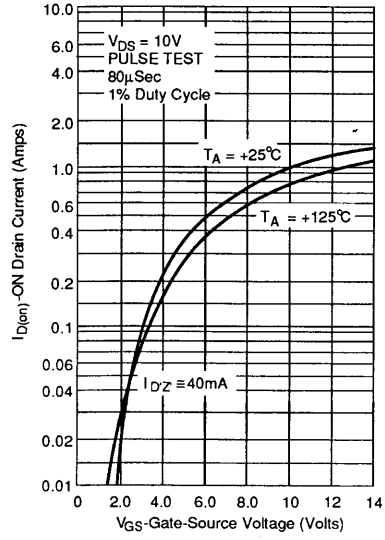
CAPACITANCES -VS- DRAIN-SOURCE VOLTAGE



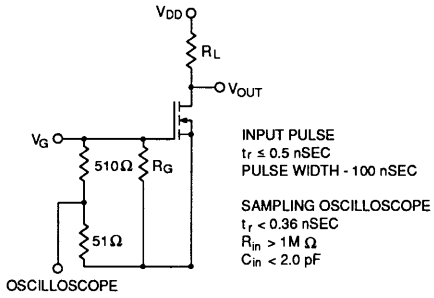
DRAIN-SOURCE ON RESISTANCE -VS- GATE-SOURCE VOLTAGE



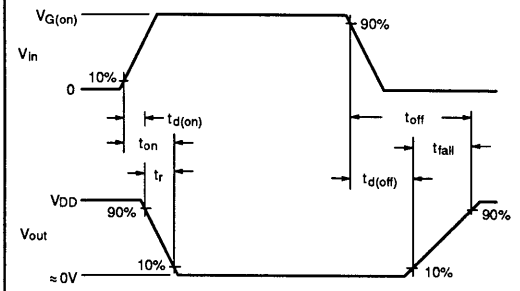
ON DRAIN CURRENT -VS- GATE-SOURCE VOLTAGE



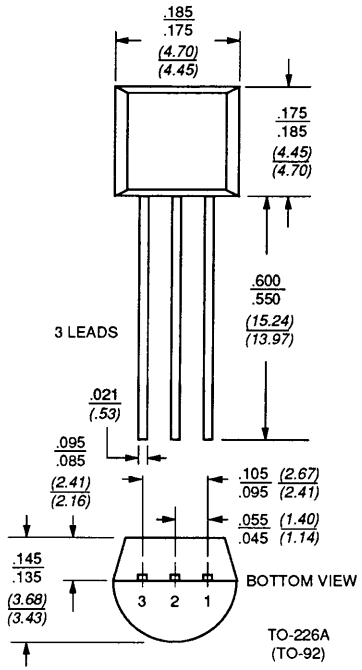
SWITCHING TIMES TEST CIRCUIT

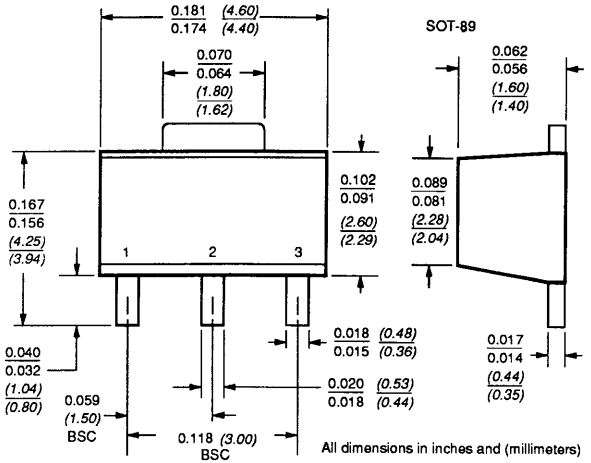


TEST WAVEFORMS



PACKAGE DIMENSIONS





N-Channel Enhancement Mode Dual DMOS FET

calogic CORPORATION

SD411

FEATURES

- **Normally "OFF" Configuration**
- **High Speed Switching ..... under 1 ns (typically)**
- **Ultra Low Capacitance .....C_{iss} <3.5 pf (typically)**
- **Tight Matching Characteristics**
- **Pin Compatible to Industry Standard Dual JFETs with Addition of Substrate Bias Pin**

APPLICATIONS

- **Wideband Differential Amplifiers**
- **Cascode Amplifiers**
- **High Intercept Point Balanced Mixers**
- **Oscillators**
- **High Speed Analog Comparators**

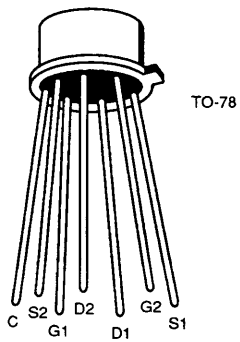
DESCRIPTION

The SD411 is constructed utilizing Calogic's high speed lateral DMOS techniques featuring tight matching characteristics between each FET. This device is an excellent choice for instrumentation, communication, RF and Video designs.

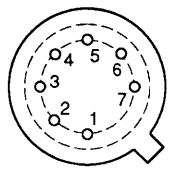
ORDERING INFOMATION

Part	Package	Temperature Range
SD411	TO-78 Hermetic Package	-55°C to +150°C
XSD411	Sorted Chips in Carriers	-55°C to +150°C

PIN CONFIGURATION

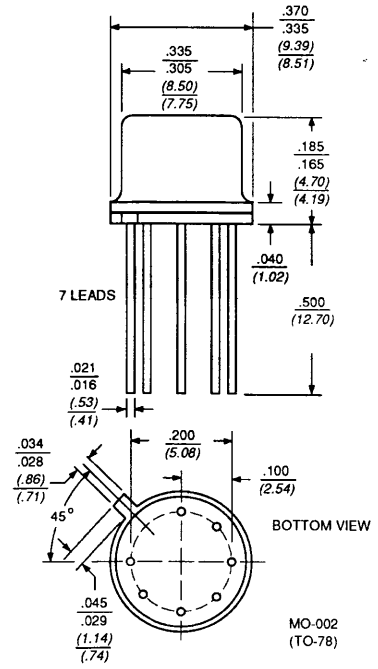


1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 CASE/BODY
5 SOURCE 2
6 DRAIN 2
7 GATE 2



BOTTOM VIEW

PACKAGE DIMENSIONS



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

V_{DS}	Drain-Source Voltage	+20V	P_D	Device Dissipation (each side) 360 mW
V_{SD}	Source-Drain Voltage	+10V		Derating Factor 2.88 mW/°C
V_{DB}	Drain-Body voltage	+25V	P_D	Total Device Dissipation 500 mW
V_{SB}	Source-Body Voltage	+15V		Derating Factor 4 mW/°C
V_{GD}	Gate-Drain Voltage	+25V	T_j	Operating Junction Temperature Range -55 to +150°C
V_{GS}	Gate-Source Voltage	+25V	T_S	Storage Temperature Range -55 to +150°C
V_{GB}	Gate-Body Voltage	+25V	T_L	Lead Temperature (1/16' from mounting surface for 10 sec.) +260°C
V_{G1G2}	Gate-to-Gate Voltage	+25V		
V_{D1D2}	Drain-to-Drain Voltage	+20V		
V_{S1S2}	Source-to-Source Voltage	+15V		
I_D	Continuous Drain Current	+50 mA		

ELECTRICAL CHARACTERISTICS(T_A = +25°C per side unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	TEST CONDITIONS
STATIC						
BV_{DS}	Drain Source Breakdown Voltage	20			V	I_D = 10 nA, V_{GS} = V_{BS} = -5V
BV_{SD}	Source-Drain Breakdown Voltage	10				I_S = 10 nA, V_{GD} = V_{BD} = -5V
BV_{DB}	Drain-Body Breakdown Voltage	25				I_D = 10 nA, V_{GB} = 0 Source Open
BV_{SB}	Source-Body Breakdown Voltage	15				I_S = 10μA, V_{GB} = 0 Drain Open
I_{DSX}	Drain-Source Leakage Current		0.7	10	nA	V_{DS} = 20V, V_{GS} = V_{BS} = -5V
I_{GBS}	Gate-Body Leakage Current			1.0	μA	V_{GS} = 25V, V_{DB} = V_{SB} = 0
$V_{GS(th)}$	Gate-Source Threshold Voltage	0.5	1.0	2.0	V	I_D = 1.0μA, V_{DS} = V_{GS}, V_{SB} = 0
$r_{DS(ON)}$	Drain-Source ON Resistance (1)			70	ohms	I_D = 1.0mA, V_{GS} = 5.0V, V_{SB} = 0
DYNAMIC						
g_{fs}	Common-Source Forward Transconductance(1)	10	12		mS	V_{DS} = 10V, I_D = 20mA, V_{SB} = 0 f = 1KHZ
C_{iss}	Common-Source Input Capacitance		3.5		pF	V_{DS} = 10V, V_{GS} = V_{BS} = 0 f = 1MHZ
C_{oss}	Common-Source Output Capacitance		1.2			
C_{rss}	Common Source Reverse Transfer Capacitance		0.3			
$C_{(gs + sb)}$	Source Node Capacitance		4.5			
MATCH						
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate Source Voltage		25		mV	V_{DS} = 10V I_D = 5.0mA V_{SB} = 0
$\frac{\Delta \lvert V_{GS1} - V_{DS2} \rvert}{\Delta T}$	Differential Drift		25		μV/ °C	T_A = -55°C to +125C°

NOTE 1: Pulse Test, 80sec, 1% Duty Cycle

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