N-CHANNELL POWER MOS TRANSISTORS

SGSP111
SGSP112

PRELIMINARY DATA

HIGH SPEED SWITCHING APPLICATIONS

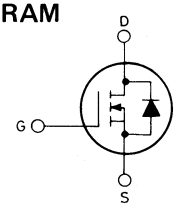
These products are diffused multi-cells silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

ABSOLUTE MAXIMUM RATINGS

		SGSP111	SGSP112
V_{DS}	Drain-source voltage (V_{GS} = 0)	100V	80V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	100V	80V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	5A	
	T_{case} = 100°C	3.2A	
I_{DM}(•)	Drain current (pulsed)	20A	
I_{DLM}	Drain inductive current, clamped	20A	
P_{tot}	Total power dissipation at T_{case} = 25°C	15W	
	Derating factor	0.12W/°C	
T_{stg}	Storage temperature	-55 to 150°C	
T_j	Max. operating junction temperature	150°C	

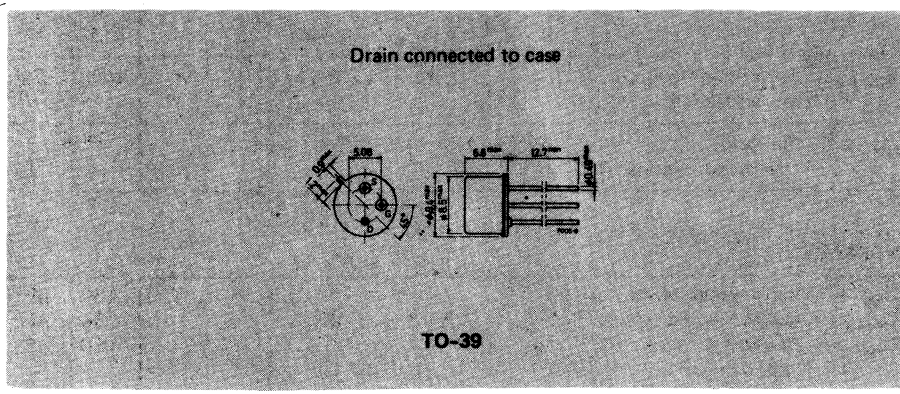
(•) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	8.3 °C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP111** for **SGSP112**	 100 80			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	V_{GS} = 10V I_D = 2.5A I_D = 5A T_C = 100°C I_D = 2.5A			0.75 1.65 1.50	V V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 2.5A			0.3	Ω
g_{fs}	Forward transconductance	V_{DS} = 25A I_D = 2.5A	2			Ʊ
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V f = 1 MHz V_{GS} = 0		375	480 230 110	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

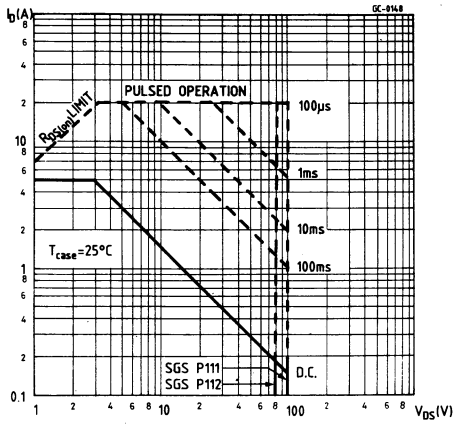
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 25V I_D = 2.5A		35		ns
t_r	Rise time	V_i = 10V R_i = 50Ω		80		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		80		ns
t_f	Fall time			40		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				5	A
I_{SDM}(•)	Source drain current (pulsed)				20	A
V_{SD}	Forward on voltage	I_{SD} = 5A V_{GS} = 0			1.8	V
t_{on}	Turn-on time	I_{SD} = 5A V_{GS} = 0		150		ns
t_{rr}	Reverse recovery	dI/dt = 25A/μs		150	200	ns

* Pulsed: pulse duration = 300μs, duty cycle = 1.5%

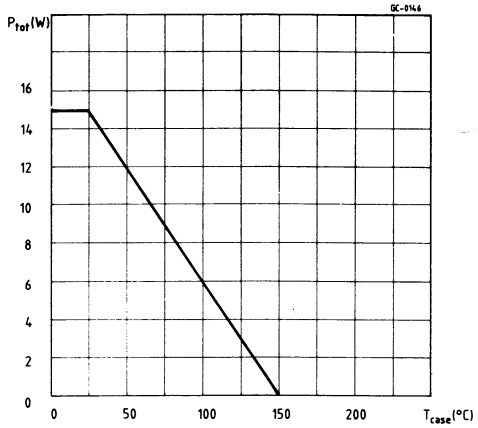
(•) Pulse width limited by safe operating area.

For typical curves switching times resistive load, clamped inductive load, gate charge, body drain diode trr measurament, test circuits see SGSP211 Datasheet.

Safe operating areas



Derating curve



N-CHANNELL POWER MOS TRANSISTORS

SGSP116
SGSP117

PRELIMINARY DATA

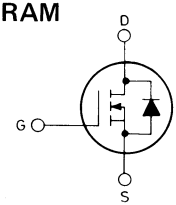
HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cells silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

ABSOLUTE MAXIMUM RATINGS		SGSP116	SGSP117
V_{DS}	Drain-source voltage (V_{GS} = 0)	250V	200V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	250V	200V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	4A	
	T_{case} = 100°C	2.5A	
I_{DM}(•)	Drain current (pulsed)	16A	
I_{DLM}	Drain inductive current, clamped	16A	
P_{tot}	Total power dissipation at T_{case} = 25°C	15W	
	Derating factor	0.12W/°C	
T_{stg}	Storage temperature	-55 to 150°C	
T_j	Max. operating junction temperature	150°C	

(•) Pulse width limited by safe operating area

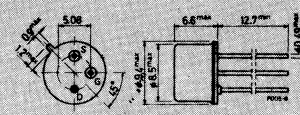
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to case



TO-39

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	8.3 °C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SGSP116** for **SGSP117**	 250 200			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250μA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	V_{GS} = 10V I_D = 2A for **SGSP116** for **SGSP117** V_{GS} = 10V I_D = 4A for **SGSP116** for **SGSP117** V_{GS} = 10V I_D = 2A T_{case} = 100°C for **SGSP116** for **SGSP117**			 2.4 1.5 5.4 3.5 4.8 3.0	 V V V V V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 2A for **SGSP116** for **SGSP117**			 1.20 0.75	 Ω Ω
gfs	Forward transconductance	V_{DS} = 25V I_D = 2A	1.5	3.2		℧

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
DYNAMIC						
C_{iss}	Input capacitance	V_{DS} = 25V f = 1 MHz		380	500	pF
C_{oss}	Output capacitance	V_{GS} = 0		100	130	pF
C_{rss}	Reverse transfer capacitance			50	65	pF
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 100V I_D = 2A		27		ns
t_r	Rise time	V_i = 10V R_i = 50Ω		27		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		30		ns
t_f	Fall time			30		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				4	A
I_{SDM}(•)	Source drain current (pulsed)				16	A
V_{SD}	Forward on voltage	I_{SD} = 4A V_{GS} = 0			1.8	V
t_{on}	Turn-on time	I_{SD} = 4A V_{GS} = 0		100		ns
t_{rr}	Reverse recovery	di/dt = 100A/μs		180		ns

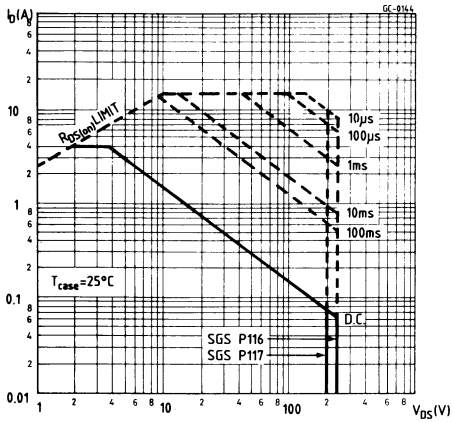
* Pulsed: pulse duration = 300μs, duty cycle = 1.5%

(•) Pulse width limited by safe operating area.

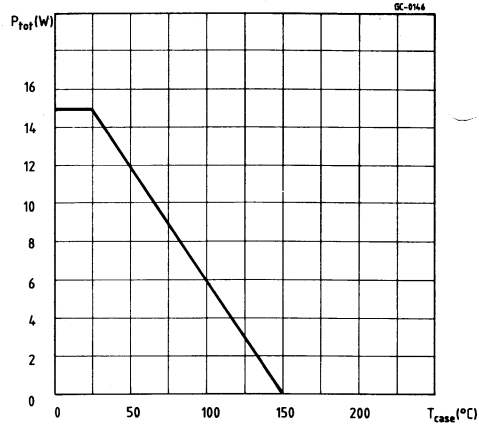
For typical curves and switching times resistive load, clamped inductive load, gate charge, body drain diode trr measurament, test circuits see SGSP216 Datasheet

SGSP116
SGSP117

Safe operating areas



Derating curve



N-CHANNELL POWER MOS TRANSISTORS

SGSP148/P149
SGSP248/P249
SGSP348/P349

ADVANCED DATA

HIGH SPEED SWITCHING APPLICATIONS

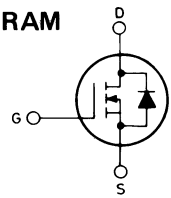
These products are diffused multi-cells silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

ABSOLUTE MAXIMUM RATINGS

		TO-39 SOT-82 TO-220	SGSP148 SGSP248 SGSP348	SGSP149 SGSP249 SGSP349
V_{DS}	Drain-source voltage (V_{GS} = 0)		550V	500V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)		550V	500V
V_{GS}	Gate-source voltage		±20V	
I_D	Drain current (continuous) T_{case} = 25°C		0.5 A	
	at T_{case} = 100°C		0.35A	
I_{DM}(•)	Drain current (pulsed)		2 A	
I_{DLM}	Drain inductive current, clamped		2 A	
		TO-39	SOT-82	TO-220
P_{tot}	Total power dissipation at T_{case} = 25°C	15W	18W	18W
	Derating factor	0.12W°C	0.14W°C	0.14W°C
T_{stg}	Storage temperature		-55 to 150°C	
T_j	Max. operating junction temperature		150°C	

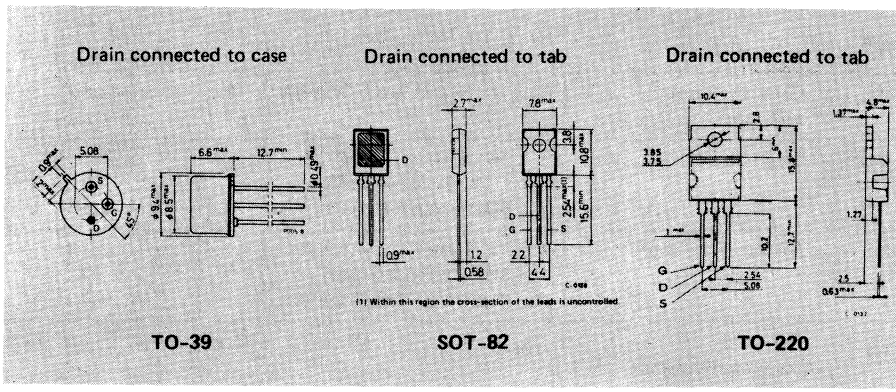
(•) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



THERMAL DATA

			TO-39	SOT-82	TO-220
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	8.3°C/W	6.8°C/W	
T_L	Maximum lead temperature for soldering purpose			275°C	

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP148/248/348** for **SGSP149/249/349**	 550 500			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$V_{DS\ (on)}$	Drain-source	V_{GS} = 10V I_D = 0.25 A for **SGSP148/248/348** for **SGSP149/249/341**			 10 7.5	 V V
$R_{DS\ (on)}$	Static drain-source	V_{GS} = 10 V I_D = 0.3 A for **SGSP148/248/348** for **SGSP149/249/349**			 30 40	 V V
g_{fs}	Forward transconductance	V_{DS} = 25A I_D = 0.3A	0.2			Ʊ

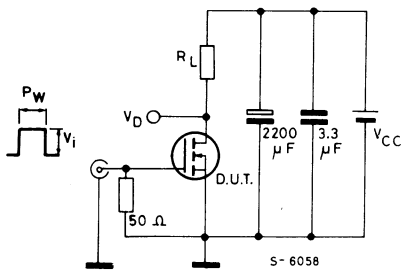
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
DYNAMIC						
C_{iss}	Input capacitance	V_{DS} = 25 V f= 1Mhz		80	105	pF
C_{oss}	Output capacitance	V_{GS} = 0			20	pF
C_{rss}	Reverse transfer capacitance				12	pF
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{CC} = 25V I_D = 0.25A		22		ns
t_r	Rise time	V_I = 10 V R_I = 50Ω		10		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		35		ns
t_f	Fall time			8		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				0.5	A
I_{SDM}(•)	Source drain current (pulsed)				2	A
V_{SD}	Forward on voltage	I_{SD} = 0.5A V_{GS} = 0			1.8	V
t_{on}	Turn-on time	I_{SD} = 5A V_{GS} = 0		24		ns
t_{rr}	Reverse recovery	dI/dt = 25 A/μs		30		ns

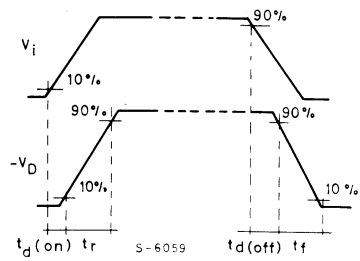
* Pulsed: pulse duration = 300μs, duty cycle = 1.5%
(•) Pulse width limited by safe operating area.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



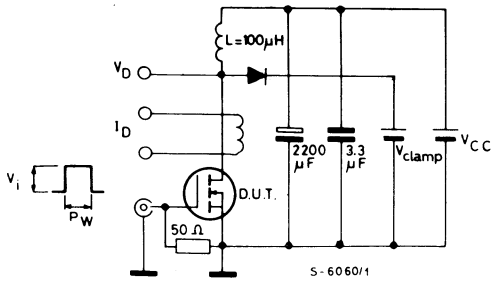
Waveforms



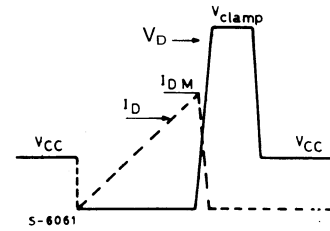
Pulse width ≤ 100 μs
Duty cycle ≤ 2%
V_i = 10V

CLAMPED INDUCTIVE LOAD

Test circuit



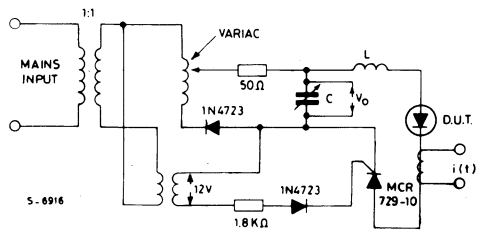
Waveforms



V_i = 12V

Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$

DIODE BODY-DRAIN t_{rr} MEASUREMENT



Jedec test circuit