N-CHANNEL POWER MOS TRANSISTORS

SGSP154/5/6
SGSP254/5/6
SGSP354/5/6

HIGH SPEED SWITCHING APPLICATIONS

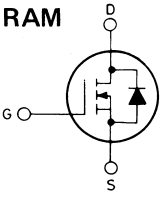
These products are diffused multi-cells silicon gate N-Channel enhancement mode Power Mos field effect transistors.

ABSOLUTE MAXIMUM RATINGS

		TO-39 / SOT-82 / TO-220	SGSP154 / SGSP254 / SGSP354	SGSP155 / SGSP255 / SGSP355	SGSP156 / SGSP256 / SGSP356
V_{DS}	Drain-source voltage ($V_{GS} = 0$)		450V	400V	350V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)		450V	400V	350V
V_{GS}	Gate-source voltage			± 20V	
I_D	Drain current (continuous) $T_{case} = 25°C$			1.5A	
	$T_{case} = 100°C$			1A	
I_{DM} (●)	Drain current (pulsed)			6A	
I_{DLM}	Drain inductive current, clamped			6A	
			TO-39	SOT-82	TO-220
P_{tot}	Total power dissipation at $T_{amb} = 25°C$		50W	40W	15W
	Derating factor		0.4W/°C	0.32W/°C	0.12W/°C
T_{stg}	Storage temperature			-55 to 150°C	
T_j	Junction temperature			150°C	

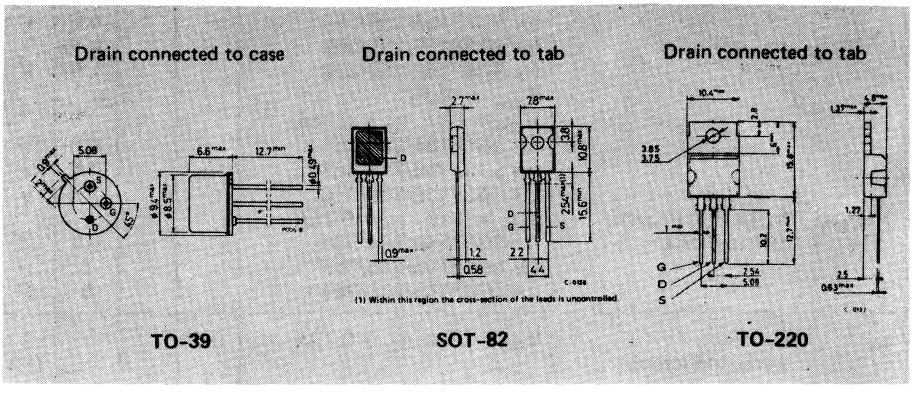
(●) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



THERMAL DATA

		TO-39	SOT-82	TO-220
$R_{th\ j\text{-}case}$	Thermal resistance junction-case max	8.3°C/W	2.5°C/W	3.12°C/W
T_L	Maximum lead temperature for soldering purpose		275°C	

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0				
		for **SGSP154/254/354**	450			V
		for **SGSP155/255/355**	400			V
		for **SGSP156/256/356**	350			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	V_{GS} = 10V I_D = 0.75A				
		for **SGSP154/254/354**			4.9	V
		for **SGSP155/255/355**			3.75	V
		for **SGSP156/256/356**			3.75	V
		T_{case} = 100°C				
		V_{GS} = 10V I_D = 0.75A				
		for **SGSP154/254/354**			9.8	V
		for **SGSP155/255/355**			7.5	V
		for **SGSP156/256/356**			7.5	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 0.75A				
		for **SGSP154/254/354**			6.5	Ω
		for **SGSP155/255/355**			5	Ω
		for **SGSP156/256/356**			5	Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 0.75A	0.85			S (℧)

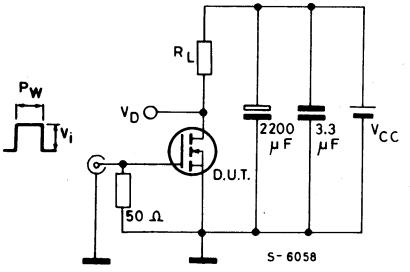
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
DYNAMIC						
C_{lss}	Input capacitance	V_{DS} = 25V f = 1MHz		180	250	pF
C_{oss}	Output capacitance	V_{GS} = 0		30	45	pF
C_{rss}	Reverse transfer			15	25	pF
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 25V V_G = 10V		60		ns
t_r	Rise time	I_D = 0.75A R_i = 50Ω		60		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		60		ns
t_f	Fall time			80		ns
SOURCE DRAIN DIODE						
I_{SD}	Source-drain current				1.5	A
I_{SDM} (●)	Source-drain current (pulsed)				6	A
V_{SD}	Forward on voltage	I_{SD} = 1.5A V_{GS} = 0			1.2	V
t_{on}	Turn-on time	I_{SD} = 1.5A V_{GS} = 0		100		ns
t_{rr}	Reverse recovery time	dI/dt = 25A/μs		70		ns

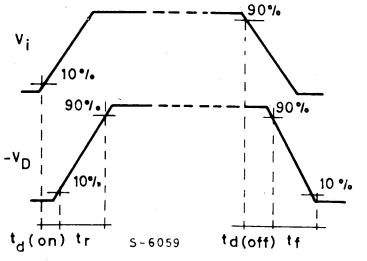
* Pulsed: pulse duration < 300μs, duty cycle < 2%
(●) Pulse width limited by safe operating area

SWITCHING TIMES RESISTIVE LOAD

Test circuit



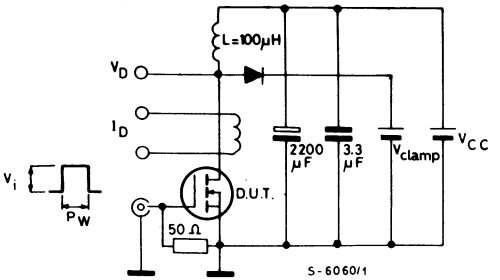
Waveforms



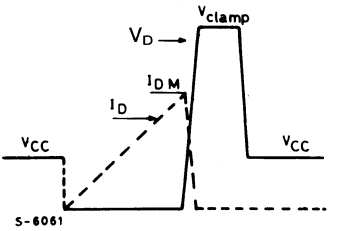
Pulse width ≤ 100 μs
Duty cycle ≤ 2%
V_i = 10V

CLAMPED INDUCTIVE LOAD

Test circuit



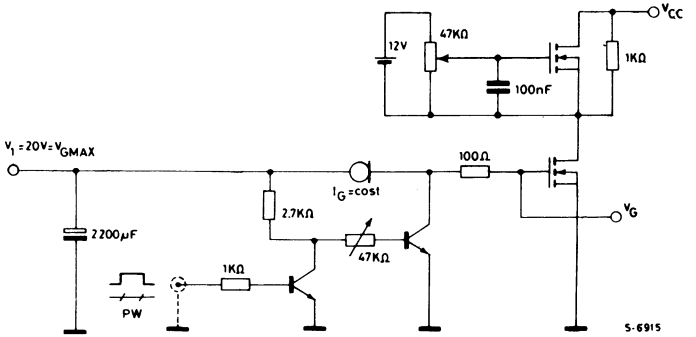
Waveforms



V_i = 12V

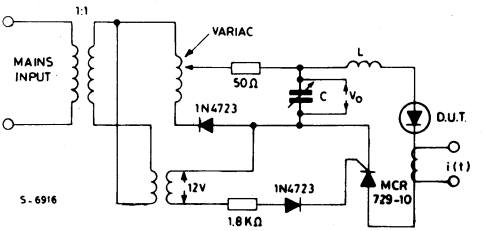
Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$

GATE CHARGE TEST CIRCUIT



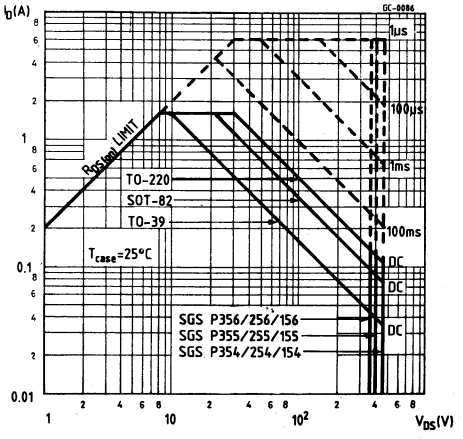
PW adjusted to obtain required V_G

DIODE BODY-DRAIN t_{rr} MEASUREMENT

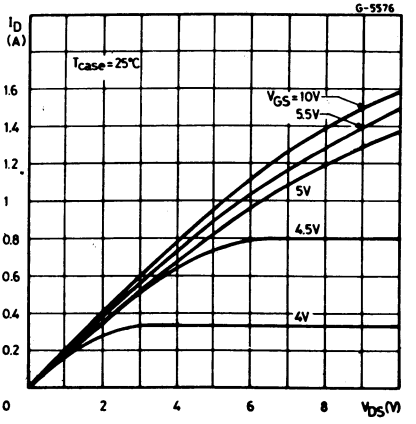


Jedec test circuit

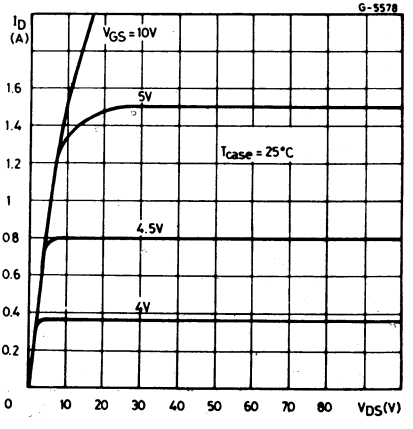
Safe operating areas



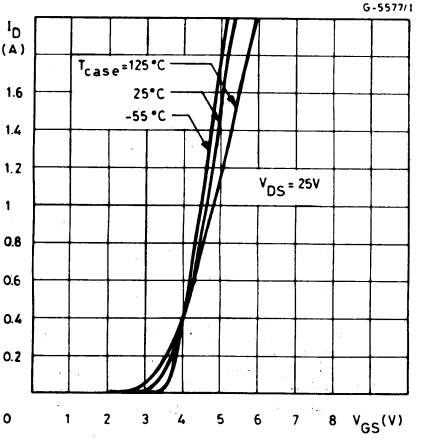
Output characteristics



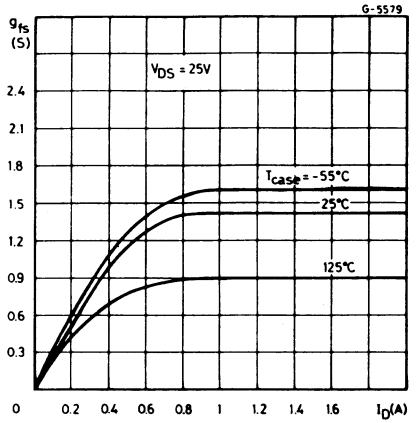
Output characteristics



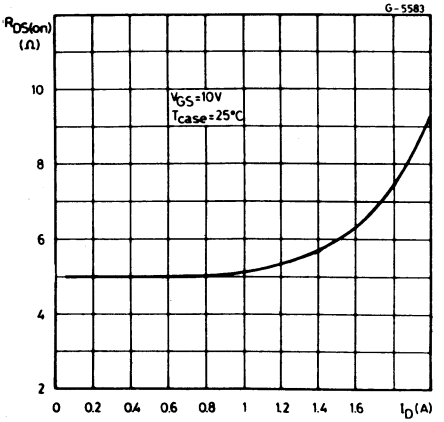
Transfer characteristics



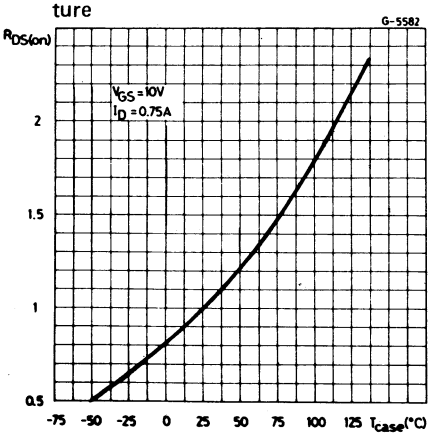
Transconductance



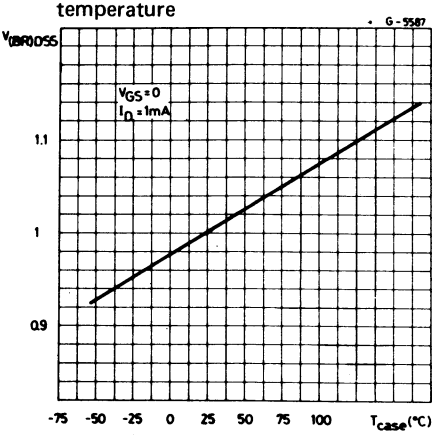
Static drain-source on resistance



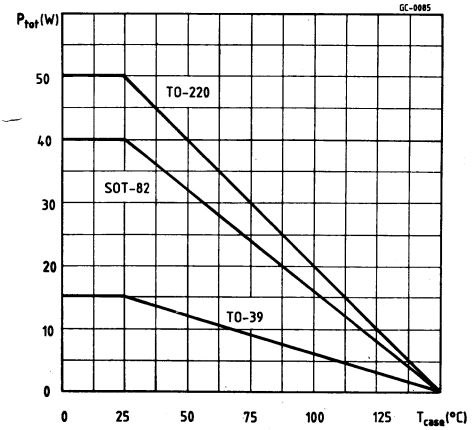
Normalized on resistance vs. temperature



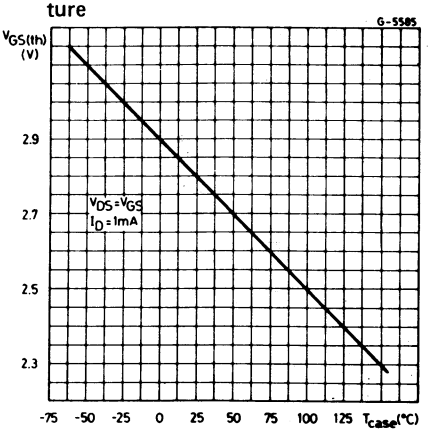
Normalized breakdown voltage vs. temperature



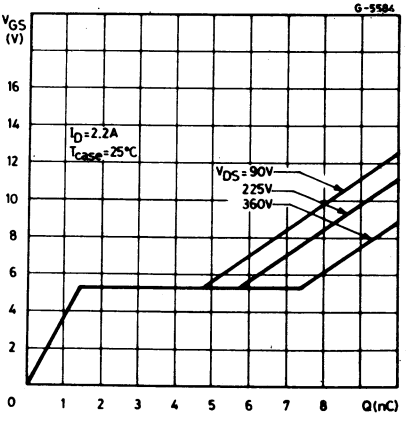
Derating curve



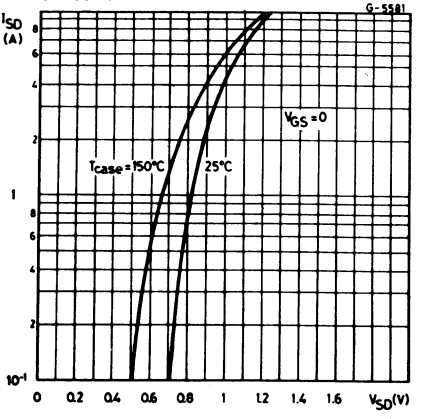
Gate threshold voltage vs. temperature



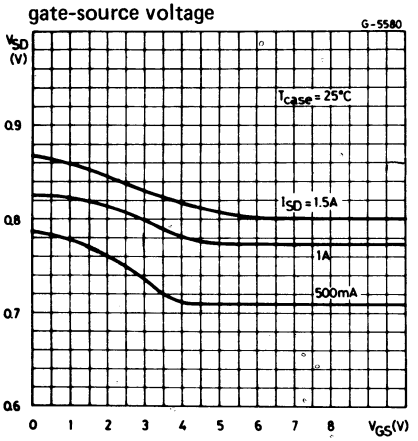
Gate charge vs. gate-source voltage



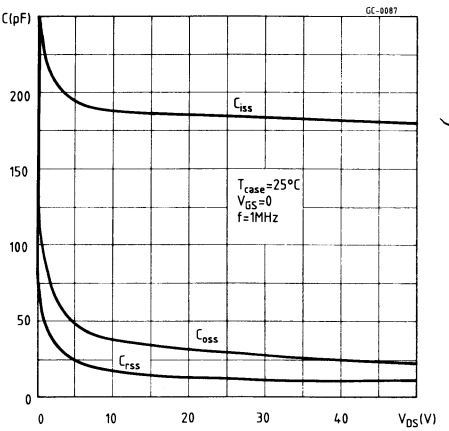
Source-drain diode forward characteristics



Source-drain diode forward voltage vs. gate-source voltage



Capacitance variation



N-CHANNELL POWER MOS TRANSISTORS

SGSP157
SGSP158

PRELIMINARY DATA

HIGH SPEED SWITCHING APPLICATIONS

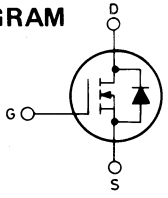
These products are diffused multi-cells silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

ABSOLUTE MAXIMUM RATINGS

		SGSP157	SGSP158
V_{DS}	Drain-source voltage (V_{GS} = 0)	60V	50V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	60V	50V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	5A	
	T_{case} = 100°C	3.2A	
I_{DM}(•)	Drain current (pulsed)	20A	
I_{DLM}	Drain inductive current, clamped	20A	
P_{tot}	Total power dissipation at T_{case} = 25°C	15W	
	Derating factor	0.12W/°C	
T_{stg}	Storage temperature	-55 to 150°C	
T_j	Max. operating junction temperature	150°C	

(•) Pulse width limited by safe operating area

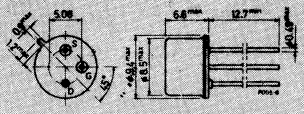
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to case



TO-39

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	8.3	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SGSP157** for **SGSP158**	 60 50			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	V_{GS} = 10V I_D = 2.5A I_D = 5A T_C = 100°C I_D = 2.5A			0.75 1.65 1.50	V V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 2.5A			0.3	Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 2.5A	1.5			℧
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V f = 1 MHz V_{GS} = 0		210 115 54	270 150 70	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

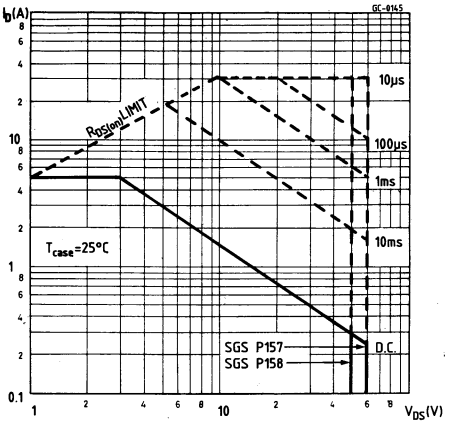
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 25V I_D = 2.5A		10		ns
t_r	Rise time	V_i = 10V R_i = 4.7 Ω		25		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		15		ns
t_f	Fall time			10		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				5	A
I_{SDM}(•)	Source drain current (pulsed)				20	A
V_{SD}	Forward on voltage	I_{SD} = 5A V_{GS} = 0			1.80	V
t_{on}	Turn-on time	I_{SD} = 5A V_{GS} = 0		90		ns
t_{rr}	Reverse recovery	di/dt = 25A/μs		120		ns

* Pulsed: pulse duration = 300μs, duty cycle = 1.5%

(•) Pulse width limited by safe operating area.

For typical curves and switching times resistive load, clamped inductive load, gate cherge, body drain diode trr measurament test circuits, see SGSP257 Datasheet.

Safe operating areas



Derating curve