Siliconix incorporated

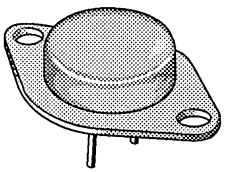
MOSPOWER

SMM20N50

N-Channel Enhancement Mode Transistor

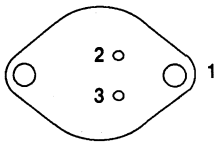
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SMM20N50	500	0.30	20



TO-204AE (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SMM20N50	Units
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	20	A
	T_C = 100°C		12.5	
Pulsed Drain Current[1]		I_{DM}	80	
Avalanche Current (see figure 9)		I_A	20	
Power Dissipation	T_C = 25°C	P_D	250	W
	T_C = 100°C		100	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	0.50	K/W
Junction-to-Ambient	R_{thJA}	-	30	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA		$V_{(BR)DSS}$	500	–	–	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1000 µA		$V_{GS(th)}$	2.0	2.6	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	–	–	1000	
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	20	–	–	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 10 A		$r_{DS(on)}$	–	0.26	0.30	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 10 A, T_J = 125°C		$r_{DS(on)}$	–	0.52	0.70	
Forward Transconductance[2] V_{DS} =15 V, I_D = 10 A		g_{fs}	8.0	11	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{lss}	–	3800	4500	pF
Output Capacitance		C_{oss}	–	750	1000	
Reverse Transfer Capacitance		C_{rss}	–	350	500	
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 20 A (Gate charge is essentially independent of operating temperature)	Q_g	–	70	100	nC
Gate-Source Charge		Q_{gs}	–	15	–	
Gate-Drain Charge		Q_{gd}	–	34	–	
Turn-On Delay Time	V_{DD} = 250 V, R_L = 25 Ω I_D = 10 A, V_{GEN} = 10 V R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	34	45	ns
Rise Time		t_r	–	57	70	
Turn-Off Delay Time		$t_{d(off)}$	–	120	150	
Fall Time		t_f	–	62	75	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	–	–	20	A
Pulsed Current[1]	I_{SM}	–	–	110	
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	–	–	1.6	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs	t_{rr}	–	300	650	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs	Q_{rr}	–	2.0	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

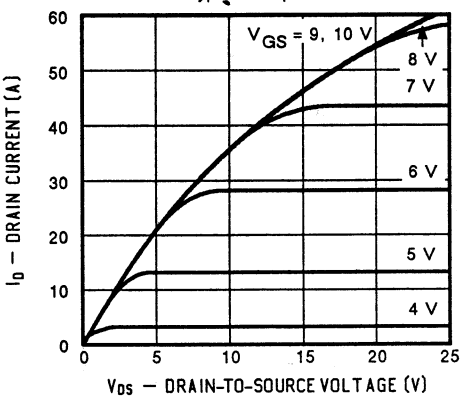


FIGURE 2: Typical Transfer Characteristics

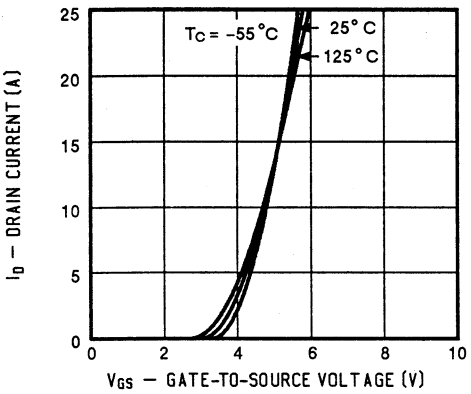


FIGURE 3: Typical Transconductance

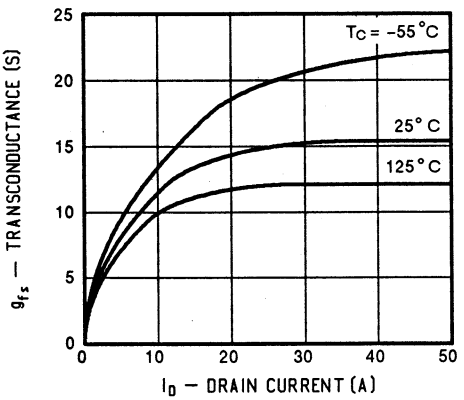


FIGURE 4: Typical On-Resistance

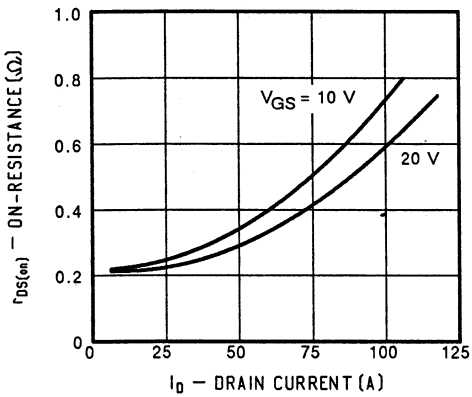


FIGURE 5: Typical Capacitance

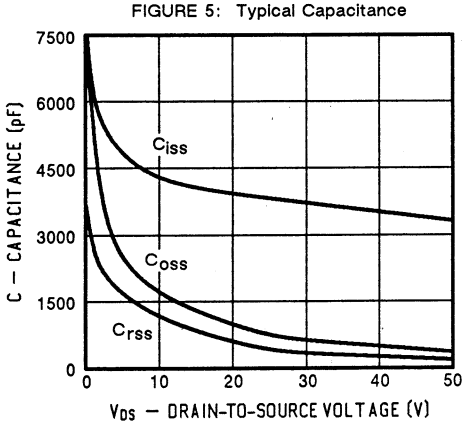
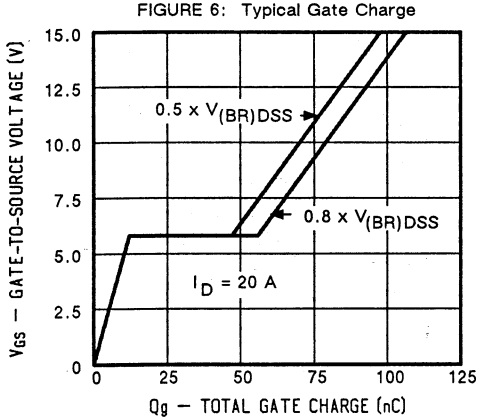


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

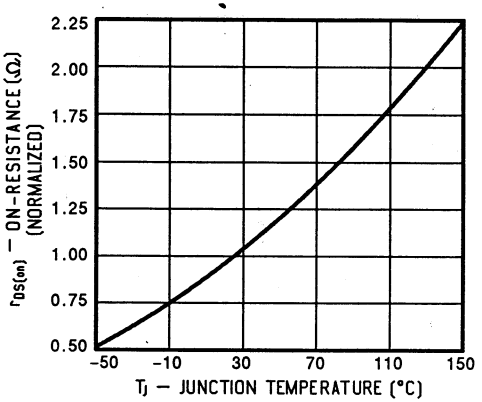


FIGURE 8: Typical Source-Drain Diode Forward Voltage

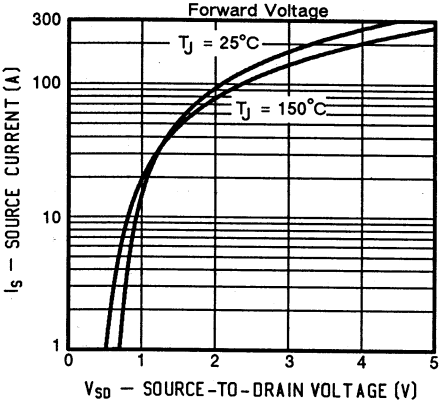


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

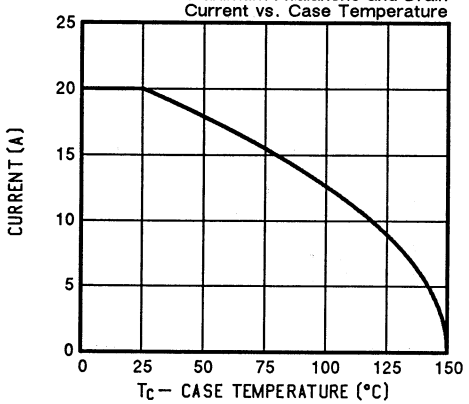
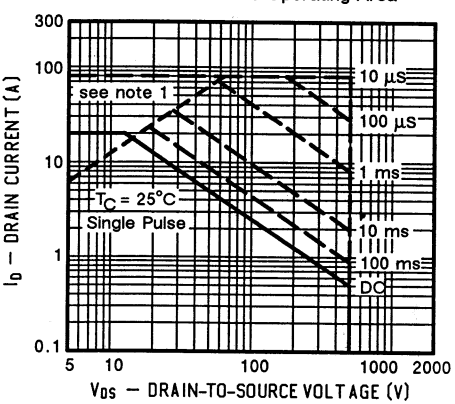
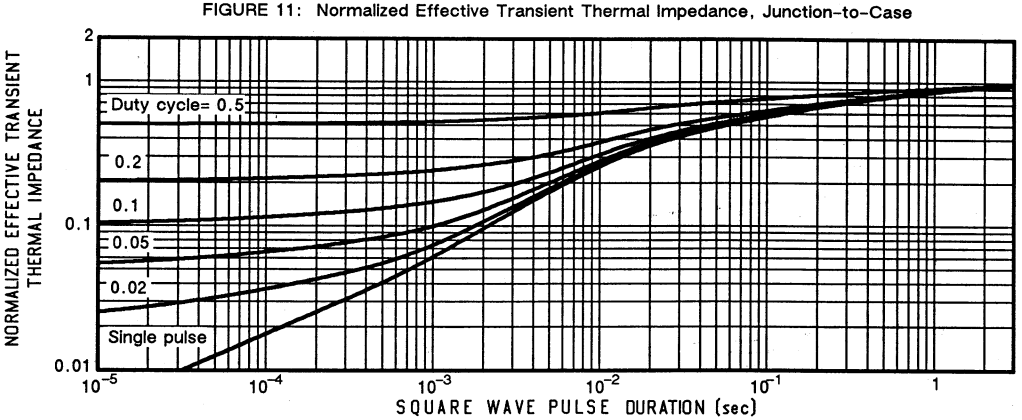


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

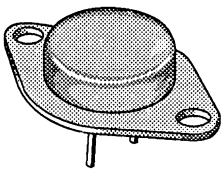
MOSPOWER

SMM20P10
SMM16P06

P-Channel Enhancement Mode Transistors[2]

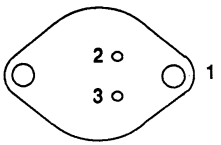
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SMM20P10	100	0.20	20
SMM16P06	60	0.30	16



TO-204AA (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SMM 20P10	SMM 16P06	Units
Drain-Source Voltage		V_{DS}	100	60	V
Gate-Source Voltage		V_{GS}	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	20	16	A
	T_C = 100°C	I_D	13	11	A
Pulsed Drain Current[1]		I_{DM}	80	64	A
Avalanche Current (see figure 9)		I_A	20	16	A
Power Dissipation	T_C = 25°C	P_D	125	125	W
	T_C = 100°C	P_D	50	50	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.0	K/W
Junction-to-Ambient	R_{thJA}	-	30	K/W
Case-to-Sink	R_{thCS}	0.1	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) P-Channel Device

Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	SMM20P10 SMM16P06	$V_{(BR)DSS}$	100 60	– –	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	–	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	SMM20P10 SMM16P06	$I_{D(on)}$	20 16	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 10 A	SMM20P10 SMM16P06	$r_{DS(on)}$	– –	0.15 0.19	0.20 0.30	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 10 A, T_J = 125°C	SMM20P10 SMM16P06	$r_{DS(on)}$	– –	0.24 0.30	0.36 0.54	
Forward Transconductance[2] V_{DS} = 10 V, I_D = 10 A		g_{fs}	4.8	6.7	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	1300	1600	pF
Output Capacitance		C_{oss}	–	750	850	
Reverse Transfer Capacitance		C_{rss}	–	310	400	
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 20 A (Gate charge is essentially independent of operating temperature)	Q_g	–	47	60	nC
Gate-Source Charge		Q_{gs}	–	10	–	
Gate-Drain Charge		Q_{gd}	–	27	–	
Turn-On Delay Time	V_{DD} = 40 V, R_L = 4.0 Ω I_D ≅ 10 A, V_{GEN} = 10 V R_G = 4.7Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	10	30	ns
Rise Time		t_r	–	50	80	
Turn-Off Delay Time		$t_{d(off)}$	–	25	80	
Fall Time		t_f	–	15	60	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	SMM20P10 SMM16P06	I_S	– –	– –	20 16	A
Pulsed Current[1]	SMM20P10 SMM16P06	I_{SM}	– –	– –	80 64	
Forward Voltage[2] I_F = I_S, V_{GS} = 0	SMM20P10 SMM16P06	V_{SD}	– –	– –	1.7 1.6	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs		t_{rr}	–	150	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs		Q_{rr}	–	0.3	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

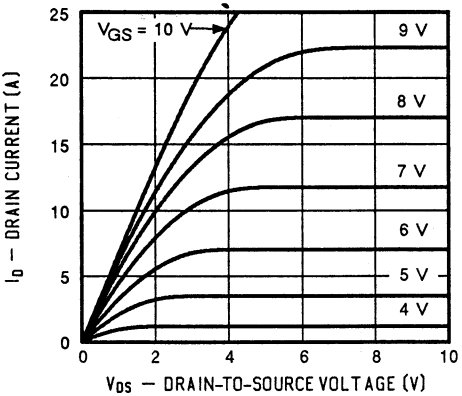


FIGURE 2: Typical Transfer Characteristics

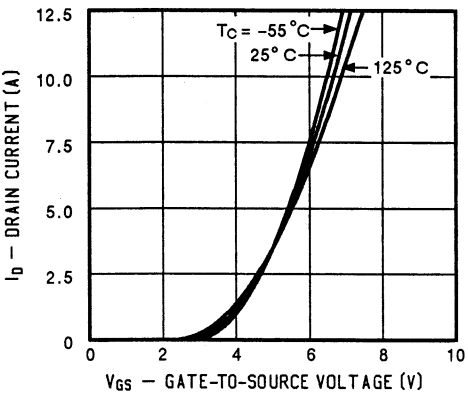


FIGURE 3: Typical Transconductance

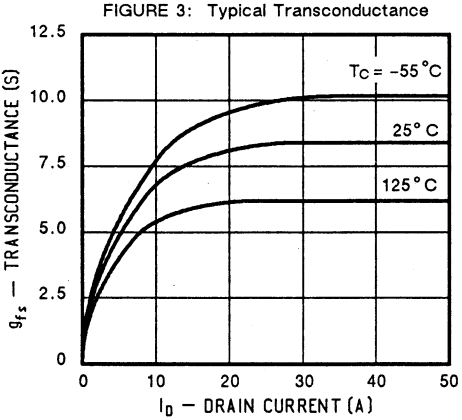


FIGURE 4: Typical On-Resistance

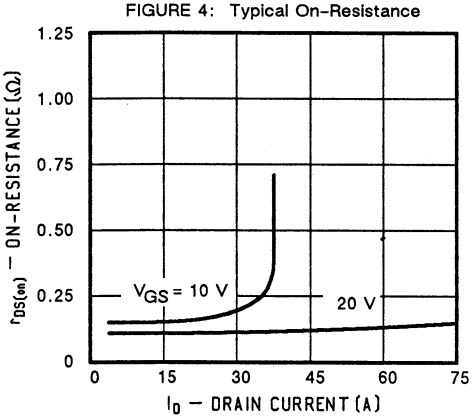


FIGURE 5: Typical Capacitance

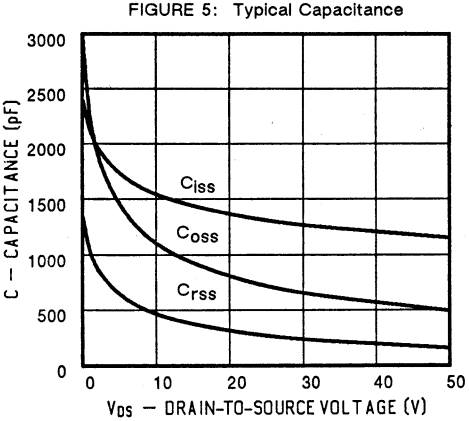
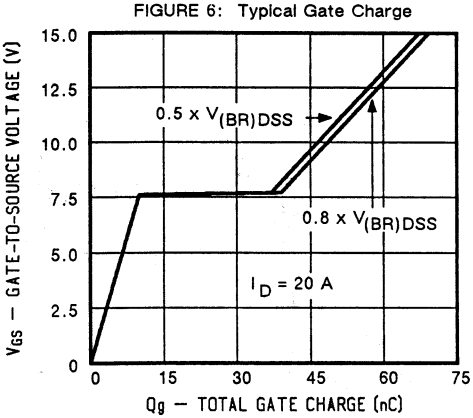


FIGURE 6: Typical Gate Charge



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Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

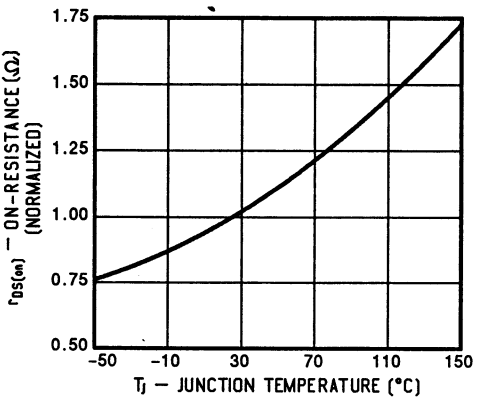


FIGURE 8: Typical Source-Drain Diode Forward Voltage

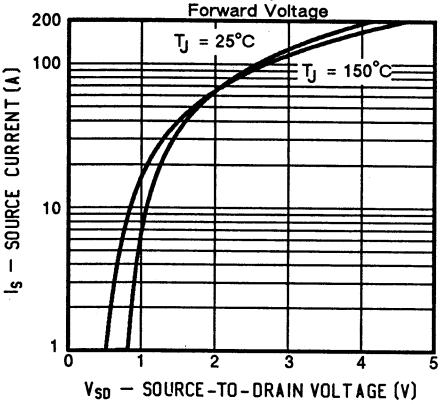


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

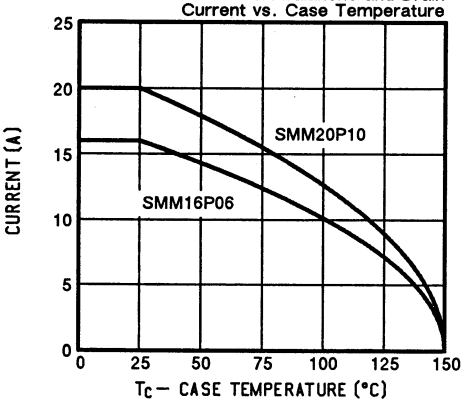
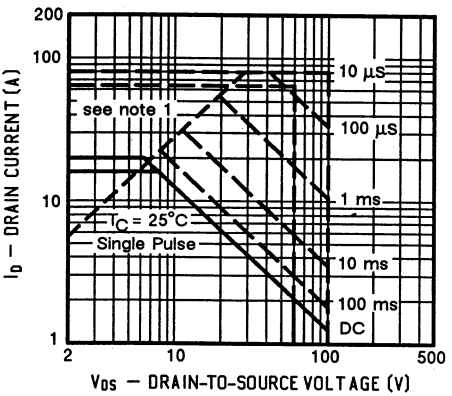


FIGURE 10: Safe Operating Area



[1] Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case