Siliconix incorporated

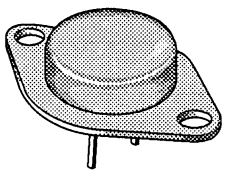
SMM24N40

N-Channel Enhancement Mode Transistor

MOSPOWER

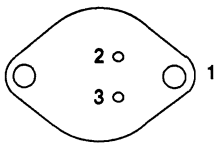
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SMM24N40	400	0.23	24



TO-204AE (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SMM24N40	Units
Drain-Source Voltage		V_{DS}	400	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	24	A
	T_C = 100°C		15	
Pulsed Drain Current[1]		I_{DM}	96	
Avalanche Current (see figure 9)		I_A	24	
Power Dissipation	T_C = 25°C	P_D	250	W
	T_C = 100°C		100	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	0.50	K/W
Junction-to-Ambient	R_{thJA}	-	30	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		$V_{(BR)DSS}$	400	–	–	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1000 μA		$V_{GS(th)}$	2.0	2.6	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	–	–	1000	
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	24	–	–	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 12 A		$r_{DS(on)}$	–	0.16	0.23	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 12 A, T_J = 125°C		$r_{DS(on)}$	–	0.32	0.41	
Forward Transconductance[2] V_{DS} =15 V, I_D = 12 A		g_{fs}	8.0	12.5	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	3800	4500	pF
Output Capacitance		C_{oss}	–	800	1000	
Reverse Transfer Capacitance		C_{rss}	–	400	500	
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 24 A (Gate charge is essentially independent of operating temperature)	Q_g	–	75	100	nC
Gate-Source Charge		Q_{gs}	–	15	–	
Gate-Drain Charge		Q_{gd}	–	38	–	
Turn-On Delay Time	V_{DD} = 200 V, R_L = 16 Ω I_D = 12 A, V_{GEN} = 10 V R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	34	45	ns
Rise Time		t_r	–	60	85	
Turn-Off Delay Time		$t_{d(off)}$	–	125	160	
Fall Time		t_f	–	70	80	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	–	–	24	A
Pulsed Current[1]	I_{SM}	–	–	96	
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	–	–	2.0	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μs	t_{rr}	–	300	650	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μs	Q_{rr}	–	2.0	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

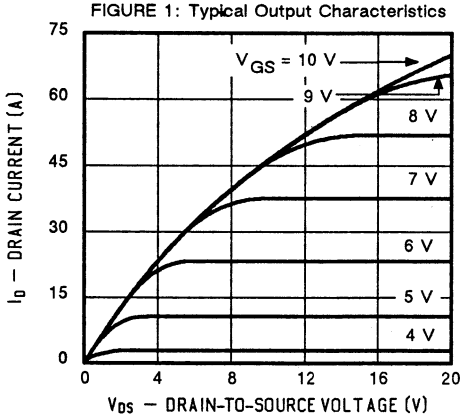


FIGURE 2: Typical Transfer Characteristics

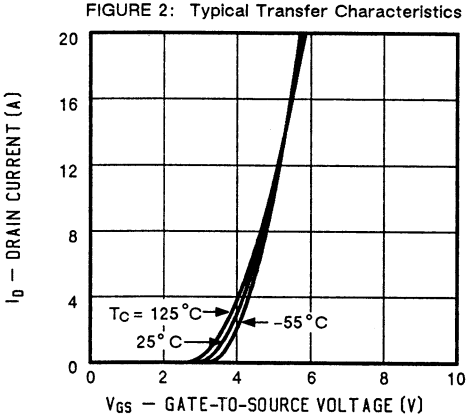


FIGURE 3: Typical Transconductance

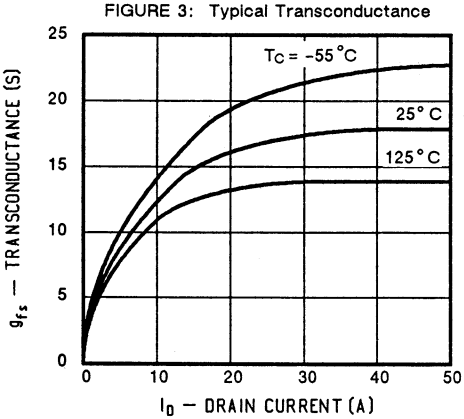


FIGURE 4: Typical On-Resistance

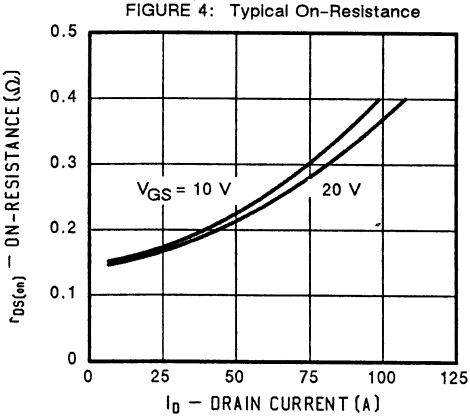


FIGURE 5: Typical Capacitance

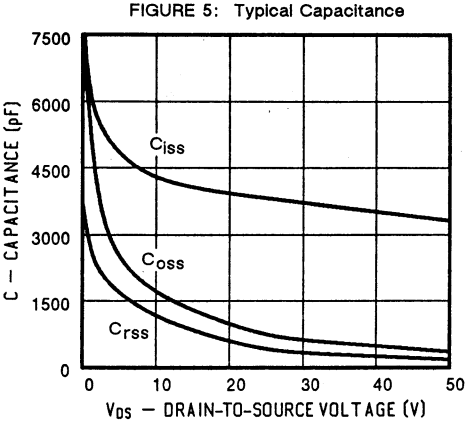
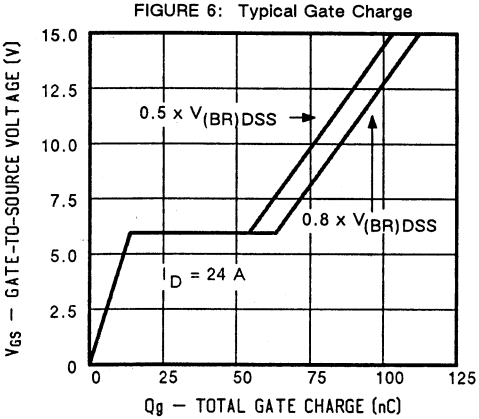


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

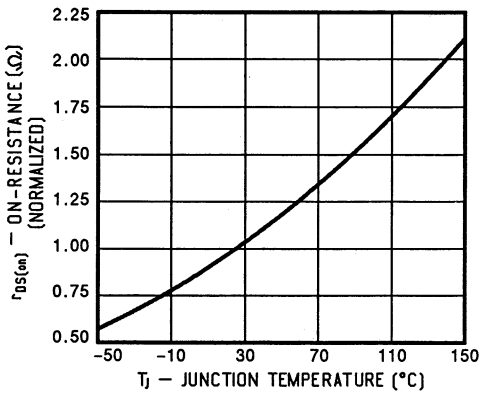


FIGURE 8: Typical Source-Drain Diode Forward Voltage

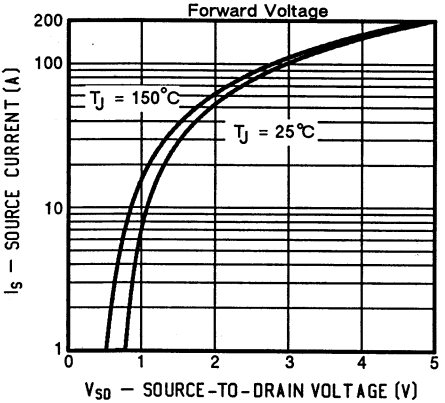


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

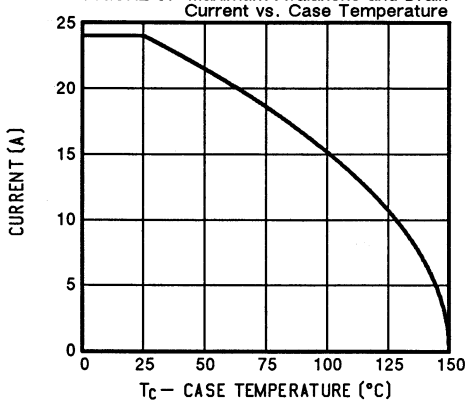
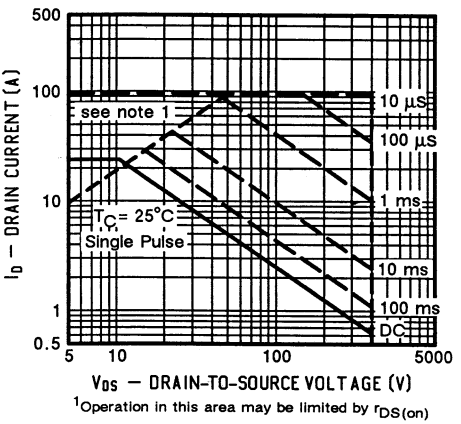
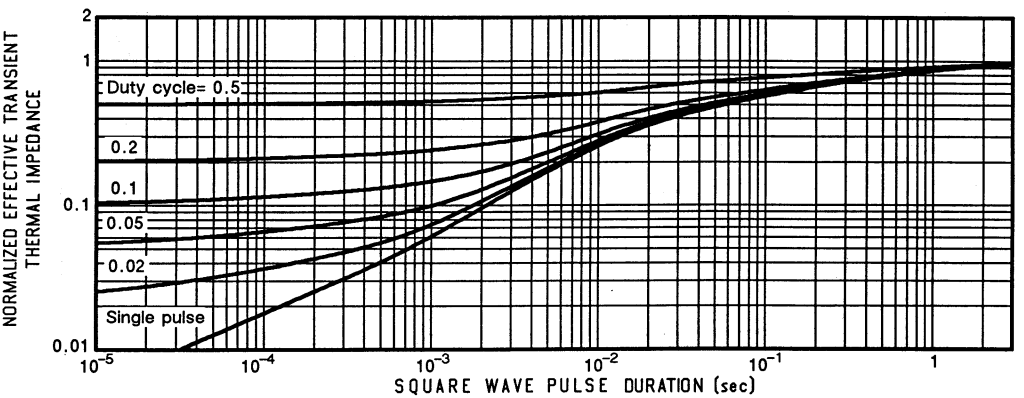


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

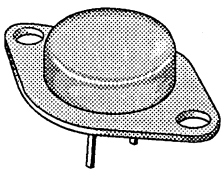
MOSPOWER

SMM40N20

N-Channel Enhancement Mode Transistor

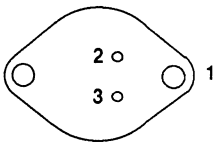
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SMM40N20	200	0.060	40



TO-204AE (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SMM40N20	Units
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	40	A
	T_C = 100°C		28	
Pulsed Drain Current[1]		I_{DM}	160	
Avalanche Current (see figure 9)		I_A	40	
Power Dissipation	T_C = 25°C	P_D	250	W
	T_C = 100°C		100	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

4

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	0.50	K/W
Junction-to-Ambient	R_{thJA}	-	30	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA		$V_{(BR)DSS}$	200	–	–	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	–	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	–	–	1000	
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	40	–	–	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 20 A		$r_{DS(on)}$	–	0.05	0.060	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 20 A, T_J = 125°C		$r_{DS(on)}$	–	0.10	0.14	
Forward Transconductance[2] V_{DS} =20 V, I_D = 20 A		g_{fs}	8.0	17	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	4200	4500	pF
Output Capacitance		C_{oss}	–	1000	1500	
Reverse Transfer Capacitance		C_{rss}	–	400	600	
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 40 A (Gate charge is essentially independent of operating temperature)	Q_g	–	82	100	nC
Gate-Source Charge		Q_{gs}	–	18	–	
Gate-Drain Charge		Q_{gd}	–	39	–	
Turn-On Delay Time	V_{DD} = 100 V, R_L = 5Ω I_D ≅ 20 A, V_{GEN} = 10 V R_G = 4.7Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	20	45	ns
Rise Time		t_r	–	55	85	
Turn-Off Delay Time		$t_{d(off)}$	–	60	150	
Fall Time		t_f	–	25	80	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	–	–	40	A
Pulsed Current[1]	I_{SM}	–	–	160	
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	–	–	2.0	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs	t_{rr}	–	250	650	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs	Q_{rr}	–	2.4	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

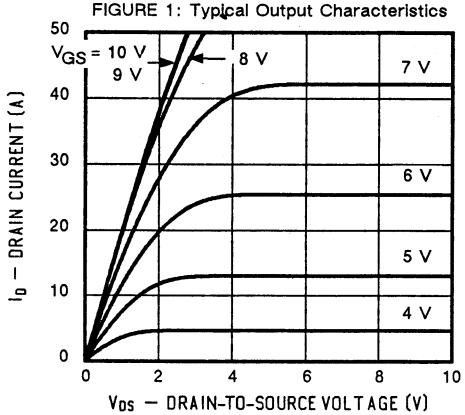


FIGURE 2: Typical Transfer Characteristics

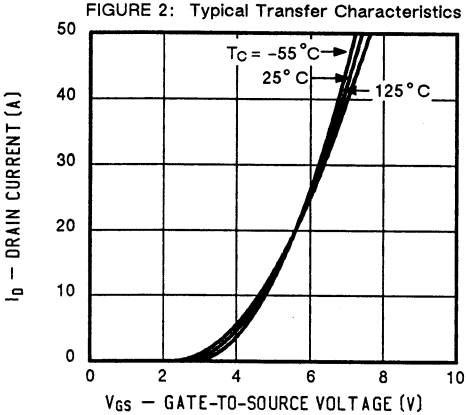


FIGURE 3: Typical Transconductance

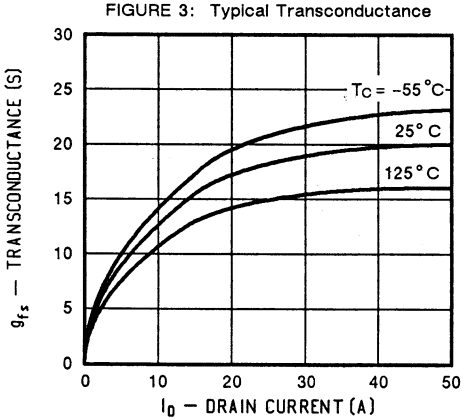


FIGURE 4: Typical On-Resistance

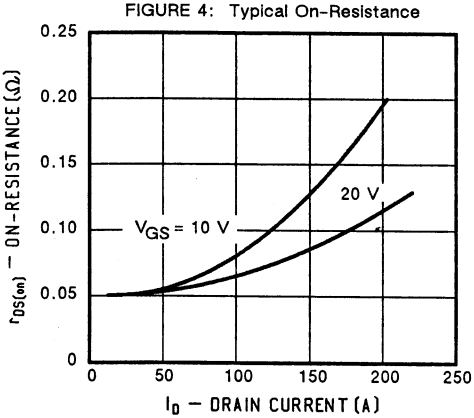


FIGURE 5: Typical Capacitance

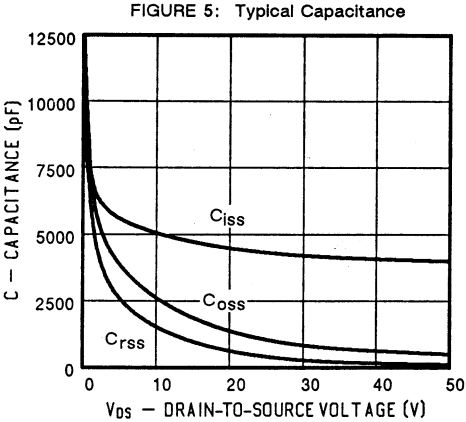
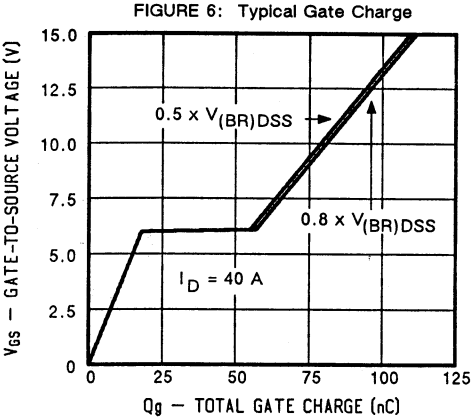


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

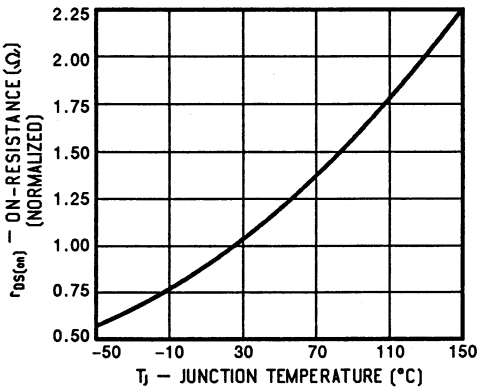


FIGURE 8: Typical Source-Drain Diode Forward Voltage

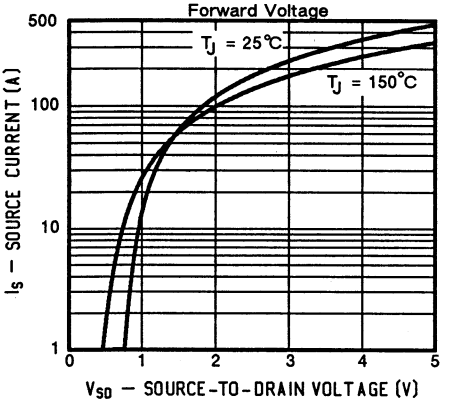


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

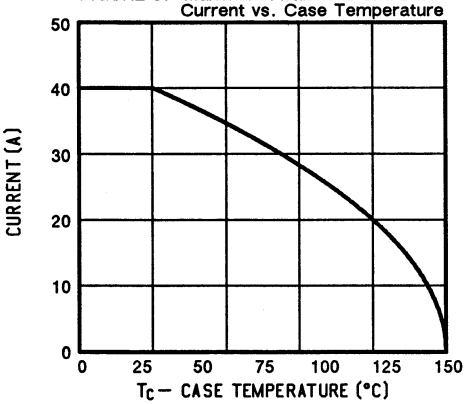
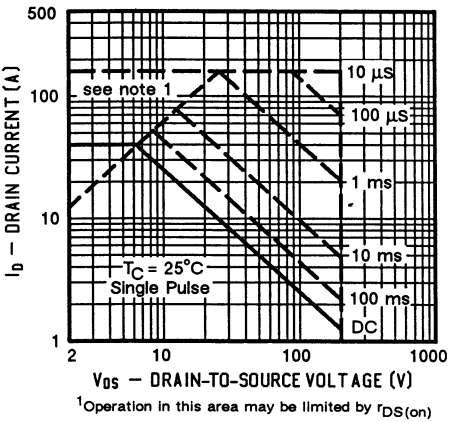
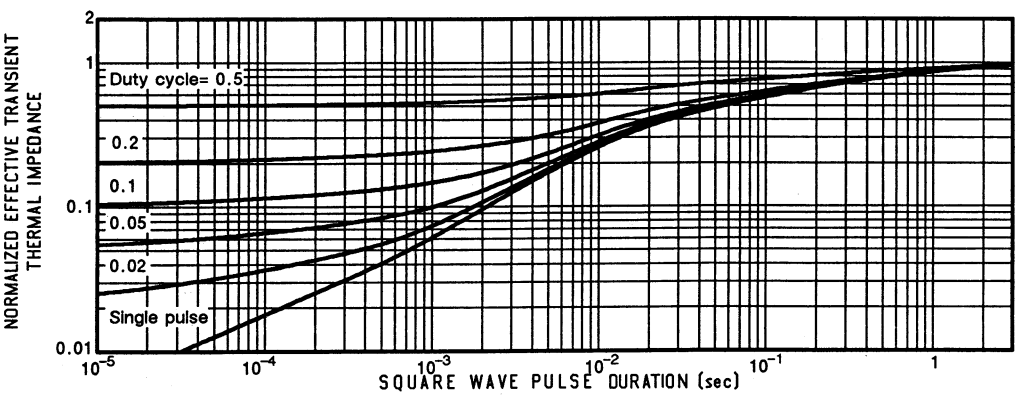


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

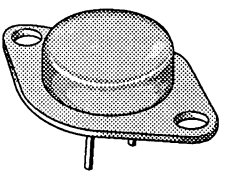
MOSPOWER

SMM60N06
SMM60N05

N-Channel Enhancement Mode Transistors

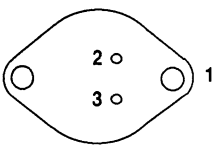
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SMM60N06	60	0.023	60
SMM60N05	50	0.023	60



TO-204AE (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SMM		Units
			60N06	60N05	
Drain-Source Voltage		V_{DS}	60	50	V
Gate-Source Voltage		V_{GS}	±40	±40	V
Continuous Drain Current	T_C = 25°C	I_D	60	60	A
	T_C = 100°C		36	36	A
Pulsed Drain Current[1]		I_{DM}	240	240	A
Power Dissipation	T_C = 25°C	P_D	150	150	W
	T_C = 100°C		60	60	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	0.83	K/W
Junction-to-Ambient	R_{thJA}	-	30	K/W
Case-to-Sink	R_{thCS}	0.1	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	SMM60N06 SMM60N05	$V_{(BR)DSS}$	60 50	65 55	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1000 μA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	μA
On-State Drain Current[2] V_{DS} = 2.0 V, V_{GS} = 10 V		$I_{D(on)}$	60	–	–	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 30 A		$r_{DS(on)}$	–	0.019	0.023	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 30 A, T_J = 125°C		$r_{DS(on)}$	–	0.025	0.032	Ω
Forward Transconductance[2] V_{DS} = 25 V, I_D = 30 A		g_{fs}	15	18	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	2900	3500	pF
Output Capacitance		C_{oss}	–	1500	1600	pF
Reverse Transfer Capacitance		C_{rss}	–	500	600	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 60 A (Gate charge is essentially independent of operating temperature)	Q_g	–	65	75	nC
Gate-Source Charge		Q_{gs}	–	15	–	nC
Gate-Drain Charge		Q_{gd}	–	35	–	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 1.0Ω I_D ≅ 30 A, V_{GEN} = 10 V R_G = 2.5Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	20	40	ns
Rise Time		t_r	–	25	50	ns
Turn-Off Delay Time		$t_{d(off)}$	–	30	60	ns
Fall Time		t_f	–	20	40	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	–	–	60	A
Pulsed Current[1]	I_{SM}	–	–	240	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	–	–	2.5	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μS	t_{rr}	–	75	100	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μS	Q_{rr}	–	0.19	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

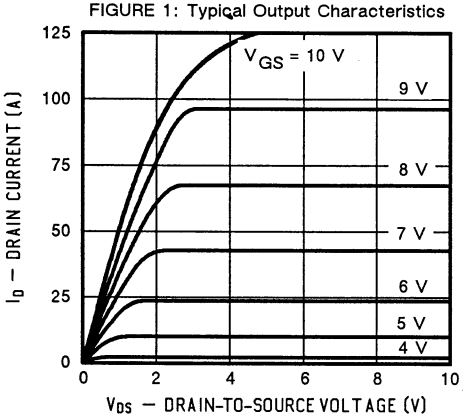


FIGURE 2: Typical Transfer Characteristics

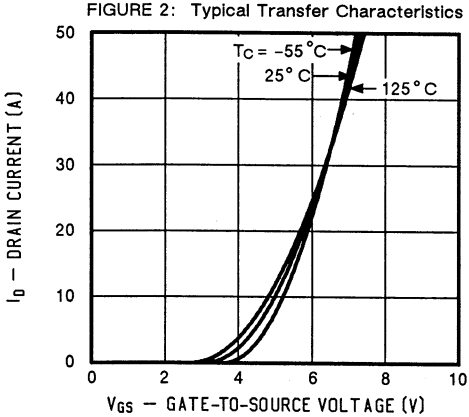


FIGURE 3: Typical Transconductance

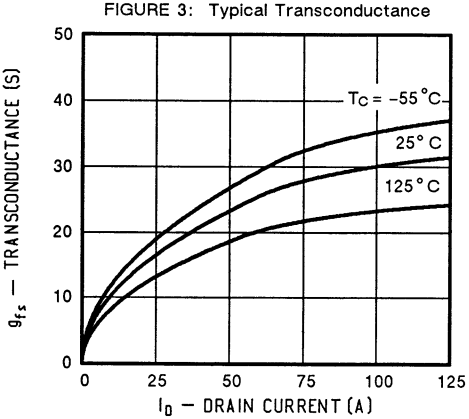


FIGURE 4: Typical On-Resistance

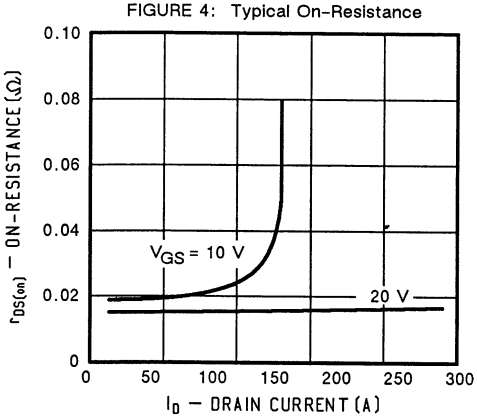


FIGURE 5: Typical Capacitance

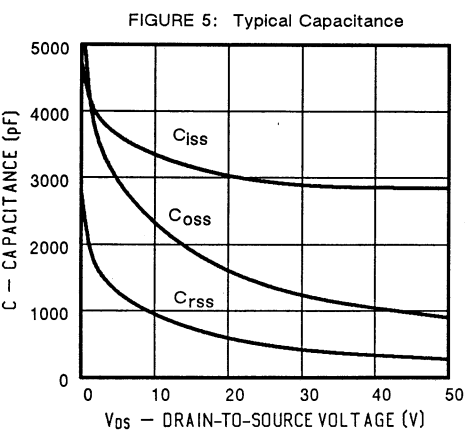
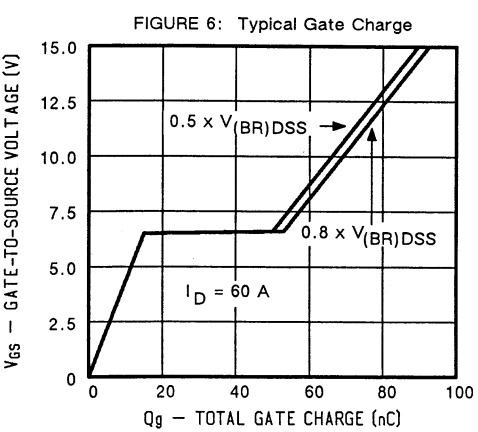


FIGURE 6: Typical Gate Charge



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Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

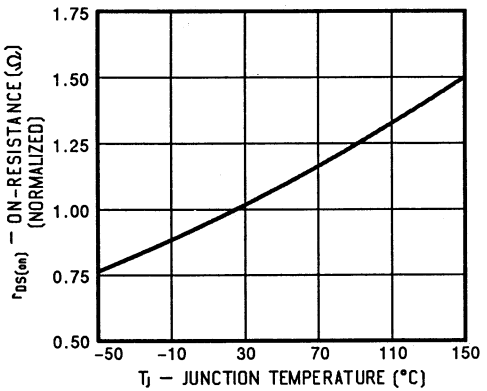


FIGURE 8: Typical Source-Drain Diode Forward Voltage

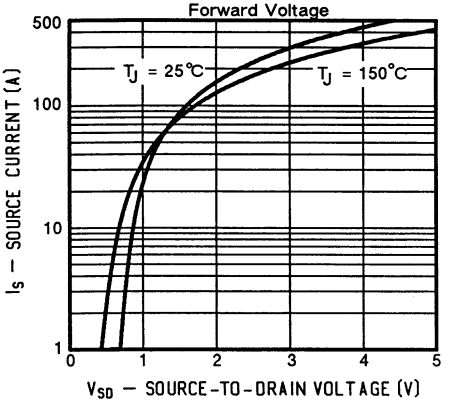


FIGURE 9: Maximum Drain Current vs. Case Temperature

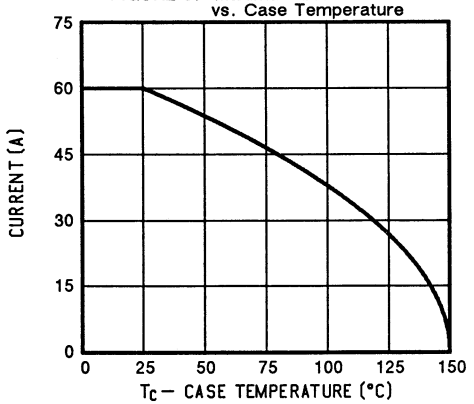
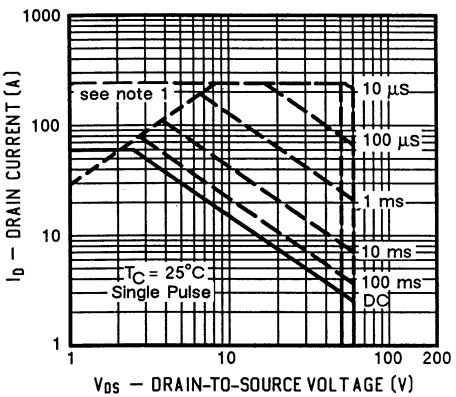
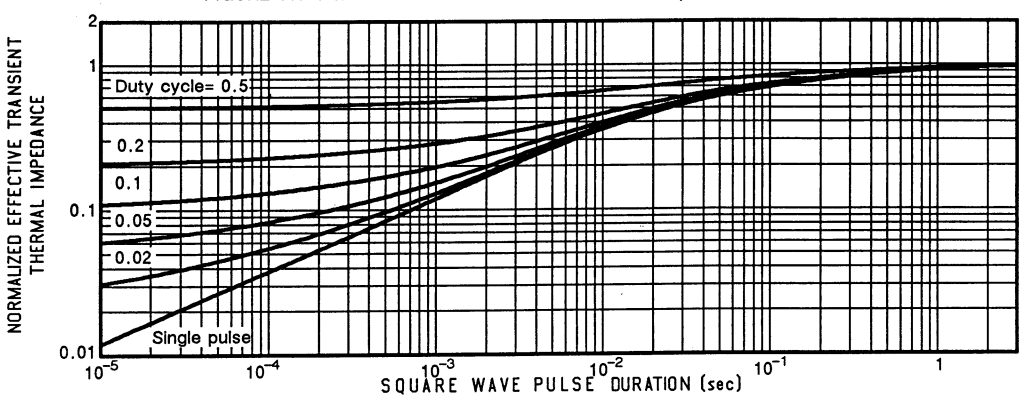


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

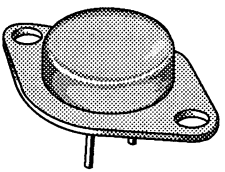
MOSPOWER

SMM70N06
SMM70N05

N-Channel Enhancement Mode Transistors

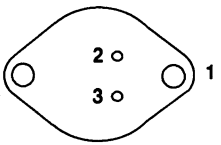
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SMM70N06	60	0.018	70
SMM70N05	50	0.018	70



TO-204AE (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SMM		Units
			70N06	70N05	
Drain-Source Voltage		V_{DS}	60	50	V
Gate-Source Voltage		V_{GS}	±40	±40	V
Continuous Drain Current	T_C = 25°C	I_D	70	70	A
	T_C = 100°C		43	43	A
Pulsed Drain Current[1]		I_{DM}	280	280	A
Power Dissipation	T_C = 25°C	P_D	250	250	W
	T_C = 100°C		100	100	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	0.50	K/W
Junction-to-Ambient	R_{thJA}	-	30	K/W
Case-to-Sink	R_{thCS}	0.1	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	SMM70N06 SMM70N05	$V_{(BR)DSS}$	60 50	65 55	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1000 µA		$V_{GS(th)}$	2.0	3.0	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	–	–	1000	µA
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V		$I_{D(on)}$	70	–	–	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 35 A		$r_{DS(on)}$	–	0.013	0.018	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 35 A, T_J = 125°C		$r_{DS(on)}$	–	0.020	0.027	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 35 A		g_{fs}	20	25	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	4800	5200	pF
Output Capacitance		C_{oss}	–	2000	2500	pF
Reverse Transfer Capacitance		C_{rss}	–	600	750	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 70 A (Gate charge is essentially independent of operating temperature)	Q_g	–	75	120	nC
Gate-Source Charge		Q_{gs}	–	17	–	nC
Gate-Drain Charge		Q_{gd}	–	41	–	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 0.86Ω I_D ≅ 35 A, V_{GEN} = 10 V R_G = 2.5Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	20	40	ns
Rise Time		t_r	–	30	60	ns
Turn-Off Delay Time		$t_{d(off)}$	–	45	90	ns
Fall Time		t_f	–	22	45	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	–	–	70	A
Pulsed Current[1]	I_{SM}	–	–	280	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	–	–	2.5	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs	t_{rr}	–	80	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs	Q_{rr}	–	0.2	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

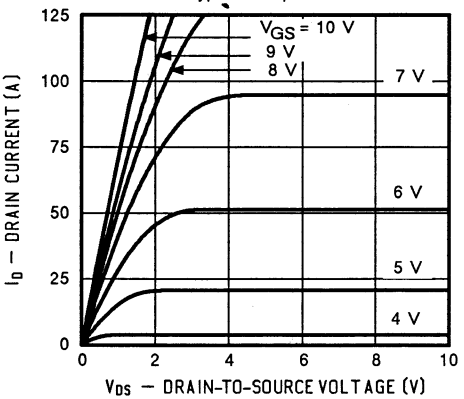


FIGURE 2: Typical Transfer Characteristics

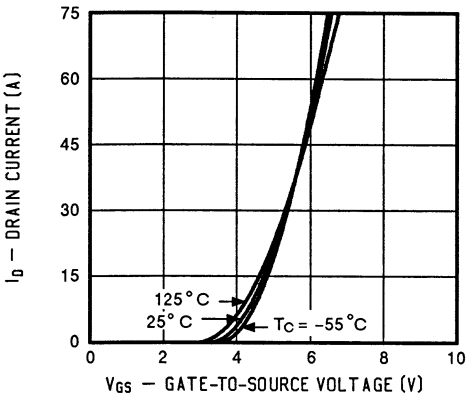


FIGURE 3: Typical Transconductance

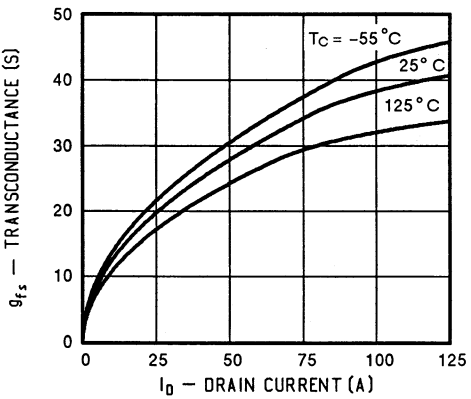


FIGURE 4: Typical On-Resistance

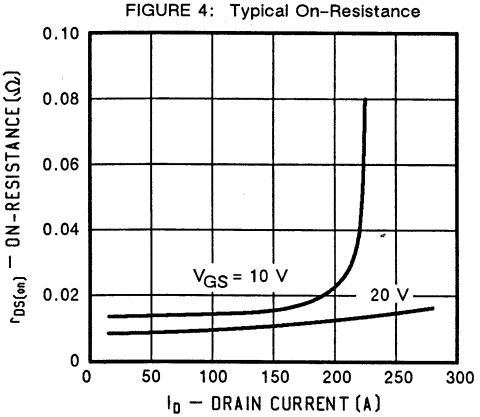


FIGURE 5: Typical Capacitance

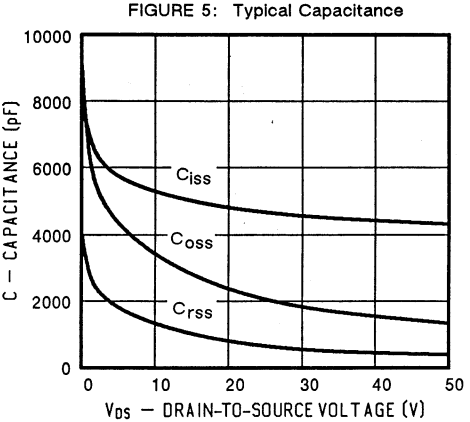
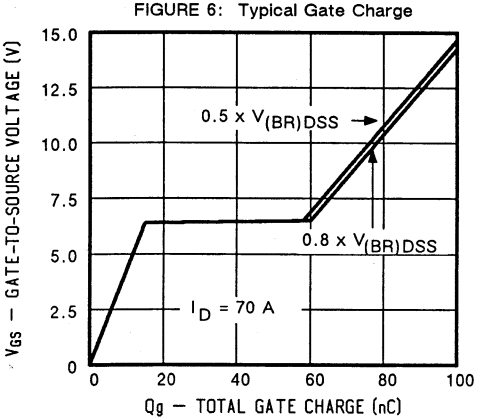


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

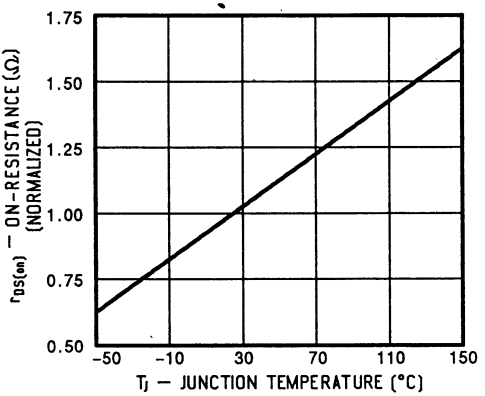


FIGURE 8: Typical Source-Drain Diode Forward Voltage

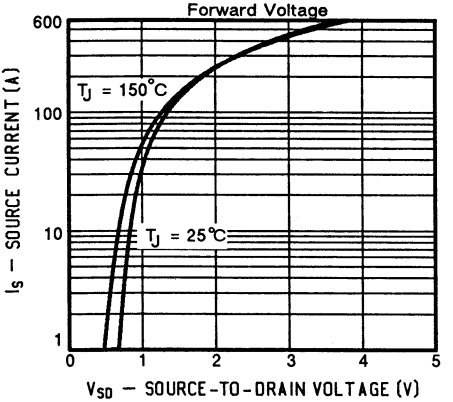


FIGURE 9: Maximum Drain Current vs. Case Temperature

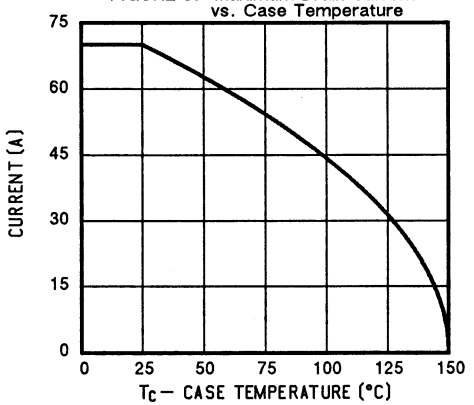
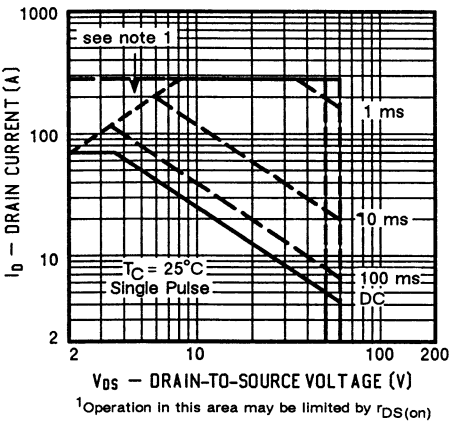


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case