Siliconix incorporated

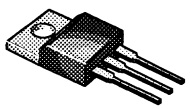
SMP3N50F

N-Channel Enhancement Mode Transistor
Fast Reverse Recovery

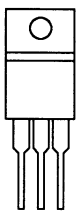
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	t_{rr} (ns)
500	3.0	2.5	250

TO-220AB



TOP VIEW



1 2 3

1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	2.5	A
	T_C = 100°C		1.6	
Pulsed Drain Current[1]		I_{DM}	12	
Avalanche Current (See Figure 9)		I_{AR}	2.5	
Repetitive Avalanche Energy[2]	L = 1 mH	E_{AR}	3	mJ
Power Dissipation	T_C = 25°C	P_D	48	W
	T_C = 100°C		19	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		2.6	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[2]Duty cycle ≤ 1%.

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA			500		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1000 µA			2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V				250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C				1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V			2.5		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 1.5 A		2.2		3.0	Ω
		V_{GS} = 10 V, I_D = 1.5 A, T_J = 125°C		4.4		6.0	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 1.5 A		1.5	1.0		S
DYNAMIC							
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		350			pF
Output Capacitance	C_{oss}			75			
Reverse Transfer Capacitance	C_{rss}			25			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 2.5 A		11		18	nC
Gate-Source Charge[2]	Q_{gs}			2		5	
Gate-Drain Charge[2]	Q_{gd}			7		11	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 250 V, R_L = 80 Ω I_D ≃ 2.5 A, V_{GEN} = 10 V, R_G = 25 Ω		7		60	ns
Rise Time[2]	t_r			15		50	
Turn-Off Delay Time[2]	$t_{d(off)}$			42		60	
Fall Time[2]	t_f			16		30	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)							
Continuous Current	I_S					3.0	A
Pulsed Current[3]	I_{SM}					12	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V				1.6	V
Reverse Recovery Time	t_{rr}	I_F = 3 A, dI_F/dt = 100 A/µs V_{DD} = 250 V	T_J = 25°C	135		250	ns
			T_J = 125°C	175		300	
Peak Reverse Recovery Current	$I_{RM(REC)}$		T_J = 25°C	5			A
			T_J = 125°C	7			
Reverse Recovery Charge	Q_{rr}		T_J = 25°C	0.34		1.2	µC
			T_J = 125°C	0.56		4.0	

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

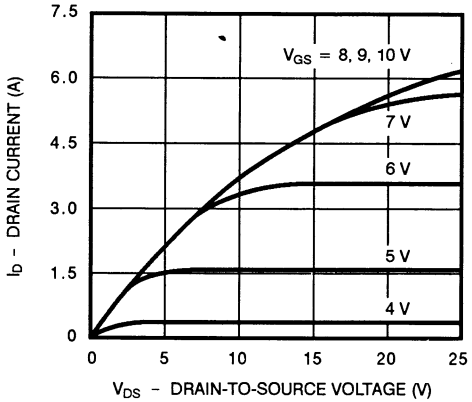


Figure 2. Transfer Characteristics

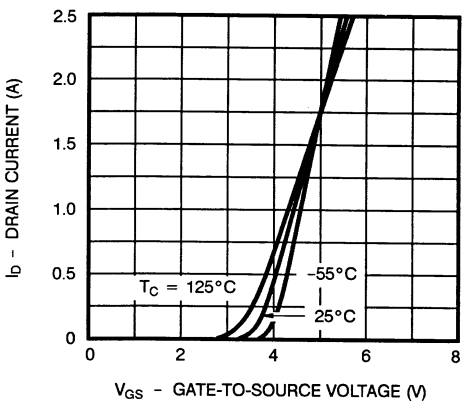


Figure 3. Transconductance

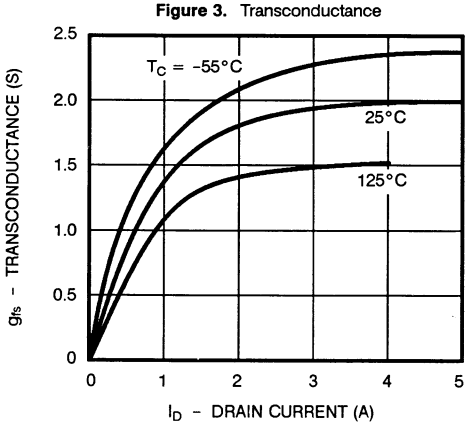


Figure 4. On-Resistance

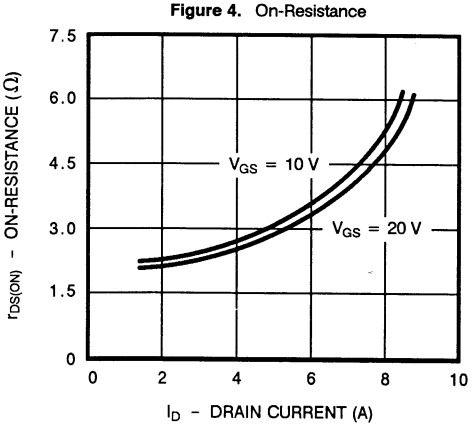


Figure 5. Capacitance

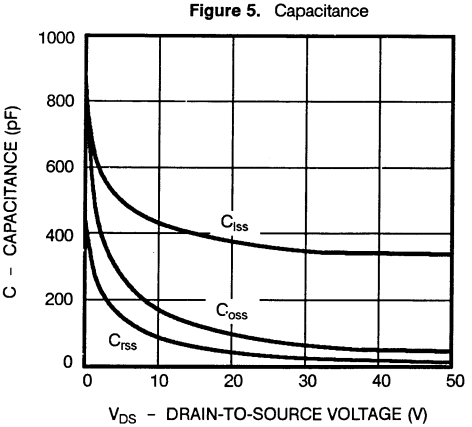
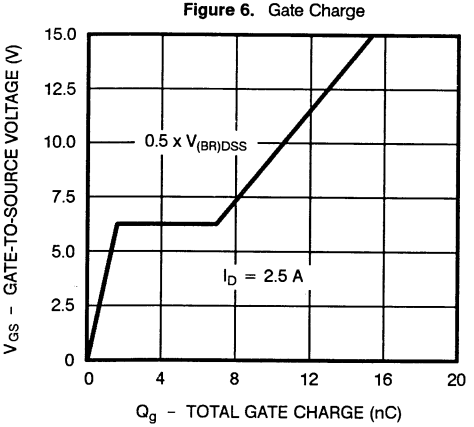


Figure 6. Gate Charge



TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

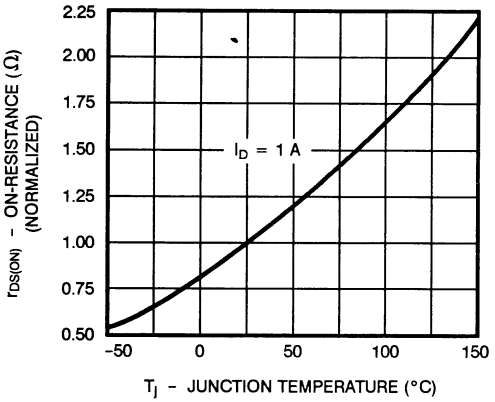
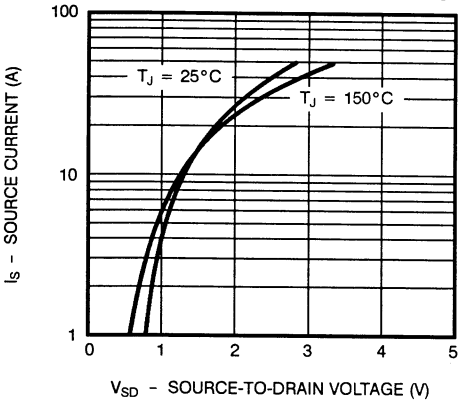


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

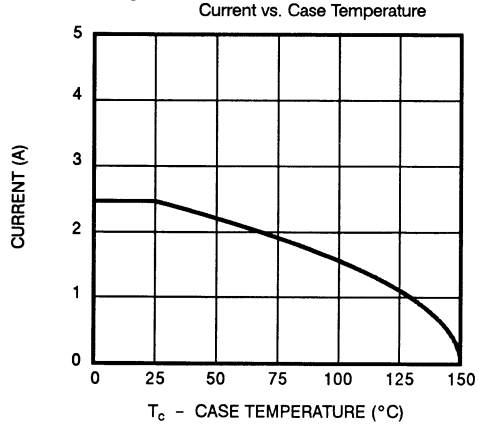


Figure 10. Safe Operating Area

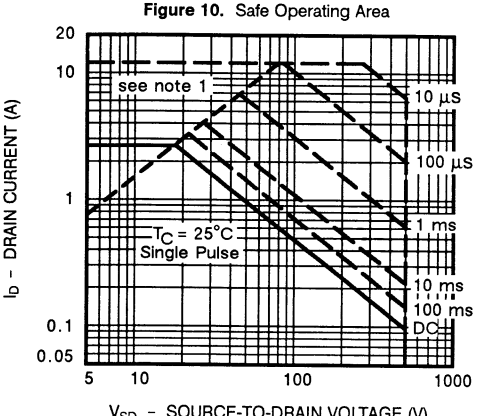
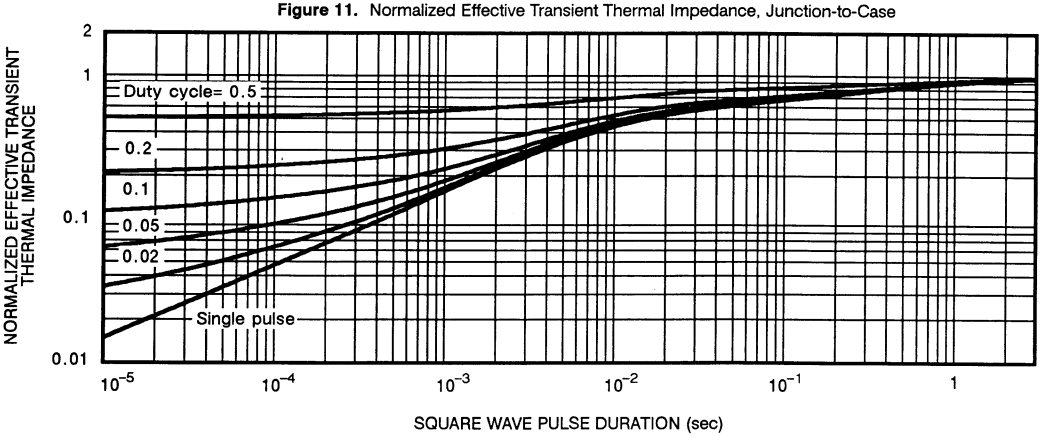


Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



DIODE CHARACTERISTICS

Figure 12. Typical Reverse Recovery Time vs. di/dt

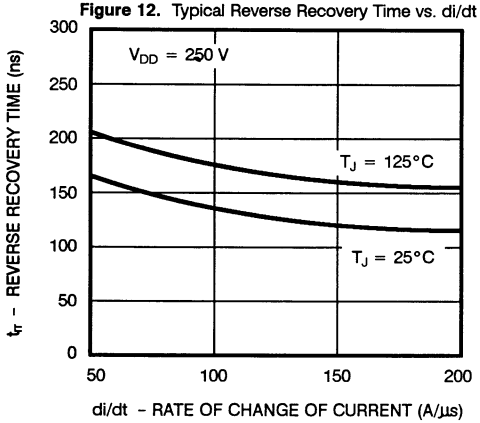


Figure 13. Typical Peak Reverse Recovery Current vs. di/dt

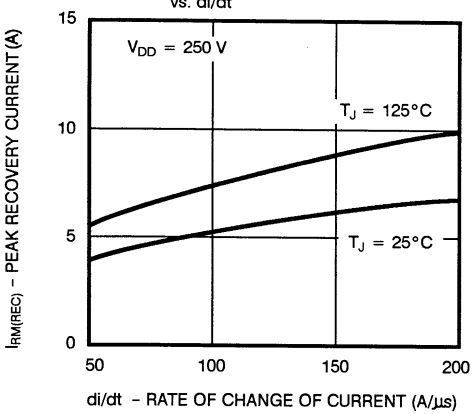


Figure 14. Commutating Safe Operating Area

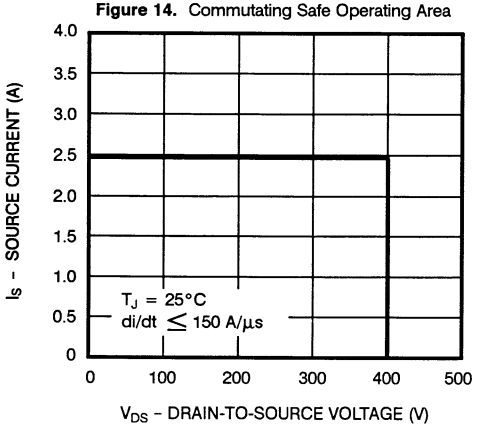


Figure 15. Typical dv/dt vs. di/dt

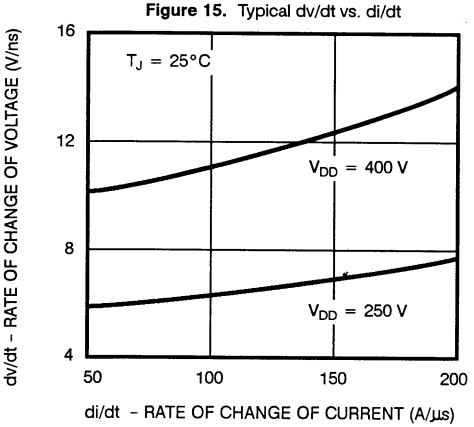
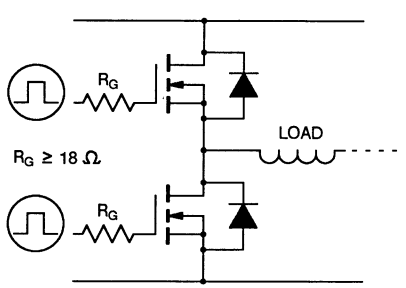
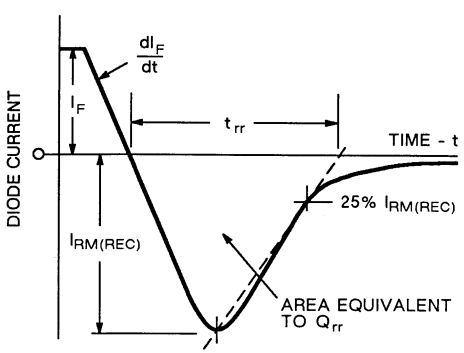


Figure 16. Minimum Value of Gate Resistor



Suggested Minimum Value of Gate Resistor to Operate within Commutating Safe Operating Area (See Figure 14).

Figure 17. Diode Reverse Recovery



4

Siliconix incorporated

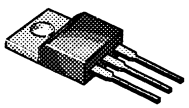
SMP4N60

N-Channel Enhancement Mode Transistor

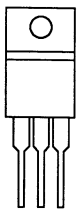
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
600	2.0	4.0

TO-220AB



TOP VIEW



1 2 3

1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	600	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	4.0	A
	T_C = 100°C		2.5	
Pulsed Drain Current[1]		I_{DM}	16	
Power Dissipation	T_C = 25°C	P_D	75	W
	T_C = 100°C		30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.67	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		600		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		4.0		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 2 A	1.8		2.0	Ω
		V_{GS} = 10 V, I_D = 2 A, T_J = 125°C	3.9		4.4	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 2 A		1.0		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	700			pF
Output Capacitance	C_{oss}		120			
Reverse Transfer Capacitance	C_{rss}		50			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 4 A	22		45	nC
Gate-Source Charge[2]	Q_{gs}		4		7	
Gate-Drain Charge[2]	Q_{gd}		12		24	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 300 V, R_L = 75 Ω, I_D ≃ 4 A, V_{GEN} = 10 V, R_G = 12 Ω	8		17	ns
Rise Time[2]	t_r		13		20	
Turn-Off Delay Time[2]	$t_{d(off)}$		48		60	
Fall Time[2]	t_f		22		35	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				4.0	A
Pulsed Current[3]	I_{SM}				16.0	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			1.5	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	500			ns
Reverse Recovery Charge	Q_{rr}		2.5			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

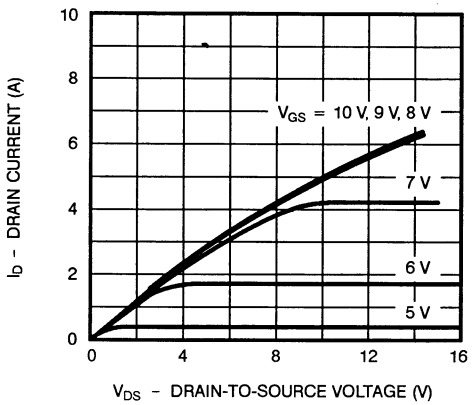


Figure 2. Transfer Characteristics

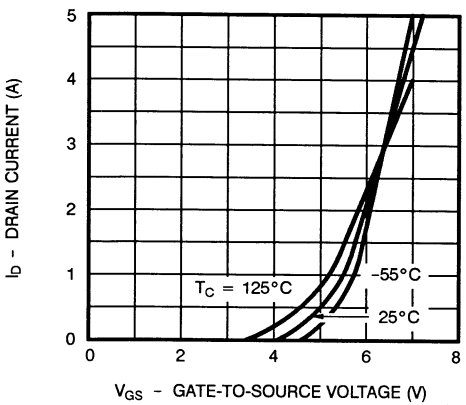


Figure 3. Transconductance

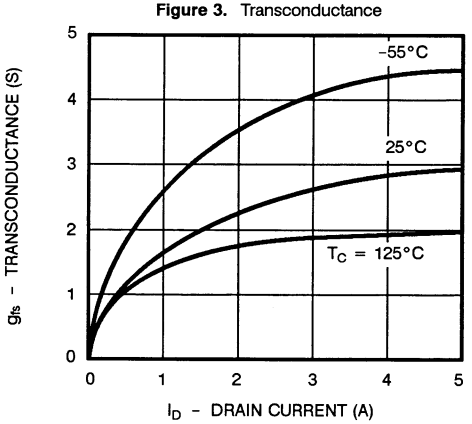


Figure 4. On-Resistance

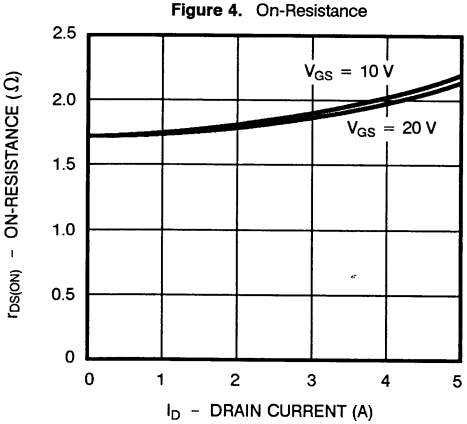


Figure 5. Capacitance

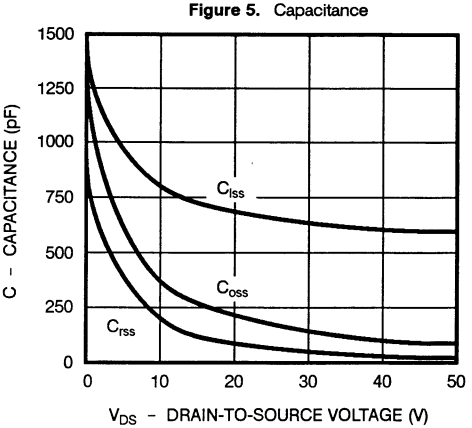
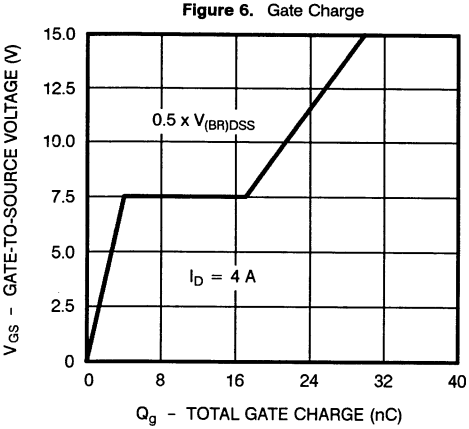


Figure 6. Gate Charge



TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

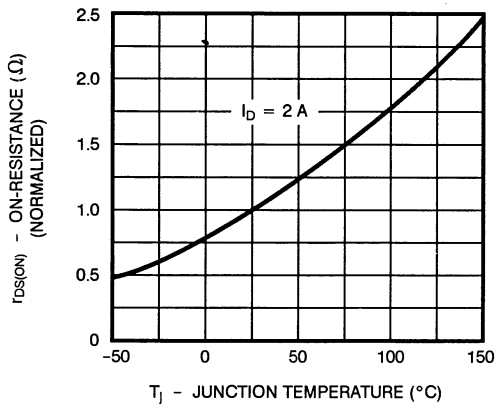
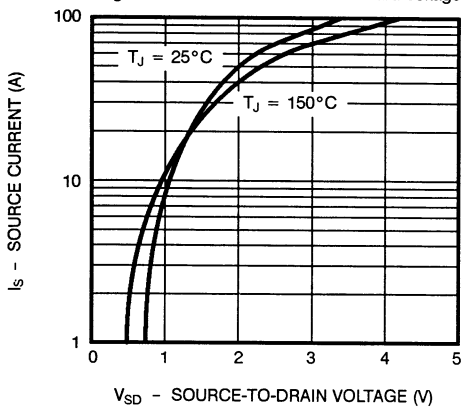


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

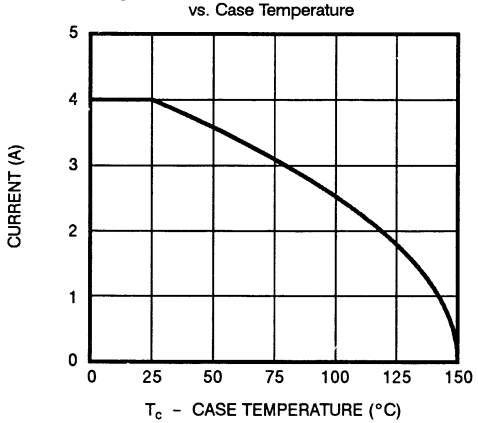
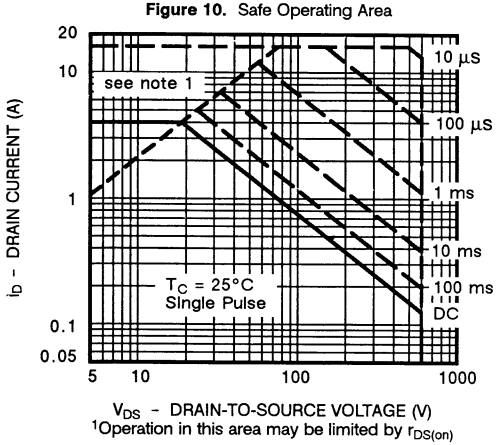
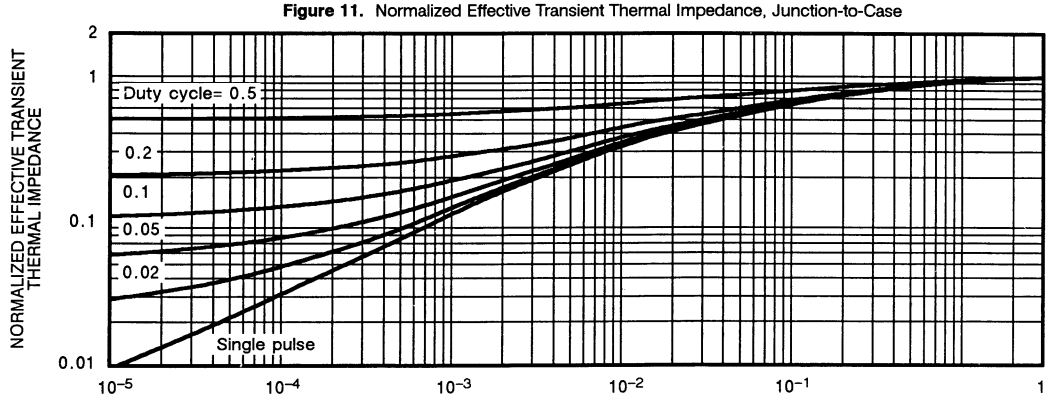


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

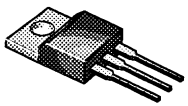
SMP5N50F

N-Channel Enhancement Mode Transistor
Fast Reverse Recovery

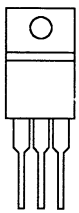
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	t_{rr} (ns)
500	1.5	4.5	250

TO-220AB



TOP VIEW



1 2 3

1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	4.5	A
	T_C = 100°C		3.0	
Pulsed Drain Current[1]		I_{DM}	20	
Avalanche Current (See Figure 9)		I_{AR}	4.5	
Repetitive Avalanche Energy[2]	L = 1 mH	E_{AR}	10	mJ
Power Dissipation	T_C = 25°C	P_D	75	W
	T_C = 100°C		30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.67	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[2]Duty cycle ≤ 1%.

4

SMP5N50F

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		500		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1000 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		5.0		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 2.5 A	1.2		1.5	Ω
		V_{GS} = 10 V, I_D = 25. A, T_J = 125°C	2.6		3.3	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 2.5 A	3.0	2.5		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	720			pF
Output Capacitance	C_{oss}		130			
Reverse Transfer Capacitance	C_{rss}		40			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 4.5 A	22		30	nC
Gate-Source Charge[2]	Q_{gs}		3.5		7	
Gate-Drain Charge[2]	Q_{gd}		11		20	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 250 V, R_L = 50 Ω I_D ≃ 4.5 A, V_{GEN} = 10 V, R_G = 7.5 Ω	8		30	ns
Rise Time[2]	t_r		13		30	
Turn-Off Delay Time[2]	$t_{d(off)}$		32		55	
Fall Time[2]	t_f		20		30	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				5.0	A
Pulsed Current[3]	I_{SM}				20	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			1.6	V
Reverse Recovery Time	t_{rr}	I_F = 5 A, dI_F/dt = 100 A/µs, V_{DD} = 250 V; T_J = 25°C	160		250	ns
		T_J = 125°C	220		300	
Peak Reverse Recovery Current	$I_{RM(REC)}$	T_J = 25°C	9			A
		T_J = 125°C	11			
Reverse Recovery Charge	Q_{rr}	T_J = 25°C	0.72		1.2	µC
		T_J = 125°C	1.16		4.0	

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

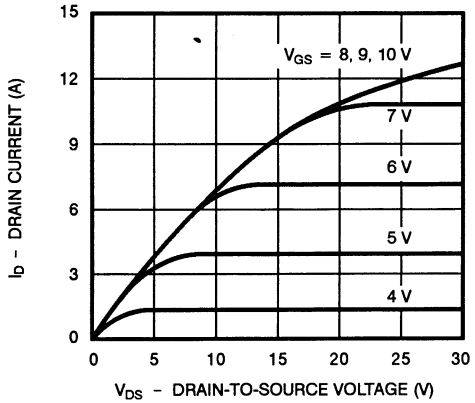


Figure 2. Transfer Characteristics

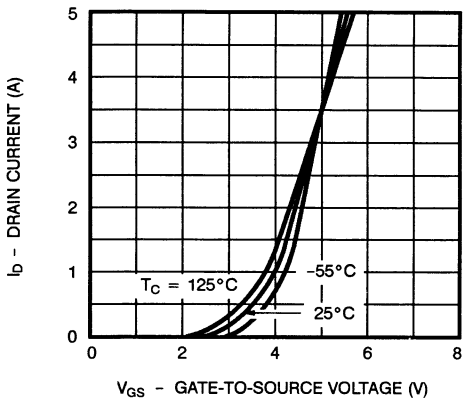


Figure 3. Transconductance

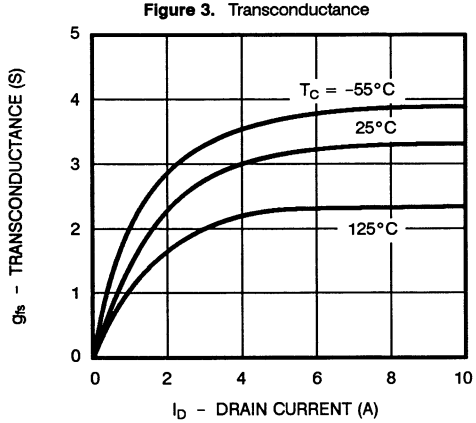


Figure 4. On-Resistance

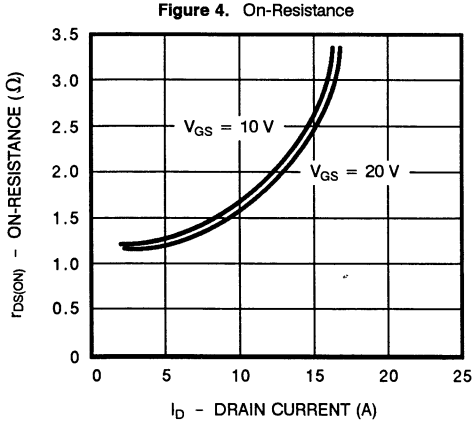


Figure 5. Capacitance

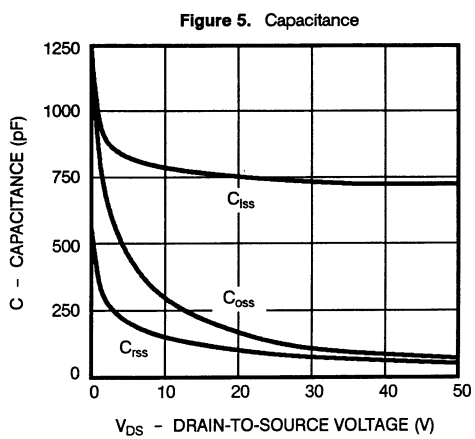
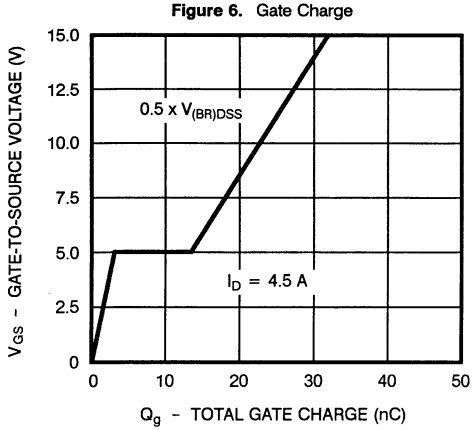


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

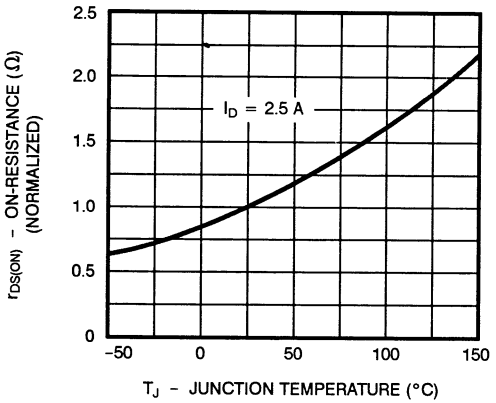
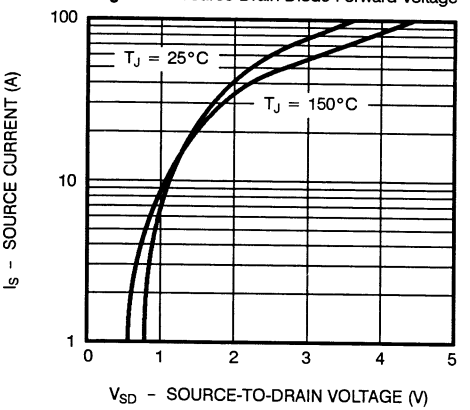


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

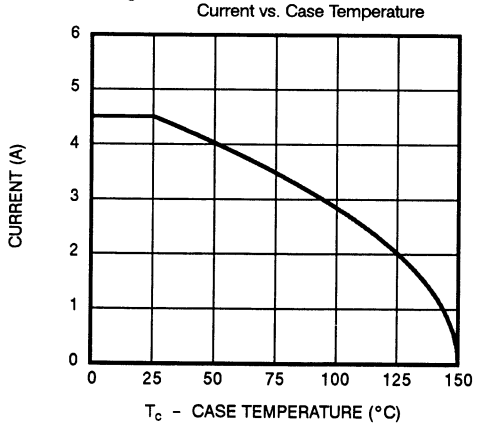


Figure 10. Safe Operating Area

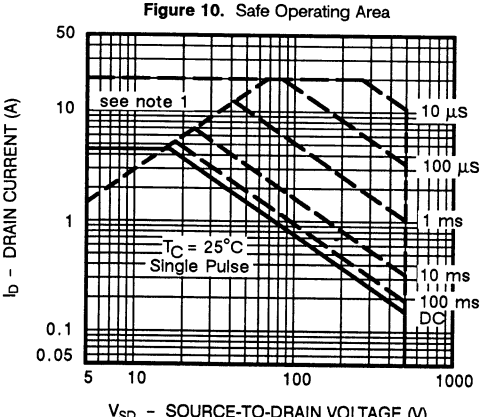
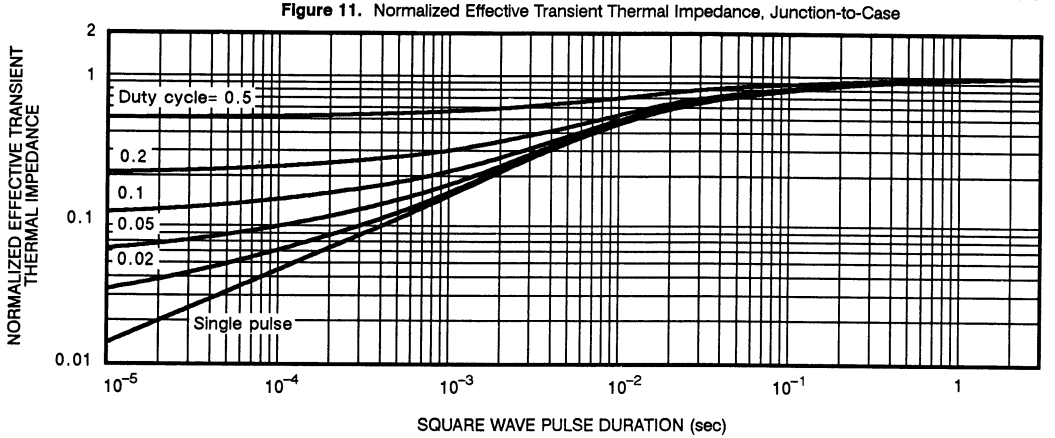


Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



DIODE CHARACTERISTICS

Figure 12. Typical Reverse Recovery Time vs. di/dt

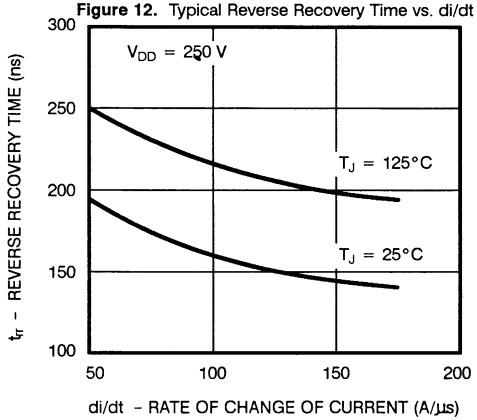


Figure 13. Typical Peak Reverse Recovery Current vs. di/dt

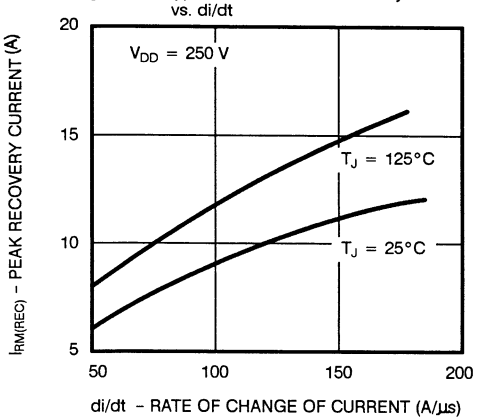


Figure 14. Commutating Safe Operating Area

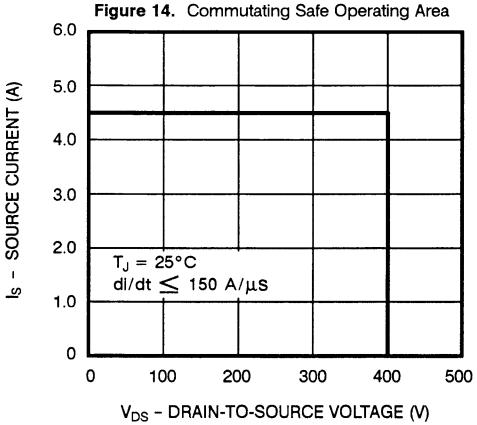


Figure 15. Typical dv/dt vs. di/dt

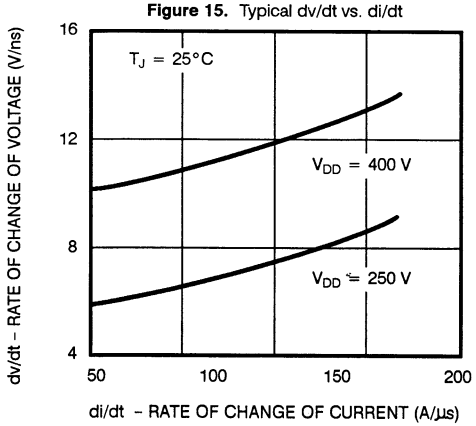
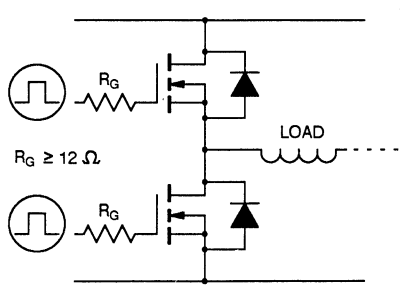
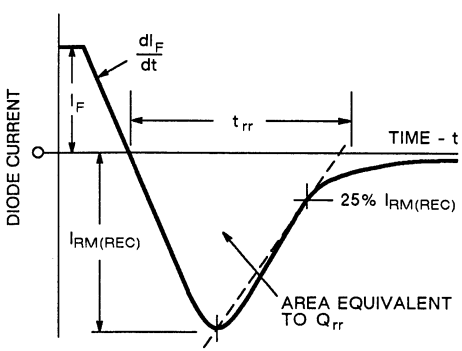


Figure 16. Minimum Value of Gate Resistor



Suggested Minimum Value of Gate Resistor to Operate within Commutating Safe Operating Area (See Figure 14).

Figure 17. Diode Reverse Recovery



4

Siliconix incorporated

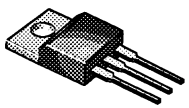
SMP7N60

N-Channel Enhancement Mode Transistor

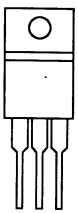
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
600	1.1	7.0

TO-220AB



TOP VIEW



1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	600	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	7.0	A
	T_C = 100°C		4.5	
Pulsed Drain Current[1]		I_{DM}	28.0	
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.0	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		600		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 600 V, V_{GS} = 0 V			250	µA
		V_{DS} = 480 V, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 9 V, V_{GS} = 10 V		7.0		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 3.5 A	0.9		1.1	Ω
		V_{GS} = 10 V, I_D = 3.5 A, T_J = 125°C			2.4	
Forward Transconductance[1]	g_{fs}	V_{DS} = 10 V, I_D = 3.5 A		2.0		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1200			pF
Output Capacitance	C_{oss}		200			
Reverse Transfer Capacitance	C_{rss}		80			
Total Gate Charge[2]	Q_g	V_{DS} = 300 V, V_{GS} = 10 V, I_D = 7 A	42		60	nC
Gate-Source Charge[2]	Q_{gs}		6.3		10	
Gate-Drain Charge[2]	Q_{gd}		25		39	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 300 V, R_L = 42 Ω, $I_D \simeq$ 7 A, V_{GEN} = 10 V, R_G = 9 Ω	11		20	ns
Rise Time[2]	t_r		27		35	
Turn-Off Delay Time[2]	$t_{d(off)}$		64		83	
Fall Time[2]	t_f		29		40	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				7	A
Pulsed Current[3]	I_{SM}				28	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			1.5	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	500			ns
Reverse Recovery Charge	Q_{rr}		3.5			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

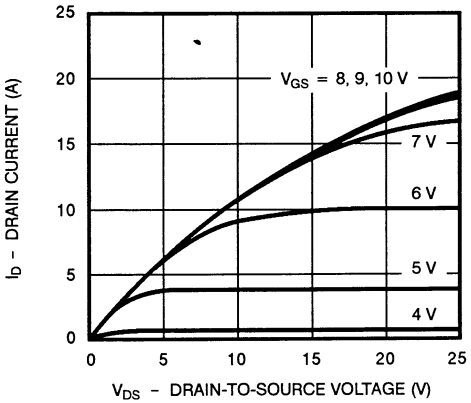


Figure 2. Transfer Characteristics

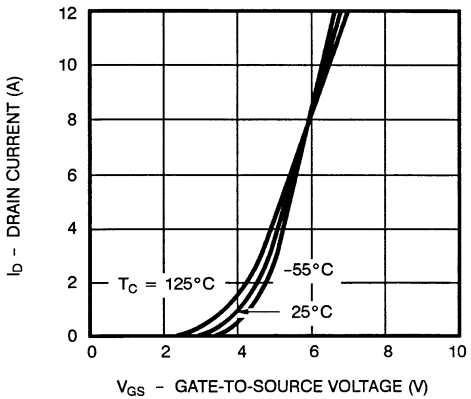


Figure 3. Transconductance

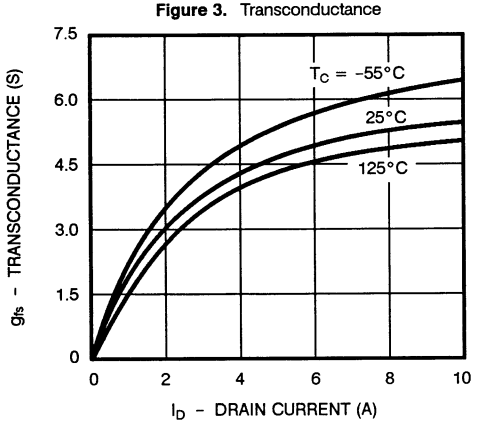


Figure 4. On-Resistance

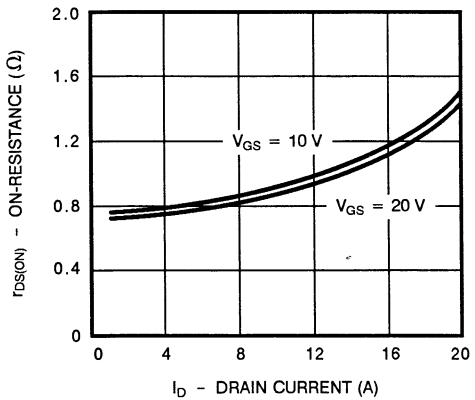


Figure 5. Capacitance

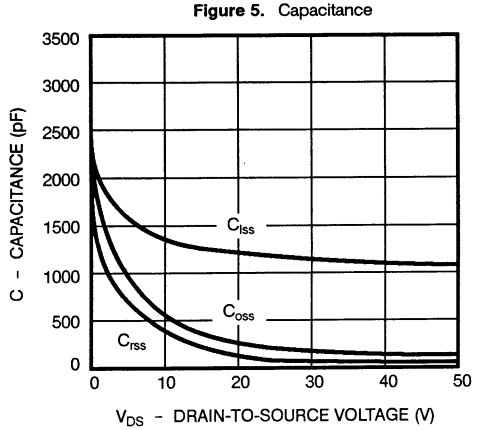
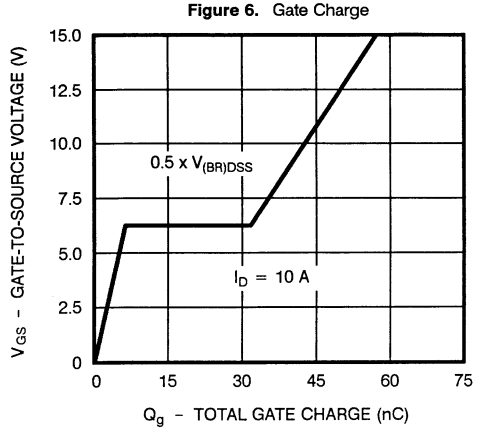


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

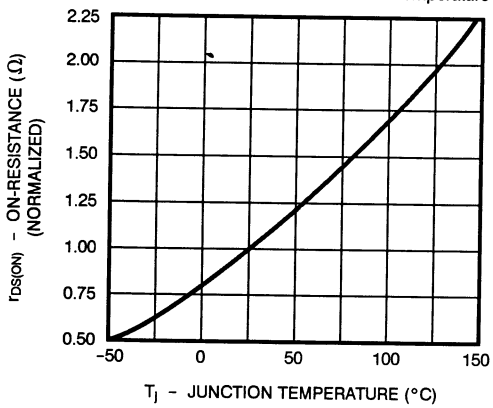
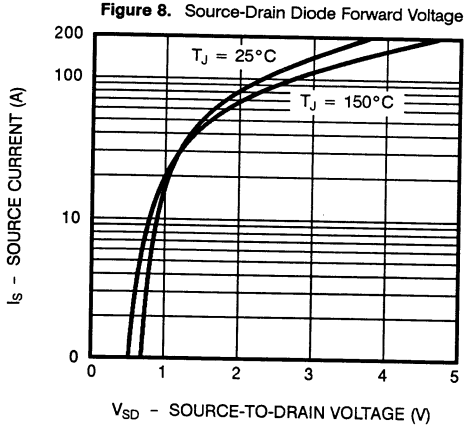


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

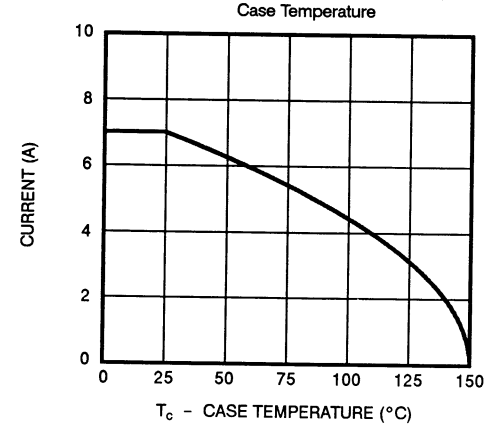
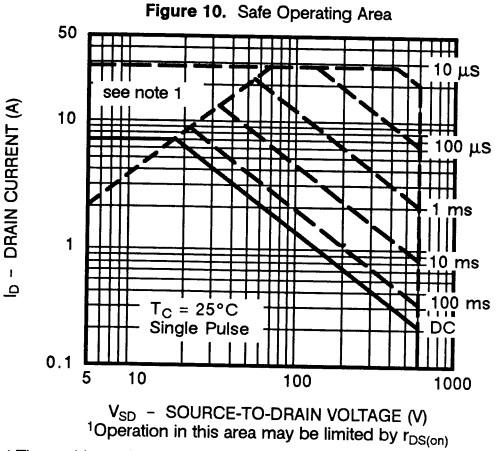
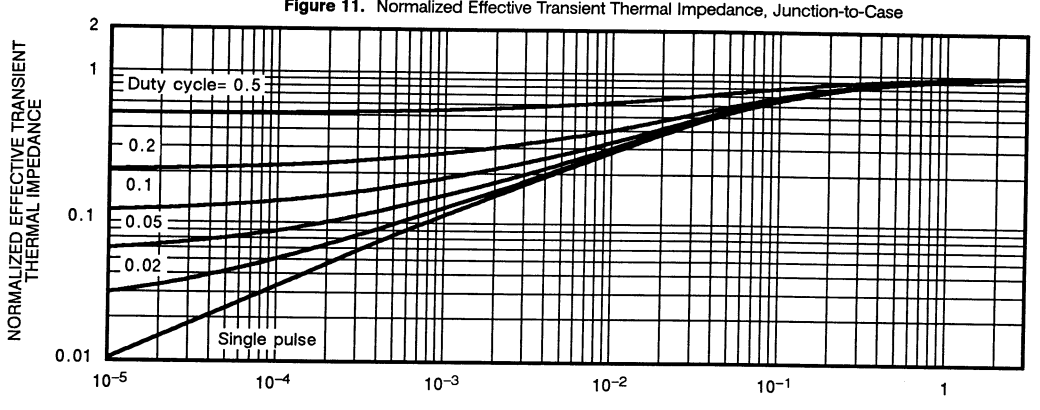


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

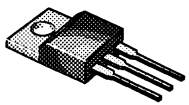
SMP8N50F

N-Channel Enhancement Mode Transistor
Fast Reverse Recovery

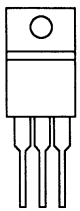
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	t_{rr} (ns)
500	0.85	8.0	250

TO-220AB



TOP VIEW



1 2 3

1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	8.0	A
	T_C = 100°C		5.0	
Pulsed Drain Current[1]		I_{DM}	32	
Avalanche Current (See Figure 9)		I_{AR}	8.0	
Repetitive Avalanche Energy[2]	L = 1 mH	E_{AR}	32	mJ
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.0	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[2]Duty cycle ≤ 1%.

SMP8N50F

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA			500		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1000 µA			2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V				250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C				1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V			8.0		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 4 A		0.60		0.85	Ω
		V_{GS} = 10 V, I_D = 4 A, T_J = 125°C		1.20		1.65	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 4 A		4.3	4.0		S
DYNAMIC							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		1360			pF
Output Capacitance	C_{oss}			300			
Reverse Transfer Capacitance	C_{rss}			80			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 8 A		45		60	nC
Gate-Source Charge[2]	Q_{gs}			7.5		15	
Gate-Drain Charge[2]	Q_{gd}			25		35	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 250 V, R_L = 31 Ω $I_D \simeq$ 8 A, V_{GEN} = 10 V, R_G = 4.7 Ω		10		35	ns
Rise Time[2]	t_r			20		25	
Turn-Off Delay Time[2]	$t_{d(off)}$			40		90	
Fall Time[2]	t_f			20		30	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)							
Continuous Current	I_S					8.0	A
Pulsed Current[3]	I_{SM}					32	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V				2.0	V
Reverse Recovery Time	t_{rr}	I_F = 8 A, dI_F/dt = 100 A/µs V_{DD} = 250 V	T_J = 25°C T_J = 125°C	170 240		250 300	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$		T_J = 25°C T_J = 125°C	11 16			A
Reverse Recovery Charge	Q_{rr}		T_J = 25°C T_J = 125°C	0.95 2.0		1.6 4.0	µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

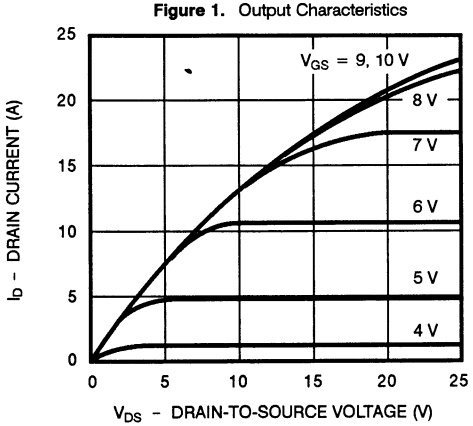


Figure 2. Transfer Characteristics

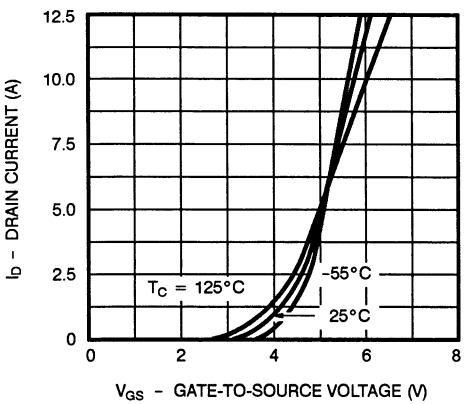


Figure 3. Transconductance

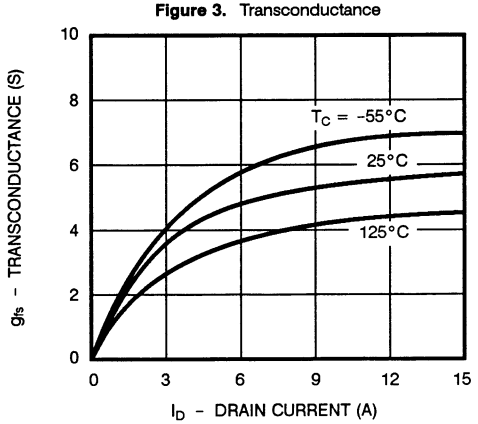


Figure 4. On-Resistance

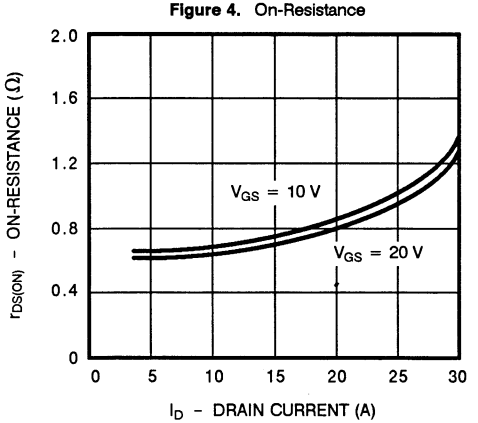


Figure 5. Capacitance

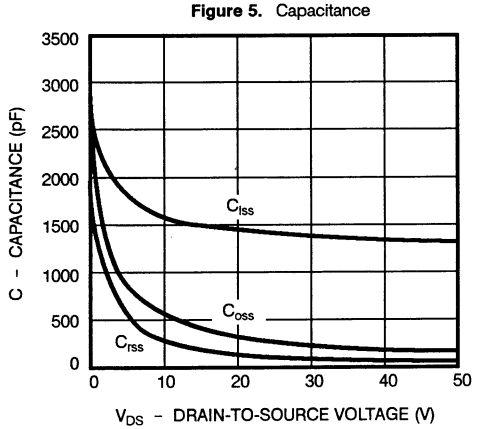
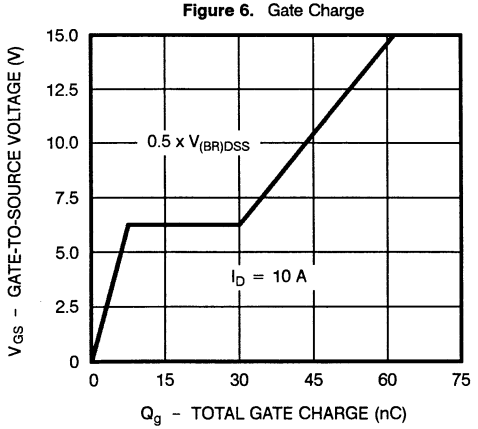


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

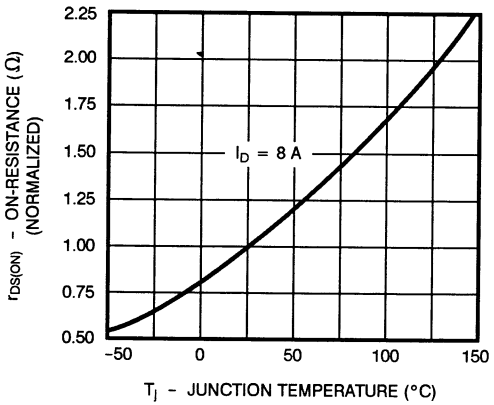
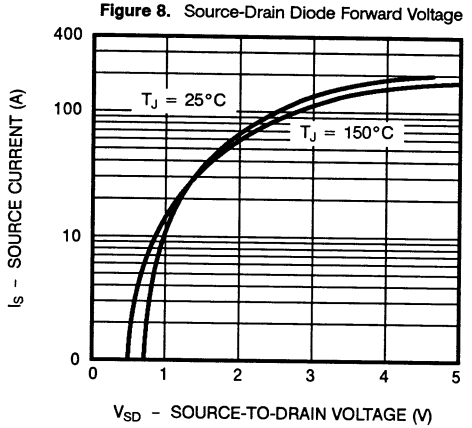


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

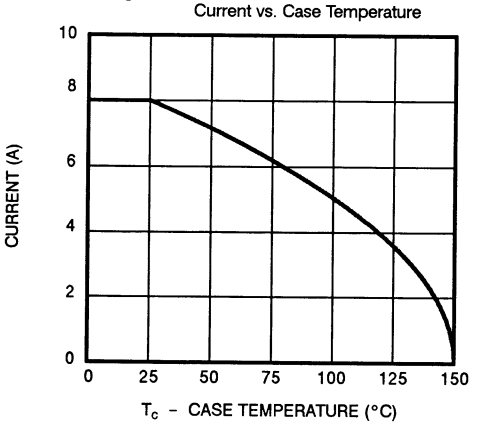
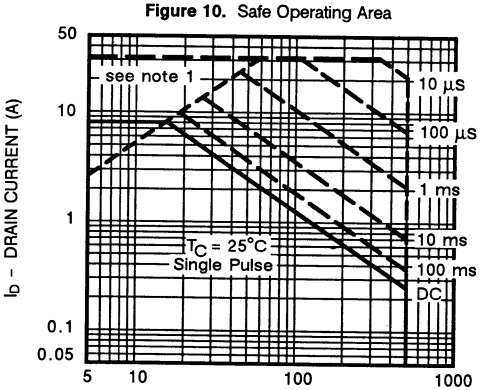
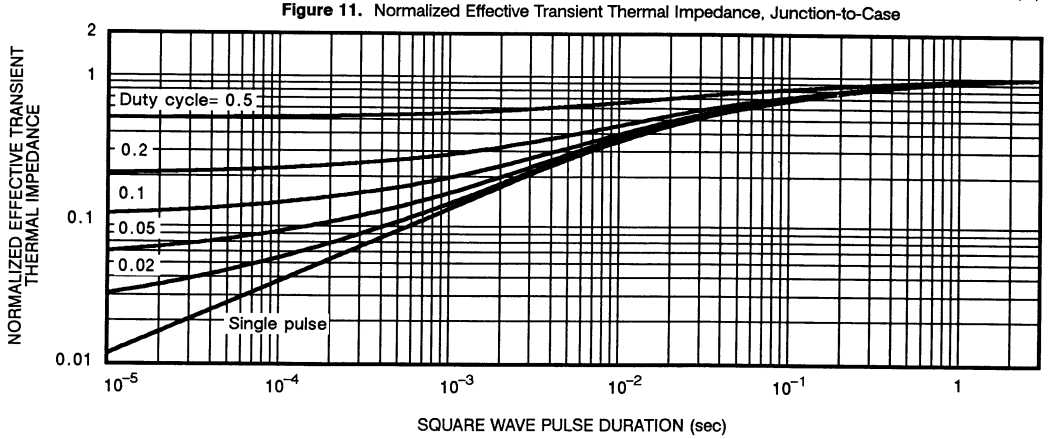


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



DIODE CHARACTERISTICS

Figure 12. Typical Reverse Recovery Time vs. di/dt

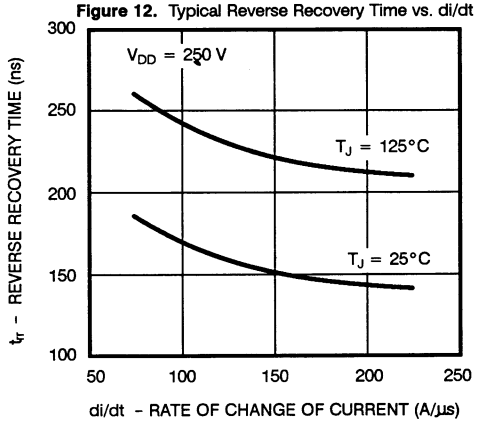


Figure 13. Typical Peak Reverse Recovery Current vs. di/dt

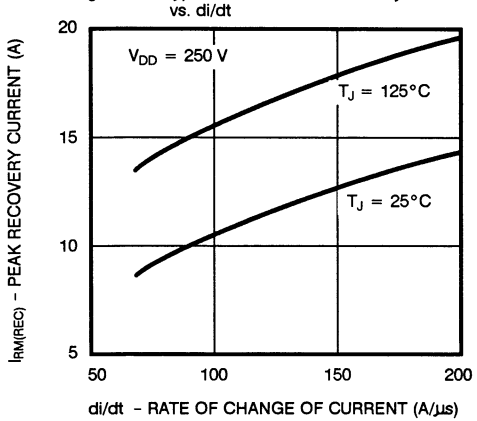


Figure 14. Commutating Safe Operating Area

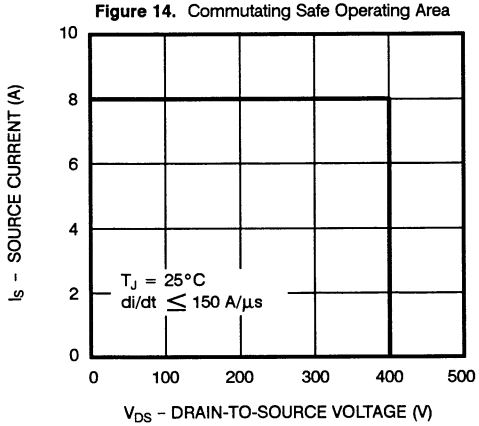


Figure 15. Typical dv/dt vs. di/dt

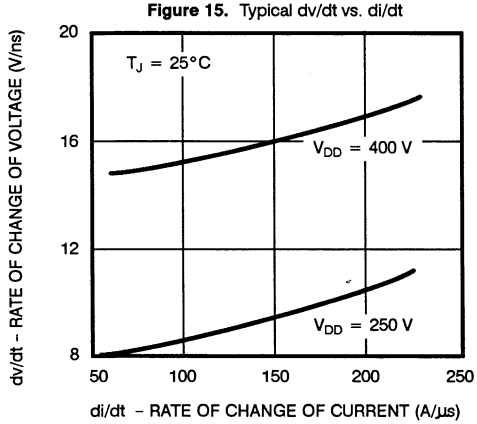
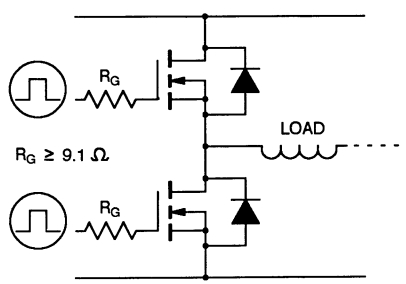
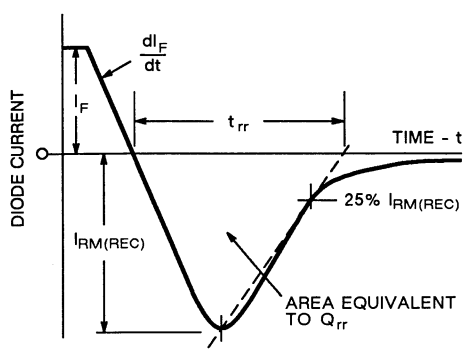


Figure 16. Minimum Value of Gate Resistor



Suggested Minimum Value of Gate Resistor to Operate within Commutating Safe Operating Area (See Figure 14).

Figure 17. Diode Reverse Recovery



4